The documentation and process conversion measures necessary to comply with this document shall be completed by 24 June 2007.

INCH-POUND

MIL-PRF-19500/255V
24 March 2007
SUPERSEDING
MIL-PRF-19500/255U
26 July 2005

PERFORMANCE SPECIFICATION SHEET

* SEMICONDUCTOR DEVICE, TRANSISTOR, NPN, SILICON, SWITCHING, TYPES 2N2221A, 2N2221AL, 2N2222A, 2N2222AL, 2N2221AUA, 2N2222AUA, 2N2221AUB, 2N2222AUB, 2N2221AUBC, AND 2N2222AUBC, JAN, JANJ, JANTX, JANTXV, JANTXVM, JANTXVD, JANTXVP, JANTXVL, JANTXVR, JANTXVF, JANTXVG, JANTXVH, JANS, JANSM, JANSD, JANSP, JANSL, JANSR, JANHCF, JANHCG, JANSH, JANHC, JANHCM, JANHCD, JANHCP, JANHCL, JANHCR, JANHCF, JANHCG, JANHCH, JANKC, JANKCM, JANKCD, JANKCP, JANKCL, JANKCR, JANKCF, JANKCG, AND JANKCH

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for NPN, silicon, switching transistors. Five levels of product assurance are provided for each encapsulated device type as specified in MIL-PRF-19500, and two levels of product assurance are provided for each unencapsulated device type. Provisions for radiation hardness assurance (RHA) to four radiation levels is provided for JANTXV, JANS, JANHC, and JANKC product assurance levels. RHA level designators “M”, “D”, “P“, “L”, “R”, “F’, “G” and “H” are appended to the device prefix to identify devices, which have passed RHA requirements.

* 1.2 Physical dimensions. See figure 1 (similar to TO-18), figures 2, 3, and 4 (surface mount case outlines UA, UB, and UBC), and figures 5 and 6 (JANHC and JANKC).

Comments, suggestions, or questions on this document should be addressed to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://assist.daps.dla.mil .

* 1.3 Maximum ratings. Unless otherwise specified T_A = +25°C.

I_C	V_{CBO}	V_{CEO}	V_{EBO}	T_J and T_{STG}
mA dc	V dc	V dc	V dc	°C
800	75	50	6	-65 to +200

Types	P_T T_A = +25°C (1) (2)	P_T T_C = +25°C (1) (2)	P_T $T_{SP(IS)}$ = +25°C (1) (2)	P_T $T_{SP(AM)}$ = +25°C (1) (2)	$R_{\theta JA}$ (2) (3)	$R_{\theta JC}$ (2) (3)	$R_{\theta JSP(IS)}$ (2) (3)	$R_{\theta JSP(AM)}$ (2) (3)
	W	W	W	W	°C/W	°C/W	°C/W	°C/W
2N2221A, AL	0.50	1	N/A	N/A	325	150	N/A	N/A
2N2222A, AL	0.50	1	N/A	N/A	325	150	N/A	N/A
2N2221AUA	0.50 (4)	N/A	1	1.5	325 (4)	N/A	110	40
2N2222AUA	0.50 (4)	N/A	1	1.5	325 (4)	N/A	110	40
2N2221AUB and UBC	0.50 (4)	N/A	1	N/A	325 (4)	N/A	90	N/A
2N2222AUB and UBC	0.50 (4)	N/A	1	N/A	325 (4)	N/A	90	N/A

(1) For derating, see figures 7, 8, 9, 10, and 11.
(2) See 3.3 for abbreviations.
(3) For thermal impedance curves, see figures 12, 13, 14, 15, and 16.
(4) For non-thermal conductive PCB or unknown PCB surface mount conditions in free air, substitute figures 7 and 12 for the UA, UB, and UC package and use $R_{\theta JA}$.

* 1.4 Primary electrical characteristics. Unless otherwise specified, T_A = +25°C.

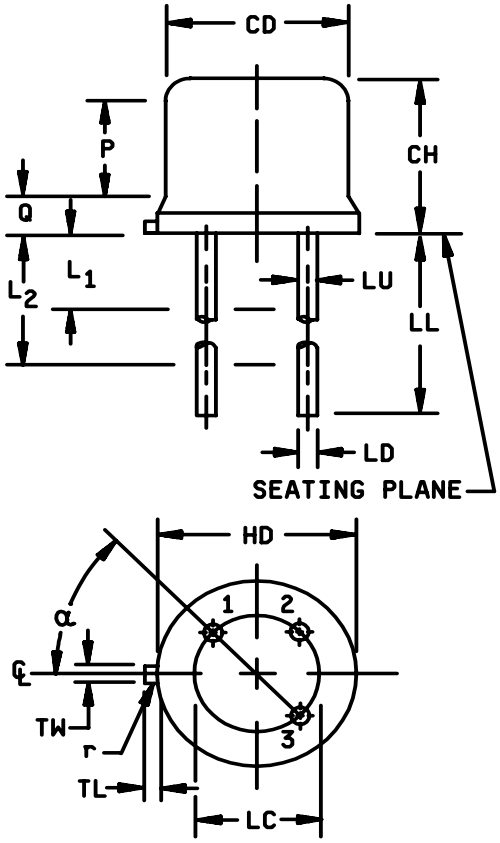
	h_{FE} at V_{CE} = 10 V dc									
	h_{FE1} I_C = 0. 1 mA dc		h_{FE2} I_C = 1.0 mA dc		h_{FE3} I_C = 10 mA dc		h_{FE4} (1) I_C = 150 mA dc		h_{FE5} (1) I_C = 500 mA dc	
	AL, UA, UB, UBC, 2N2221A, 2N2222A		AL, UA, UB, UBC, 2N2221A, 2N2222A		AL, UA, UB, UBC, 2N2221A, 2N2222A		AL, UA, UB, UBC, 2N2221A, 2N2222A		AL, UA, UB, UBC, 2N2221A, 2N2222A	
Min	30	50	35	75	40	100	40	100	20	30
Max			150	325			120	300		

Types	Limit	/h_{fe}/ f = 100 MHz V_{CE} = 20 V dc I_C = 20 mA dc	C_{obo} 100 kHz ≤ f ≤ 1 MHz V_{CB} = 10 V dc I_E = 0	Switching (saturated)	
				t_{on} See figure 17	t_{off} See figure 18
			pF	ns	ns
2N2221A, 2N2222A AL, UA, UB, and UBC	Min	2.5			
	Max		8	35	300

Types	Limit	$V_{CE(sat)1}$ (1) I_C = 150 mA dc I_B = 15 mA dc	$V_{CE(sat)2}$ (1) I_C = 500 mA dc I_B = 50 mA dc	$V_{BE(sat)1}$ (1) I_C = 150 mA dc I_B = 15 mA dc	$V_{BE(sat)2}$ (1) I_C = 500 mA dc I_B = 50 mA dc
		V dc	V dc	V dc	V dc
2N2221A, 2N2222A AL, UA, UB, and UBC	Min			0.6	
	Max	0.3	1.0	1.2	2.0

(1) Pulsed see 4.5.1.

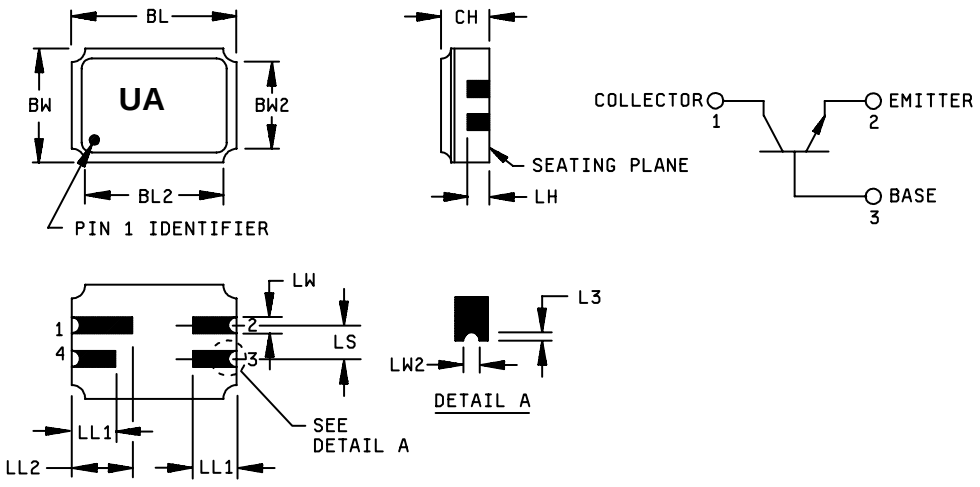
Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.178	.195	4.52	4.95	
CH	.170	.210	4.32	5.33	
HD	.209	.230	5.31	5.84	
LC	.100 TP		2.54 TP		6
LD	.016	.021	0.41	0.53	7,8
LL	.500	.750	12.70	19.05	7,8,13
LU	.016	.019	0.41	0.48	7,8
L_1		.050		1.27	7,8
L_2	.250		6.35		7,8
P	.100		2.54		
Q		.030		0.76	5
TL	.028	.048	0.71	1.22	3,4
TW	.036	.046	0.91	1.17	3
r		.010		0.25	10
α	45° TP		45° TP		6
1, 2, 9, 11, 12, 13					



NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Beyond r (radius) maximum, TL shall be held for a minimum length of .011 inch (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC.
7. Dimension LU applies between L_1 and L_2. Dimension LD applies between L_2 and LL minimum. Diameter is uncontrolled in L_1 and beyond LL minimum.
8. All three leads.
9. The collector shall be internally connected to the case.
10. Dimension r (radius) applies to both inside corners of tab.
11. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
12. Lead 1 = emitter, lead 2 = base, lead 3 = collector.
13. For L suffix devices, dimension LL = 1.5 inches (38.10 mm) min. and 1.75 inches (44.45 mm) max.

FIGURE 1. Physical dimensions (similar to TO-18).



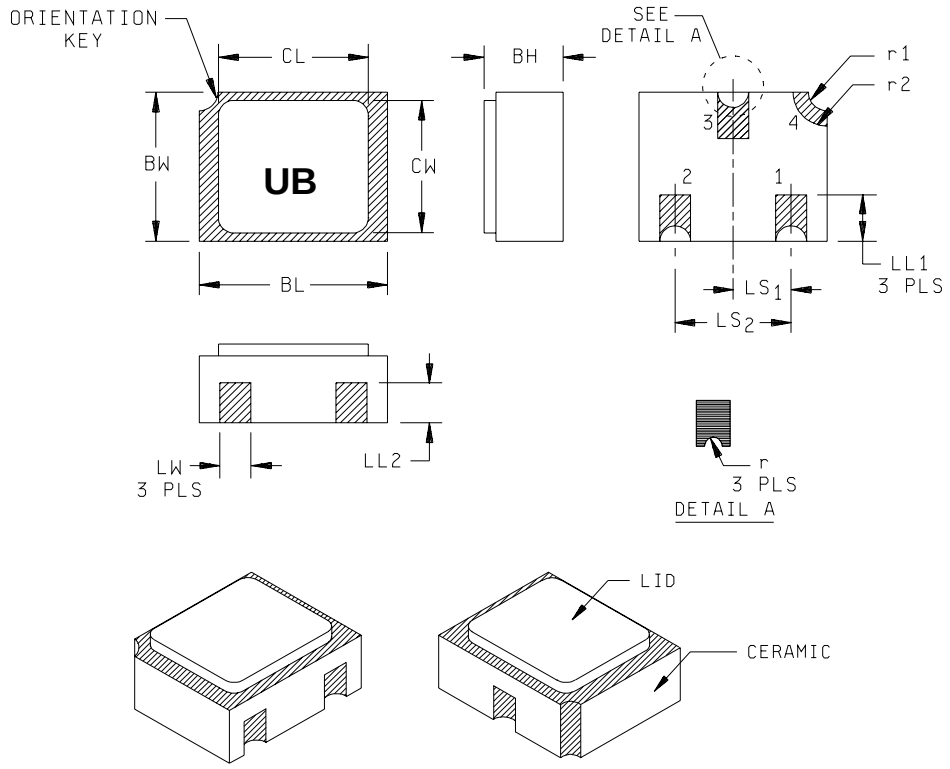
Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.215	.225	5.46	5.71	
BL2		.225		5.71	
BW	.145	.155	3.68	3.93	
BW2		.155		3.93	
CH	.061	.075	1.55	1.90	3
L3	.003	.007	0.08	0.18	5
LH	.029	.042	0.74	1.07	
LL1	.032	.048	0.81	1.22	
LL2	.072	.088	1.83	2.23	
LS	.045	.055	1.14	1.39	
LW	.022	.028	0.56	0.71	
LW2	.006	.022	0.15	0.56	5

Pin no.	1	2	3	4
Transistor	Collector	Emitter	Base	N/C

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Dimension CH controls the overall package thickness. When a window lid is used, dimension CH must increase by a minimum of .010 inch (0.254 mm) and a maximum of .040 inch (1.020 mm).
4. The corner shape (square, notch, radius) may vary at the manufacturer's option, from that shown on the drawing.
5. Dimensions LW2 minimum and L3 minimum and the appropriate castellation length define an unobstructed three-dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on the bottom two layers, optional on the top ceramic layer.) Dimension LW2 maximum and L3 maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.
6. The co-planarity deviation of all terminal contact points, as defined by the device seating plane, shall not exceed .006 inch (0.15mm) for solder dipped leadless chip carriers.
7. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 2. Physical dimensions, surface mount (UA version).

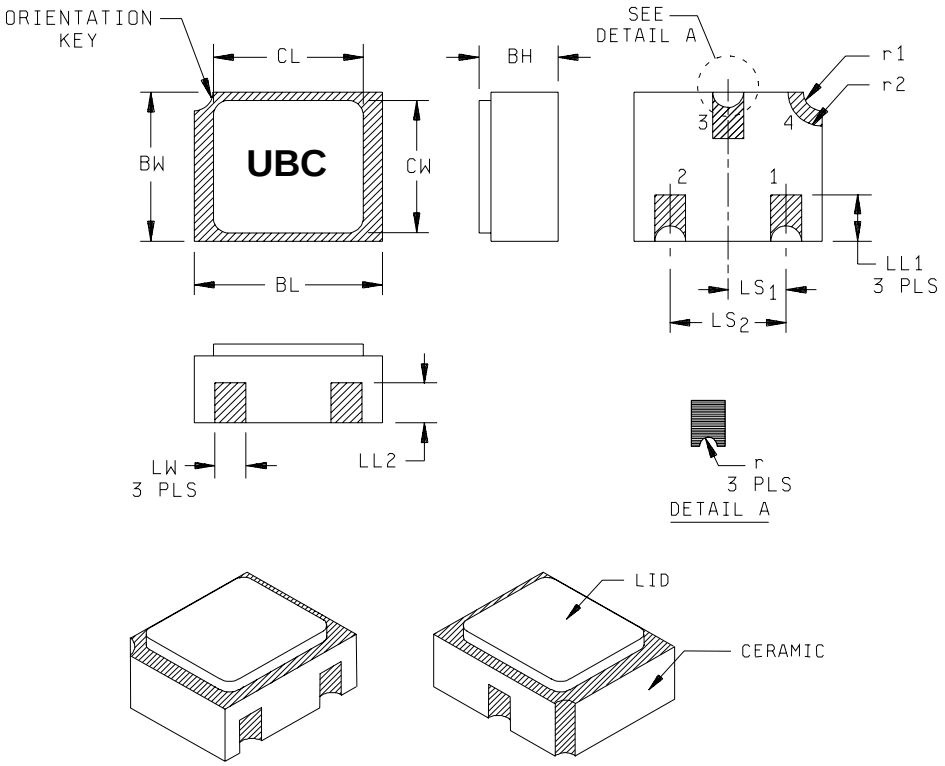


Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BH	.046	.056	1.17	1.42	
BL	.115	.128	2.92	3.25	
BW	.085	.108	2.16	2.74	
CL		.128		3.25	
CW		.108		2.74	
LL1	.022	.038	0.56	0.96	
LL2	.017	.035	0.43	0.89	

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
LS_1	.036	.040	0.91	1.02	
LS_2	.071	.079	1.81	2.01	
LW	.016	.024	0.41	0.61	
r		.008		.203	
r1		.012		.305	
r2		.022		.559	

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Hatched areas on package denote metallized areas
4. Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Pad 4 = Shielding connected to the lid.
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 3. Physical dimensions, surface mount (UB version).

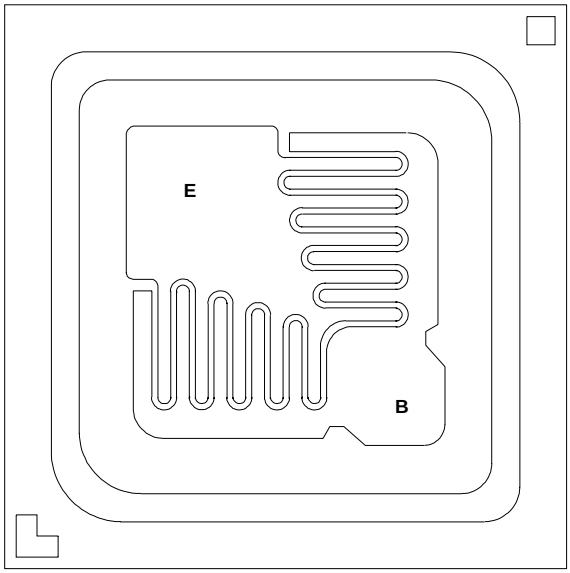


Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BH	.046	.056	1.17	1.42	
BL	.115	.128	2.92	3.25	
BW	.085	.108	2.16	2.74	
CL		.128		3.25	
CW		.108		2.74	
LL1	.022	.038	0.56	0.96	
LL2	.017	.035	0.43	0.89	

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
LS_1	.036	.040	0.91	1.02	
LS_2	.071	.079	1.81	2.01	
LW	.016	.024	0.41	0.61	
r		.008		.203	
r1		.012		.305	
r2		.022		.559	

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Hatched areas on package denote metallized areas
4. Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Pad 4 = connected to the lid braze ring.
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

* FIGURE 4. Physical dimensions, surface mount (UBC version, ceramic lid).

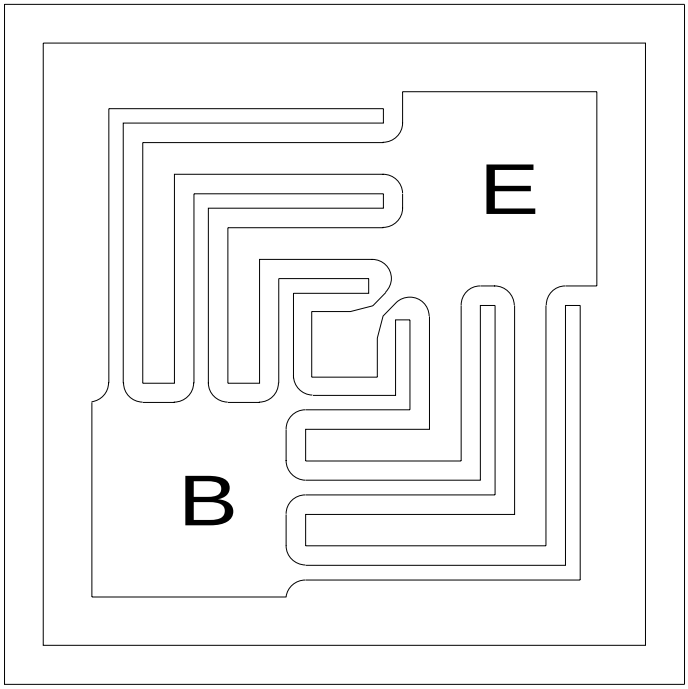


Physical characteristics:
B-version

NOTES:

1.	Chip size:	0.023 x 0.023 mils ±0.002 mils (0.584 mm x 0.584 mm ±0.051 mm).
2.	Chip thickness:	0.010 ±0.0015 mils (0.254 mm ±0.038 mm).
3.	Top metal:	Aluminum 15,000Å minimum, 18,000Å nominal for JANHC. AlSiCu 16,000Å minimum, 18,000Å nominal for JANKC.
4.	Back metal:	Gold 4,500Å minimum, 5,000Å nominal.
5.	Glassivation:	Si_3N_4 2,000 Å minimum, 8,000 Å nominal for JANHC. SiON 8,500 Å minimum, 9,000 Å nominal for JANKC
6.	Backside:	Collector.
7.	Bonding pad:	B = 0.0042 x 0.0042 mils (0.107 mm x 0.107 mm). E = 0.0042 x 0.0042 mils (0.107 mm x 0.107 mm).

* FIGURE 5. JANHC and JANKC (B-version) die dimensions.



NOTES:

1.	Die size:	.020 x .020 inch (0.508 mm x 0.508 mm).
2.	Die thickness:	.008 ±.0016 inch (0.2032 mm ±0.04064 mm).
3.	Base bonding pad:	.004 x .004 inch (0.1016 mm x 0.1016 mm).
4.	Emitter bonding pad:	.004 x .004 inch.
5.	Back metal:	Gold, 6,500 ±1,950 Å.
6.	Top metal:	Aluminum, 27,000 ±3,000 Å.
7.	Back side:	Collector.
8.	Glassivation:	SiO_2, 7,500 ±1,500 Å.

* FIGURE 6. JANHC and JANKC (C-version) die dimensions.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

* 3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows.

PCB ..... Printed circuit board.
$R_{\theta JA}$ ..... Thermal resistance junction to ambient.
$R_{\theta JC}$ ..... Thermal resistance junction to case.
$R_{\theta JSP(AM)}$ ..... Thermal resistance junction to solder pads (adhesive mount to PCB).
$R_{\theta JSP(IS)}$ ..... Thermal resistance junction to solder pads (infinite sink mount to PCB).
$T_{SP(AM)}$ ..... Temperature of solder pads (adhesive mount to PCB).
$T_{SP(IS)}$ ..... Temperature of solder pads (infinite sink mount to PCB).
UA, UB, and UBC .. Surface mount case outlines (see figures 2, 3, and 4).

* 3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figures 1, 2, 3, 4, 5, and 6 herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Radiation hardness assurance (RHA). Radiation hardness assurance requirements, PIN designators, and test levels shall be as defined in MIL-PRF-19500.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in paragraph 1.3, 1.4, and table I.

3.7 Electrical test requirements. The electrical test requirements shall be as specified in table I.

* 3.8 Marking. Marking shall be in accordance with MIL-PRF-19500, except for the UB suffix package. Marking on the UB package shall consist of an abbreviated part number, the date code, and the manufacturer's symbol or logo. The prefixes JAN, JANTX, JANTXV, JANJ, and JANS can be abbreviated as J, JX, JV, JJ, and JS respectively. The "2N" prefix and the "AUB" suffix can also be omitted. The radiation hardened designator M, D, P, L, R, F, G, or H shall immediately precede (or replace) the device "2N" identifier (depending upon degree of abbreviation required).

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4, and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 JANJ devices. For JANJ level, 3.3.1 through 3.3.1.3 of MIL-PRF-19500 shall apply, except as modified herein. Supplier imposed requirements as well as alternate screens, procedures, and controls shall be documented in the QM plan and must be submitted to the qualifying activity for approval. When alternate screens, procedures, and controls are used in lieu of the JANJ screens herein, equivalency shall be proven and documented in the QM plan. Radiation characterization may be submitted in the QM plan at the option of the manufacturer, however, 3.3.1.1 of MIL-PRF-19500 is not required. Die lot controls and rework requirements shall be in accordance with 3.13 and D.3.13.2.1 of MIL-PRF-19500 as required for the JANS level. Lot formation and conformance inspection requirements for JANJ shall be those used for JANS devices.

4.2.2 JANJ qualification. For JANJ qualification, 4.4.2.2 herein shall be performed as required by the qualifying activity. A JANS certified supplier may supply JANJ product utilizing the JANJ screening flow in 4.3 herein.

4.2.3 JANHC and JANKC qualification. JANHC and JANKC qualification inspection shall be in accordance with MIL-PRF-19500.

4.2.4 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.3 Screening (JANS, JANJ, JANTX, and JANTXV levels only). Screening shall be in accordance with table E-IV MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500)	Measurement		
	JANS level	JANJ level	JANTX and JANTXV levels
2	Optional	Optional	Optional
3a 3b (1) 3c	Required Not applicable Thermal impedance (transient), method 3131 of MIL-STD-750. (2) (see 4.3.3)	Required Not applicable Thermal impedance (transient), method 3131 of MIL-STD-750. (2) (see 4.3.3)	Required Not applicable Thermal impedance (transient), method 3131 of MIL-STD-750. (2) (see 4.3.3)
4	Required	Optional	Optional
5	Required	Required	Not applicable
8	Required	Not required	Not required
9	I_{CBO2}, h_{FE4}	I_{CBO2}, h_{FE4}	Not applicable
10	48 hours minimum	48 hours minimum	48 hours minimum
11	I_{CBO2}; h_{FE4}; ΔI_{CBO2} = 100 percent of initial value or 5 nA dc, whichever is greater. Δh_{FE4} = ±15 percent	I_{CBO2}; h_{FE4}; ΔI_{CBO2} = 100 percent of initial value or 5 nA dc, whichever is greater. Δh_{FE4} = ±15 percent	I_{CBO2}; h_{FE4}
12	See 4.3.2	See 4.3.2	See 4.3.2
13	Subgroups 2 and 3 of table I herein; ΔI_{CBO2} = 100 percent of initial value or 5 nA dc, whichever is greater; Δh_{FE4} = ±15 percent	Subgroups 2 and 3 of table I herein; ΔI_{CBO2} = 100 percent of initial value or 5 nA dc, whichever is greater; Δh_{FE4} = ±15 percent	Subgroup 2 of table I herein; ΔI_{CBO2} = 100 percent of initial value or 5 nA dc, whichever is greater; Δh_{FE4} = ±15 percent
15	Required	Required	Not required
16	Required	Required	Not required

(1) Shall be performed anytime after temperature cycling, screen 3a; and does not need to be repeated in screening requirements.
(2) Thermal impedance limits shall not exceed figures 12, 13, 14, 15, and 16.

4.3.1 Screening (JANHC and JANKC). Screening of JANHC and JANKC die shall be in accordance with MIL-PRF-19500 "Discrete Semiconductor Die/Chip Lot Acceptance". Burn-in duration for the JANKC level follows JANS requirements; the JANHC follows JANTX requirements.

* 4.3.2 Power burn-in conditions. Power burn-in conditions are as follows: V_{CB} = 10 - 30 V dc. Power shall be applied to achieve T_J = +135°C minimum using a minimum P_D = 75 percent of P_T maximum, T_A ambient rated as defined in 1.3, = T_A = 35°C. With approval of the qualifying activity and preparing activity, alternate burn-in criteria (hours, bias conditions, T_J, and mounting conditions) may be used for JANTX and JANTXV quality levels. A justification demonstrating equivalence is required. In addition, the manufacturing site's burn-in data and performance history will be essential criteria for burn-in modification approval. Method 3100 of MIL-STD-750 to measure T_J shall be used.

* 4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{MD} (and V_C where appropriate). The thermal impedance limit shall comply with the thermal impedance graph on figures 12, 13, 14, 15, and 16 (less than or equal to the curve value at the same t_H time) and shall be less than the process determined statistical maximum limit as outlined in method 3131 of MIL-STD-750. See table III, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein. If alternate screening is being performed in accordance with MIL-PRF-19500, a sample of screened devices shall be submitted to and pass the requirements of subgroups 1 and 2, of table I herein, inspection only (table E-VIb, group B, subgroup 1 is not required to be performed since solderability and resistance to solvents testing is performed in A1 herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500, and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-VIa (JANS and JANJ) of MIL-PRF-19500 and 4.4.2.1. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup 2 and 4.5.3 herein: delta requirements only apply to subgroups B4, and B5. See 4.4.2.2 for JAN, JANTX, and JANTXV group B testing. Electrical measurements (end-points) and delta requirements for JAN, JANTX, and JANTXV shall be after each step in 4.4.2.2 and shall be in accordance with table I, subgroup 2 and 4.5.3 herein.

4.4.2.1 Group B inspection (JANS and JANJ), table E-VIa of MIL-PRF-19500.

Subgroup	Method	Condition
B4	1037	V_{CB} = 10 V dc, adjust device current, or power, to achieve a minimum ΔT_J of +100°C.
B5	1027	V_{CB} = 10 V dc; $P_D \geq$ 100 percent of maximum rated P_T (see 1.3). (NOTE: If a failure occurs, resubmission shall be at the test conditions of the original sample.) Option 1: 96 hours minimum sample size in accordance with MIL-PRF-19500, table E-VIa, adjust T_A or P_D to achieve T_J = +275°C minimum. Option 2: 216 hours minimum, sample size = 45, c = 0; adjust T_A or P_D to achieve a T_J = +225°C minimum.

* 4.4.2.2 Group B inspection, (JAN, JANTX, and JANTXV). Separate samples may be used for each step. In the event of a lot failure, the resubmission requirements of MIL-PRF-19500 shall apply. In addition, all catastrophic failures during CI shall be analyzed to the extent possible to identify root cause and corrective action. Whenever a failure is identified as wafer lot or wafer processing related, the entire wafer lot and related devices assembled from the wafer lot shall be rejected unless an appropriate determined corrective action to eliminate the failures mode has been implemented and the devices from the wafer lot are screened to eliminate the failure mode.

Step	Method	Condition
1	1026	Steady-state life: 1,000 hours minimum, V_{CB} = 10 V dc, power shall be applied to achieve T_J = +150°C minimum using a minimum of P_D = 75 percent of maximum rated P_T as defined in 1.3. n = 45 devices, c = 0. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.
2	1048	Blocking life, T_A = +150°C, V_{CB} = 80 percent of rated voltage, 48 hours minimum. n = 45 devices, c = 0.
3	1032	High-temperature life (non-operating), t = 340 hours, T_A = +200°C. n = 22, c = 0.

* 4.4.2.3 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

a. For JAN, JANTX, and JANTXV samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot. For JANS and JANJ, samples shall be selected from each inspection lot. See MIL-PRF-19500.

b. Shall be chosen from an inspection lot that has been submitted to and passed table I, subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (subgroups B4 and B5 for JANS and JANJ, and group B for JAN, JANTX, and JANTXV) may be pulled prior to the application of final lead finish.

4.4.3 Group C inspection, Group C inspection shall be conducted in accordance with the test and conditions specified for subgroup testing in table E-VII of MIL-PRF-19500, and in 4.4.3.1 (JANS and JANJ) and 4.4.3.2 (JAN, JANTX, and JANTXV) herein for group C testing. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup 2 and 4.5.3 herein; delta requirements only apply to subgroup C6.

* 4.4.3.1 Group C inspection (JANS and JANJ), table E-VII of MIL-PRF-19500.

Subgroup	Method	Condition
C2	2036	Test condition E; (not applicable for UA, UB, and UBC devices).
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see 1.3) and in accordance with thermal impedance curves.
C6	1026	1,000 hours at V_{CB} = 10 V dc; power shall be applied to achieve T_J = +150°C minimum and a minimum of P_D = 75 percent of maximum rated P_T as defined in 1.3 n = 45, c = 0. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.

* 4.4.3.2 Group C inspection (JAN, JANTX, and JANTXV), table E-VII of MIL-PRF-19500.

Subgroup	Method	Condition
C2	2036	Test condition E; not applicable for UA, UB, and UBC devices.
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see 1.3 and 4.3.3) and in accordance with thermal impedance curves.
C6		Not applicable.

4.4.3.3 Group C sample selection. Samples for subgroups in group C shall be chosen at random from any inspection lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes table I tests herein for conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for C6 life test may be pulled prior to the application of final lead finish. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

4.4.4 Group D inspection. Conformance inspection for hardness assured JANS, JANJ, and JANTXV types shall include the group D tests specified in table II herein. These tests shall be performed as required in accordance with MIL-PRF-19500 and method 1019 of MIL-STD-750, for total ionizing dose or method 1017 of MIL-STD-750 for neutron fluence as applicable (see 6.2 herein), except group D, subgroup 2 may be performed separate from other subgroups.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table III herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein; delta measurements shall be in accordance with the applicable steps of 4.5.3.

4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Input capacitance. This test shall be conducted in accordance with method 3240 of MIL-STD-750, except the output capacitor shall be omitted.

4.5.3 Delta requirements. Delta requirements shall be as specified below:

Step	Inspection	MIL-STD-750		Symbol	Limit	Unit
		Method	Conditions			
1	Collector-base cutoff current	3036	Bias condition D, V_{CB} = 60 V dc	ΔI_{CB02} (1)	100 percent of initial value or 8 nA dc, whichever is greater.	
2	Forward current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 150 mA dc; pulsed, see 4.5.1	Δh_{FE4} (1)	±25 percent change from initial reading.	

(1) Devices which exceed the table I limits herein for this test shall not be accepted.

* TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 1 2/						
Visual and mechanical examination 3/	2071	n = 45 devices, c = 0				
Solderability 3/ 4/	2026	n = 15 leads, c = 0				
Resistance to solvents 3/ 4/ 5/	1022	n = 15 devices, c = 0				
Temp cycling 3/ 4/	1051	Test condition C, 25 cycles. n = 22 devices, c = 0				
Hermetic seal 4/ 6/ Fine leak Gross leak	1071	n = 22 devices, c = 0				
Electrical measurements 4/		Table I, subgroup 2				
Bond strength 3/ 4/	2037	Precondition T_A = +250°C at t = 24 hours or T_A = +300°C at t = 2 hours n = 11 wires, c = 0				
Decap internal visual (design verification) 4/	2075	n = 4 devices, c = 0				
Subgroup 2						
Thermal impedance	3131	See 4.3.3	$Z_{\theta JX}$			°C/W
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 75 V dc	I_{CBO1}		10	µA dc
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 6 V dc	I_{EBO1}		10	µA dc
Breakdown voltage, collector to emitter	3011	Bias condition D; I_C = 10 mA dc; pulsed (see 4.5.1)	$V_{(BR)CEO}$	50		V dc
Collector to emitter cutoff current	3041	Bias condition C; V_{CE} = 50 V dc	I_{CES}		50	nA dc
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 60 V dc	I_{CBO2}		10	nA dc
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 4 V dc	I_{EBO2}		10	nA dc
Forward-current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 0.1 mA dc	h_{FE1}			
2N2221A, AL, UA, UB, UBC				30		
2N2222A, AL, UA, UB, UBC				50		

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - Continued						
Forward-current transfer ratio 2N2221A, AL, UA, UB, UBC 2N2222A, AL, UA, UB, UBC	3076	V_{CE} = 10 V dc; I_C = 1.0 mA dc	h_{FE2}	 35 75	 150 325	
Forward-current transfer ratio 2N2221A, AL, UA, UB, UBC 2N2222A, AL, UA, UB, UBC	3076	V_{CE} = 10 V dc; I_C = 10 mA dc	h_{FE3}	 40 100		
Forward-current transfer ratio 2N2221A, AL, UA, UB, UBC 2N2222A, AL, UA, UB, UBC	3076	V_{CE} = 10 V dc; I_C = 150 mA dc; pulsed (see 4.5.1)	h_{FE4}	 40 100	 120 300	
Forward-current transfer ratio 2N2221A, AL, UA, UB, UBC 2N2222A, AL, UA, UB, UBC	3076	V_{CE} = 10 V dc; I_C = 500 mA dc; pulsed (see 4.5.1)	h_{FE5}	 20 30		
Collector-emitter saturation voltage	3071	I_C = 150 mA dc; I_B = 15 mA dc; pulsed (see 4.5.1)	$V_{CE(sat)1}$		0.3	V dc
Collector-emitter saturation voltage	3071	I_C = 500 mA dc; I_B = 50 mA dc; pulsed (see 4.5.1)	$V_{CE(sat)2}$		1.0	V dc
Base-emitter saturation voltage	3066	Test condition A; I_C = 150 mA dc; I_B = 15 mA dc; pulsed (see 4.5.1)	$V_{BE(sat)1}$	0.6	1.2	V dc
Base-emitter saturation voltage	3066	Test condition A; I_C = 500 mA dc; I_B = 50 mA dc; pulsed (see 4.5.1)	$V_{BE(sat)2}$		2.0	V dc
Subgroup 3						
High temperature operation		T_A = +150°C				
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 60 V dc	I_{CBO3}		10	μA dc
Low temperature operation		T_A = -55°C				
Forward-current transfer ratio 2N2221A, AL, UA, UB, UBC 2N2222A, AL, UA, UB, UBC	3076	V_{CE} = 10 V dc; I_C = 10 mA dc	h_{FE6}	 15 35		
Subgroup 4						
Small-signal short-circuit forward current transfer ratio 2N2221A, AL, UA, UB, UBC 2N2222A, AL, UA, UB, UBC	3206	V_{CE} = 10 V dc; I_C = 1 mA dc; f = 1 kHz	h_{fe}	 30 50		

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 4 - Continued						
Magnitude of small-signal short- circuit forward current transfer ratio	3306	V_{CE} = 20 V dc; I_C = 20 mA dc; f = 100 MHz	$\|h_{fe}\|$	2.5		
Open circuit output capacitance	3236	V_{CB} = 10 V dc; I_E = 0; 100 kHz ≤ f ≤ 1 MHz	C_{obo}		8	pF
Input capacitance (output open-circuited)	3240	V_{EB} = 0.5 V dc; I_C = 0; 100 kHz ≤ f ≤ 1 MHz	C_{ibo}		25	pF
Saturated turn-on time		(See figure 17)	t_{on}		35	ns
Saturated turn-off time		(See figure 18)	t_{off}		300	ns
Subgroups 5 and 6						
Not required						

1/ For sampling plan see MIL-PRF-19500.
2/ For resubmission of failed test in subgroup 1 of table I, double the sample size of the failed test or sequence of tests. A failure in table I, subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.
3/ Separate samples may be used.
4/ Not required for JANS devices.
5/ Not required for laser marked devices.
6/ This hermetic seal test is an end-point to temp-cycling in addition to electrical measurements.

* TABLE II. Group D inspection.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 1 4/						
Neutron irradiation	1017	Neutron exposure V_{CES} = 0V				
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 60 V dc	I_{CBO1}		20	nA dc
Forward-current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 0.1 mA dc	[h_{FE1}] 5/			
M through H2N2221A M through H2N2222A				[15] [25]		
Forward-current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 1.0 mA dc	[h_{FE2}] 5/			
M through H2N2221A M through H2N2222A				[17.5] [37.5]		
Forward-current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 10 mA dc	[h_{FE3}] 5/			
M through H2N2221A M through H2N2222A				[20] [50]		
Forward-current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 150 mA dc	[h_{FE4}] 5/			
M through H2N2221A M through H2N2222A				[20] [50]		
Forward-current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 500 mA dc	[h_{FE5}] 5/	27		
M through H2N2221A M through H2N2222A				[10] [15]		
Collector-emitter saturation voltage	3071	I_C = 150 mA dc; I_B = 15 mA dc	$V_{CE(sat)1}$		.35	V dc
Collector-emitter saturation voltage	3071	I_C = 500 mA dc; I_B = 50 mA dc	$V_{CE(sat)2}$		1.15	V dc

See footnotes at end of table.

* TABLE II. Group D inspection - Continued.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 2						
Total dose irradiation	1019	Gamma exposure V_{CES} = 40 V				
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 60 V dc	I_{CBO1}		20	nA dc
Forward-current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 0.1 mA dc	[h_{FE1}] 5/			
M through H2N2221A M through H2N2222A				[15] [25]		
Forward-current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 1.0 mA dc	[h_{FE2}] 5/			
M through H2N2221A M through H2N2222A				[17.5] [37.5]		
Forward-current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 10 mA dc	[h_{FE3}] 5/			
M through H2N2221A M through H2N2222A				[20] [50]		
Forward-current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 150 mA dc	[h_{FE4}] 5/			
M through H2N2221A M through H2N2222A				[20] [50]		
Forward-current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 500 mA dc	[h_{FE4}] 5/			
M through H2N2221A M through H2N2222A				[10] [15]		

See footnotes at end of table.

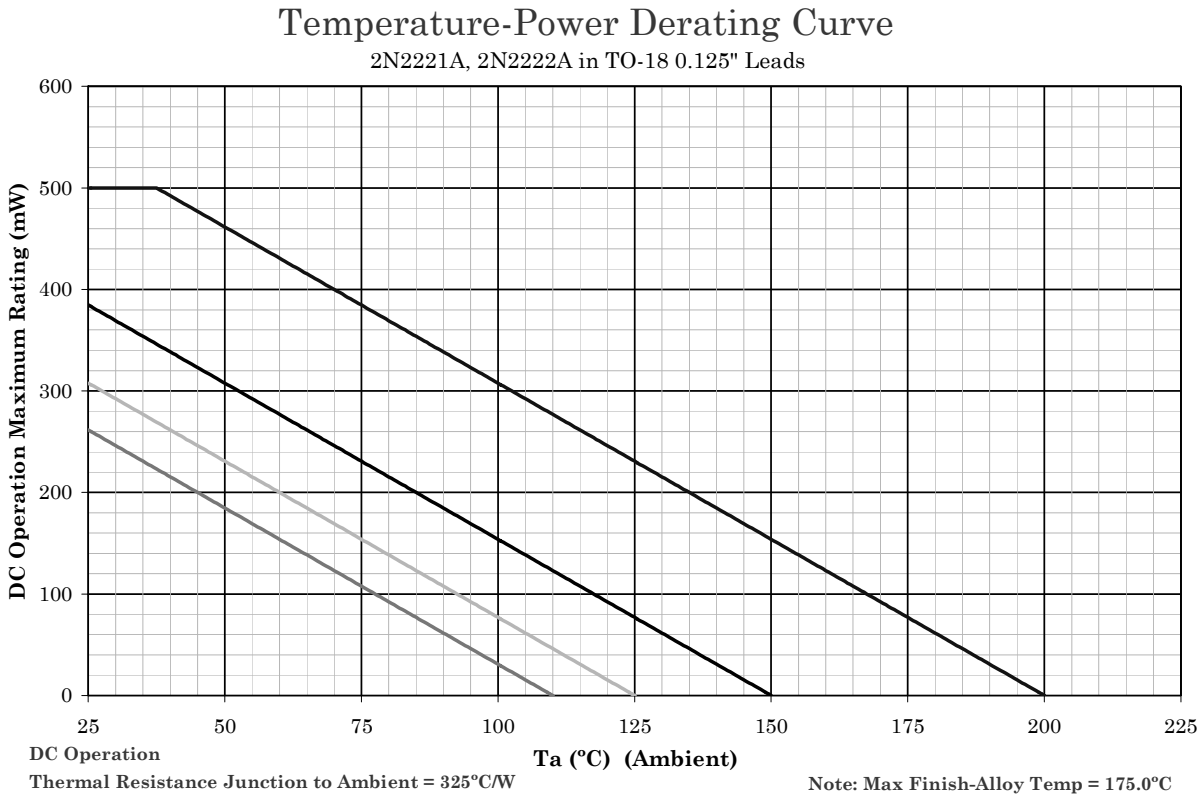
* TABLE II. Group D inspection - Continued.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - Continued						
Collector-emitter saturation voltage	3071	I_C = 150 mA dc; I_B = 15 mA dc;	$V_{CE(sat)1}$		.35	V dc
Collector-emitter saturation voltage	3071	I_C = 500 mA dc; I_B = 50 mA dc;	$V_{CE(sat)2}$		1.15	V dc

1/ Tests to be performed on all devices receiving radiation exposure.
2/ For sampling plan, see MIL-PRF-19500.
3/ Electrical characteristics apply to the corresponding AL, UA, UB, and UBC suffix versions unless otherwise noted.
4/ See 6.2.g herein.
5/ See method 1019 of MIL-STD-750 for how to determine [h_{FR}] by first calculating the delta ($1/h_{FE}$) from the pre- and Post-radiation h_{FE}. Notice the [h_{FE}] is not the same as h_{FE} and cannot be measured directly. The [h_{FE}] value can never exceed the pre-radiation minimum h_{FE} that it is based upon.

* TABLE III. Group E inspection (all quality levels) - for qualification or re-qualification only.

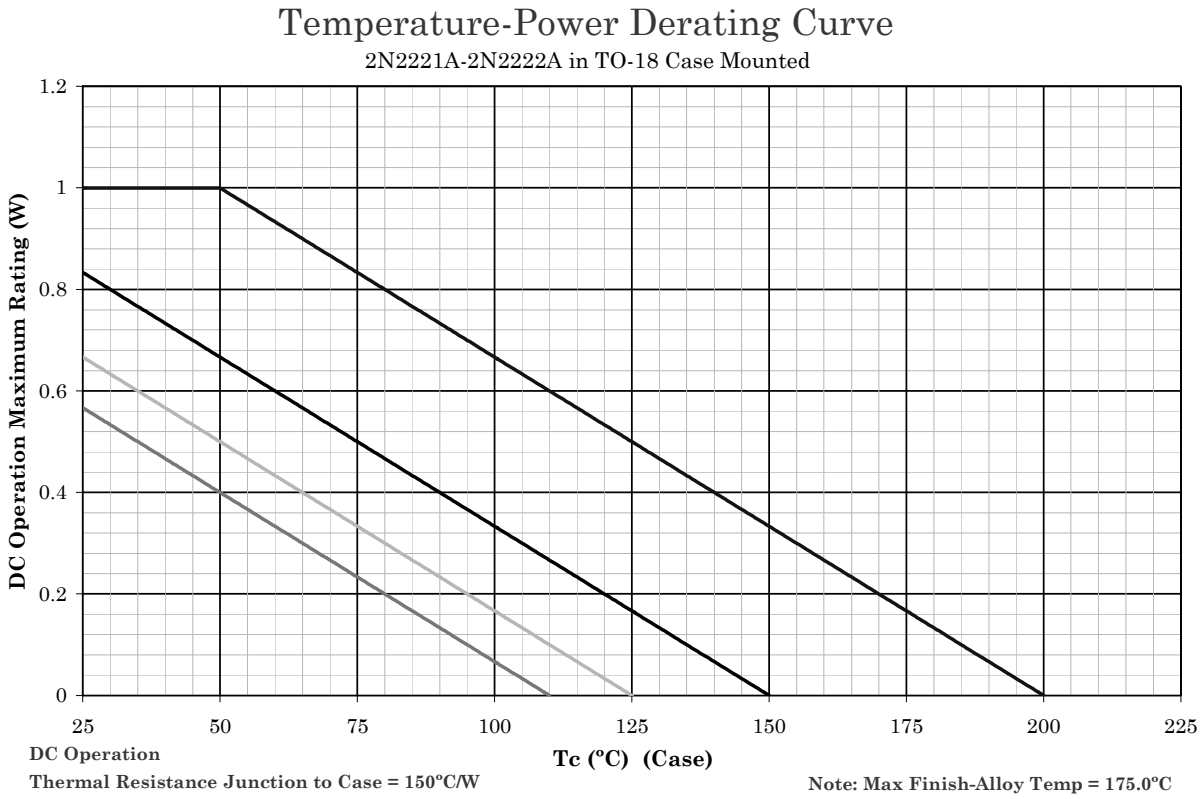
Inspection	MIL-STD-750		Qualification
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I, subgroup 2 and 4.5.3 herein.	
Subgroup 2			45 devices c = 0
Intermittent life	1037	Intermittent operation life: V_{CB} = 10 V dc, 6,000 cycles. Adjust device current, or power, to achieve a minimum ΔT_J of +100°C.	
Electrical measurements		See table I, subgroup 2 and 4.5.3 herein.	
Subgroup 4			
Thermal resistance	3131	$R_{\theta JSP(IS)}$ can be calculated but shall be measured once in the same package with a similar die size to confirm calculations (may apply to multiple specification sheets). $R_{\theta JSP(AM)}$ need be calculated only.	15 devices, c = 0
Thermal impedance curves		See MIL-PRF-19500	Sample size N/A
Subgroup 5			
Not applicable			
Subgroup 6			3 devices
Electrostatic discharge (ESD)	1020		
Subgroup 8			45 devices c = 0
Reverse stability	1033	Condition B	



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

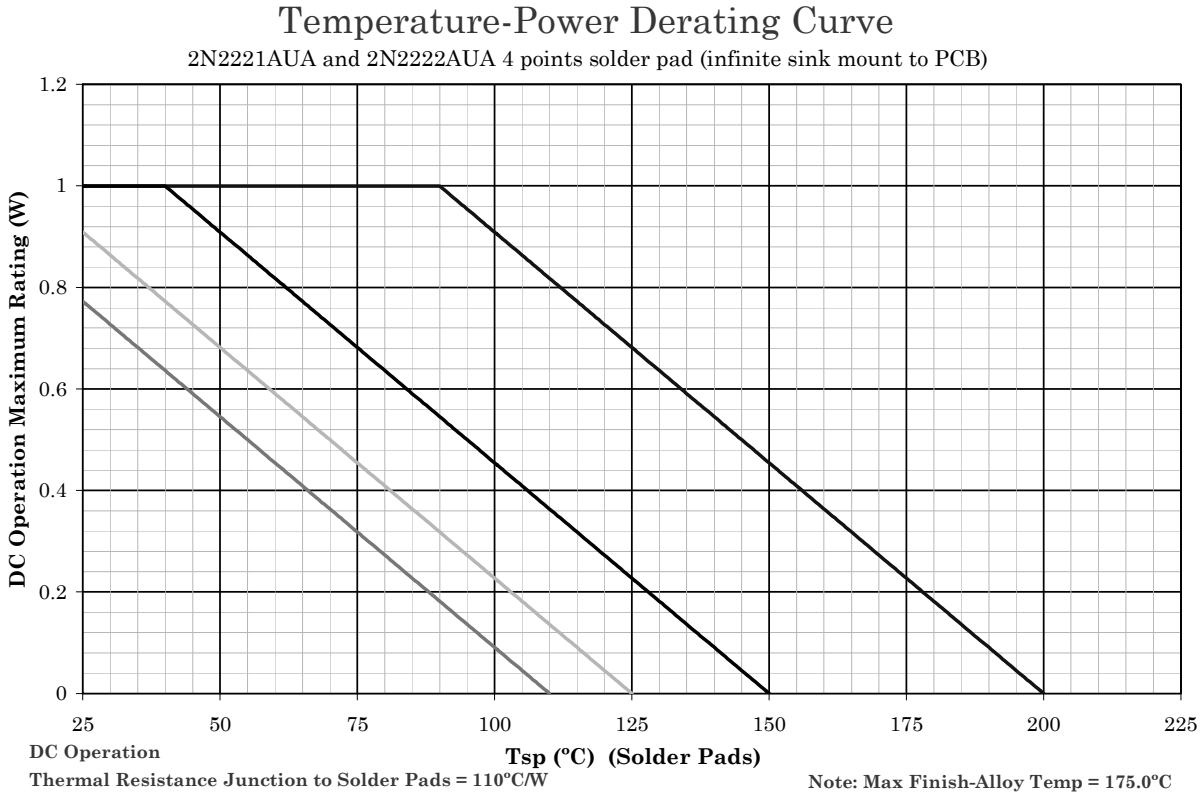
* FIGURE 7. Temperature-power derating for 2N2221A, 2N2221AL, 2N2222A, and 2N2222AL (TO-18 package).



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq +125°C$, and +110°C to show power rating where most users want to limit T_J in their application.

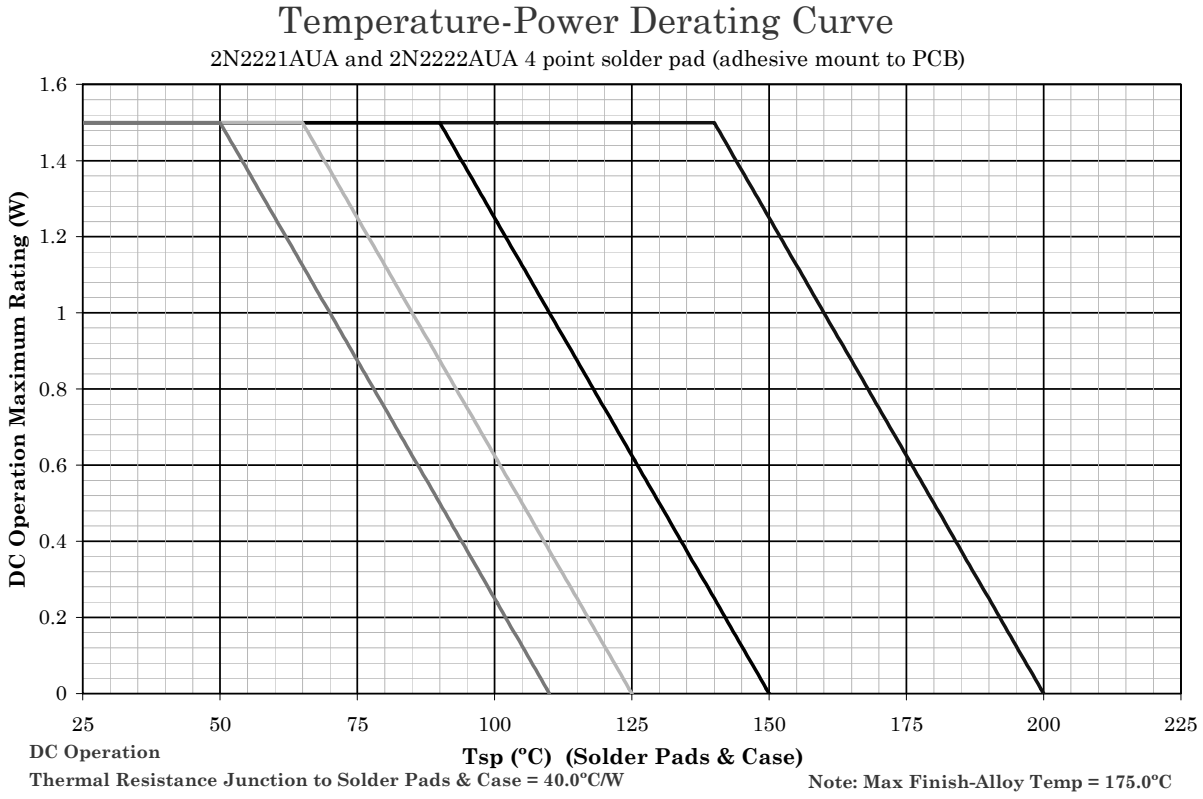
* FIGURE 8. Temperature-power derating for 2N2221A 2N2221AL, 2N2222A and 2N2222AL (TO-18 package case base mounted).



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq +125°C$, and +110°C to show power rating where most users want to limit T_J in their application.

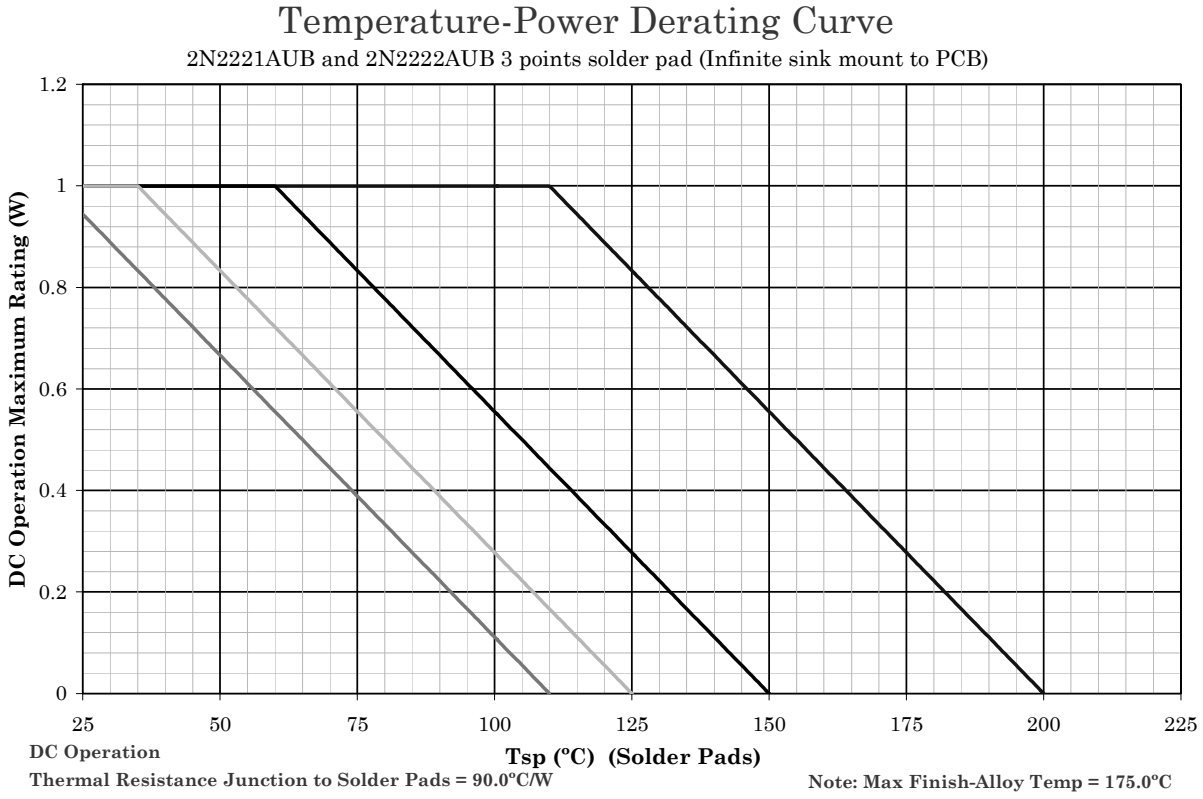
* FIGURE 9. Temperature-power derating for 2N2221AUA and 2N2222AUA.



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq +125°C$, and +110°C to show power rating where most users want to limit T_J in their application.

* FIGURE 10. Temperature-power derating for 2N2221AUA and 2N2222AUA.



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq +125°C$, and +110°C to show power rating where most users want to limit T_J in their application.

* FIGURE 11. Temperature-power derating curve for 2N2221AUB and 2N2222AUB.

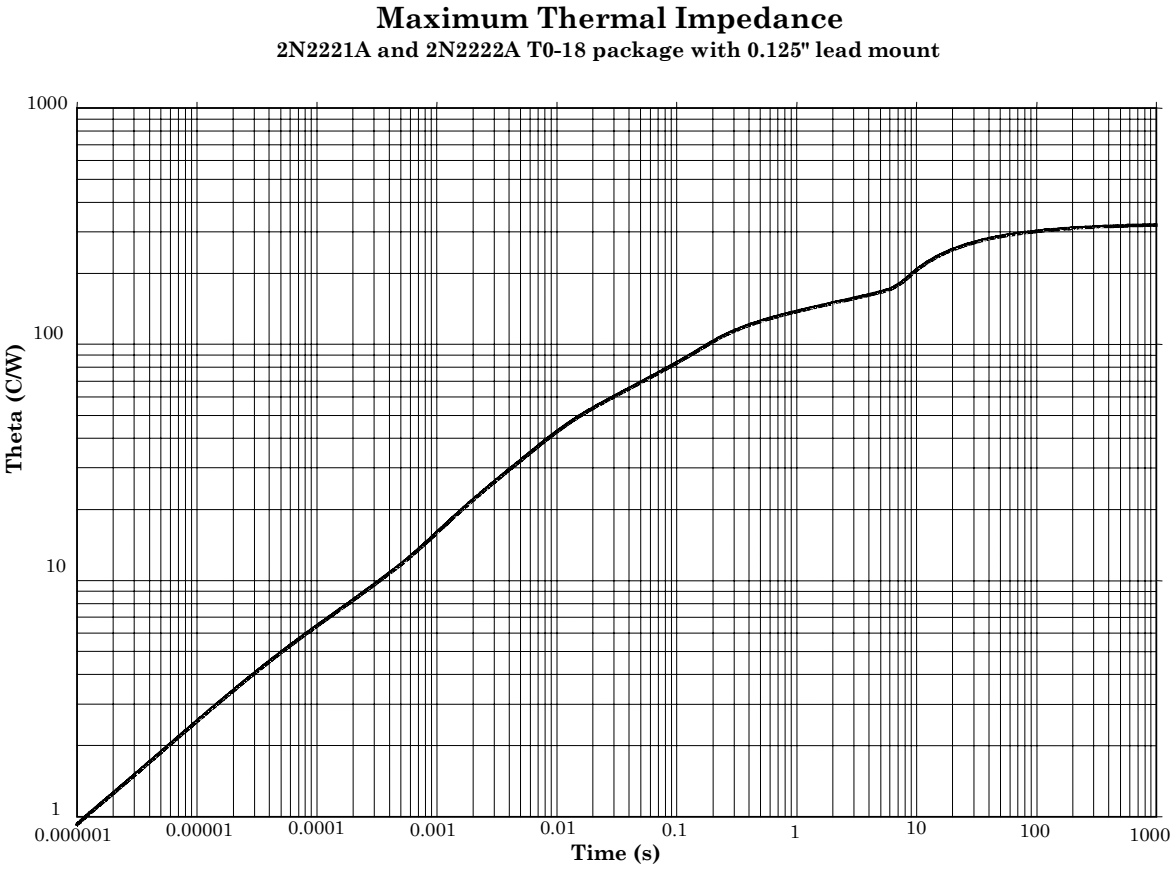


FIGURE 12. Thermal impedance graph ($R_{\theta JA}$) for 2N2221A, 2N2221AL, 2N2222A, and 2N2222AL (TO-18).

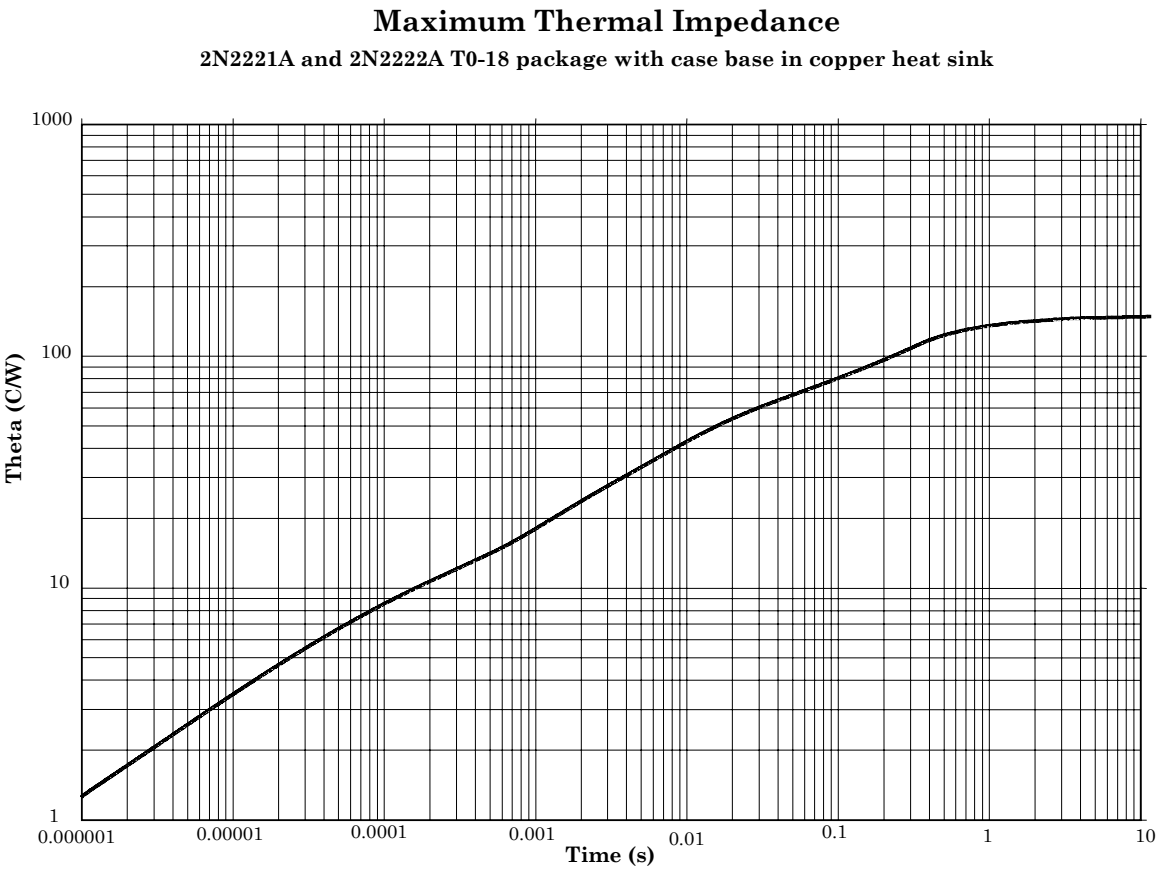


FIGURE 13. Thermal impedance graph ($R_{\theta JC}$) for 2N2221A, 2N2221AL, 2N2222A, and 2N2222AL (TO-18).

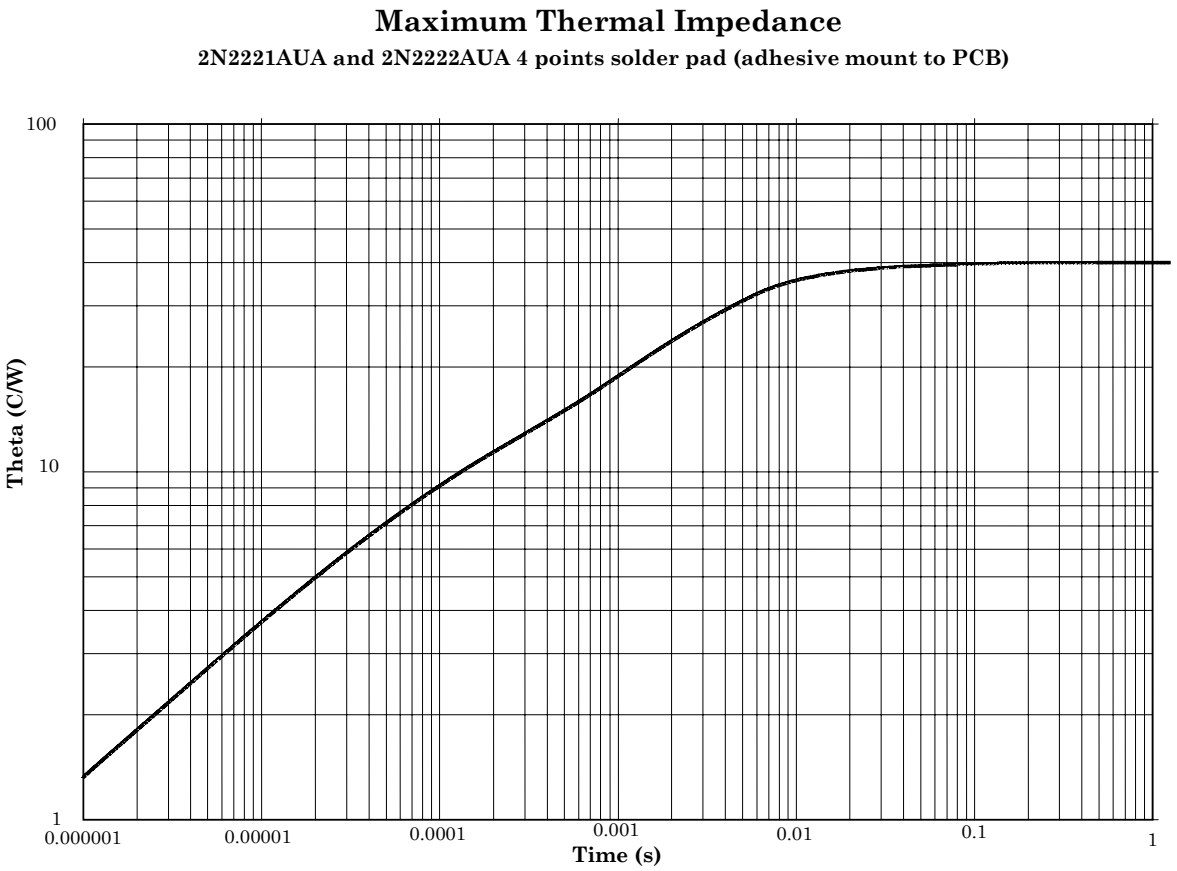


FIGURE 14. Thermal impedance graph ($R_{\theta JSP(AM)}$) for 2N2221AUA and 2N2222AUA.

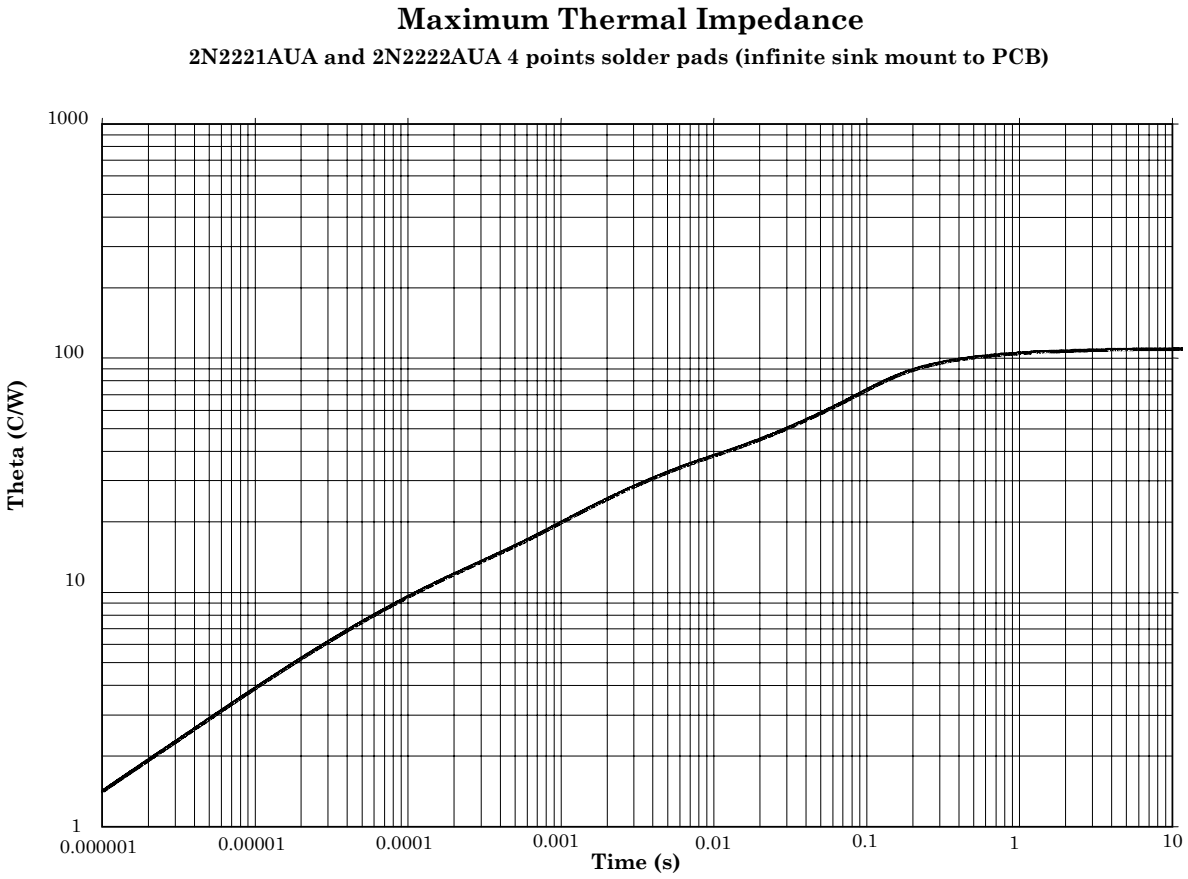


FIGURE 15. Thermal impedance graph ($R_{\theta JSP(IS)}$) for 2N2221AUA and 2N2222AUA.

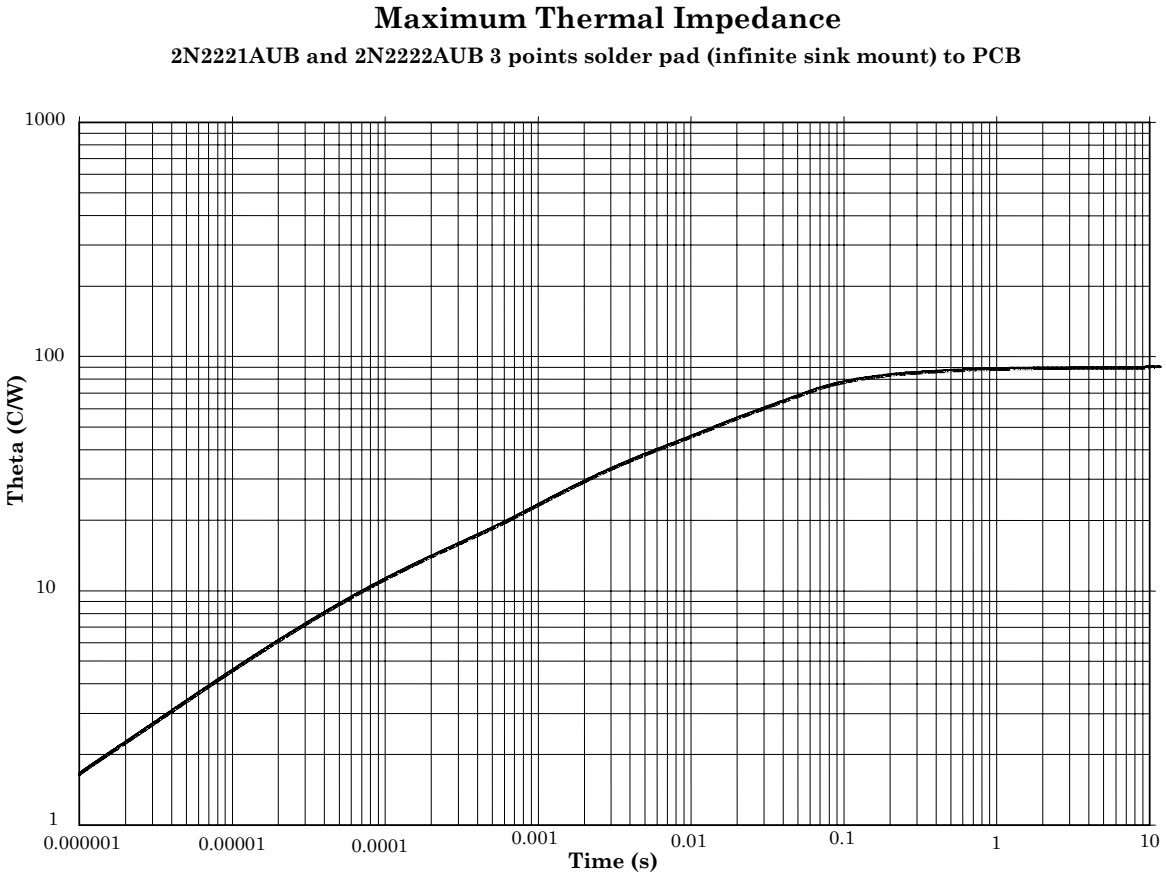
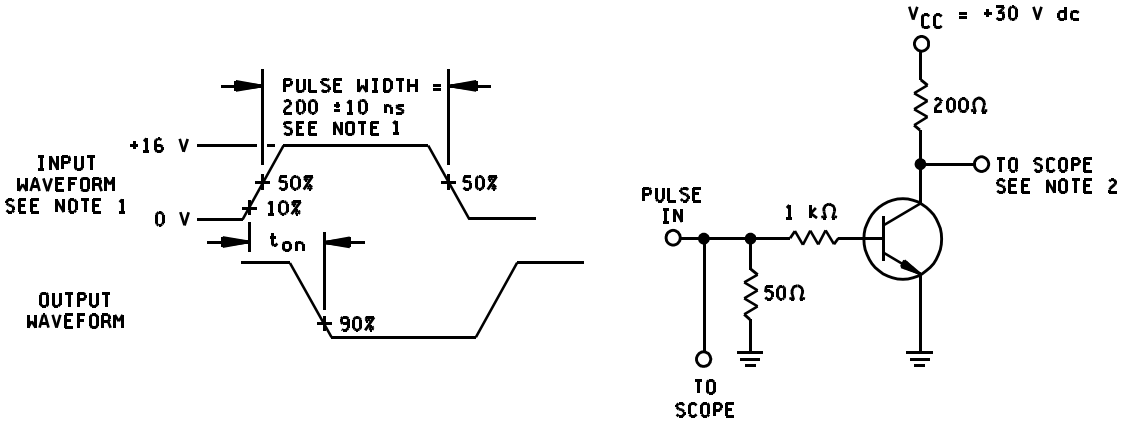


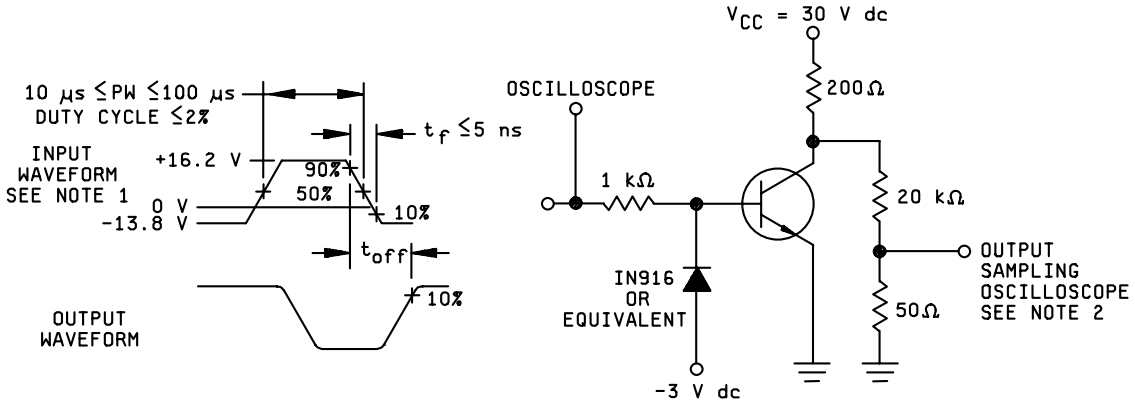
FIGURE 16. Thermal impedance graph ($R_{\theta JSP(IS)}$) for 2N2221AUB and 2N2222AUB.



NOTES:

1. The rise time (t_r) of the applied pulse shall be ≤ 2.0 ns, duty cycle ≤ 2 percent, and the generator source impedance shall be 50 Ω.
2. Sampling oscilloscope: $Z_{IN} \geq 100$ kΩ, $C_{IN} \leq 12$ pF, rise time ≤ 5 ns.

FIGURE 17. Saturated turn-on switching time test circuit.



NOTES:

1. The rise time (t_r) of the applied pulse shall be ≤ 2.0 ns, duty cycle ≤ 2 percent, and the generator source impedance shall be 50 Ω.
2. Sampling oscilloscope: $Z_{IN} \geq 100$ kΩ, $C_{IN} \leq 12$ pF, rise time ≤ 5 ns.

FIGURE 18. Saturated turn-off switching time test circuit.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

* (This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

* 6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

* 6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. Product assurance level and type designator.

e. For die acquisition, the JANHC or JANKC letter version shall be specified (see figures 5 and 6) as well as the RHA designer, if applicable. The JANHCA/JANKCA die version is obsolete as of the date of this revision. Other letter versions should be used.

f. Surface mount designation if applicable.

g. For acquisition of RHA designated devices, table II, subgroup 1 testing of group D herein is optional. If subgroup 1 is desired, it must be specified in the contract.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil.

6.4 Supersession data. Devices covered by this specification supersede the manufacturers' and users' Part or Identifying Number (PIN). The term PIN is equivalent to the term part number which was previously used in this specification. This information in no way implies that manufacturers' PIN's are suitable as a substitute for the military PIN.

6.5 Suppliers of JANHC and JANKC die. The qualified JANHC and JANKC suppliers with the applicable letter version (example JANHCB2N2221A) will be identified on the QML. The JANHCA/JANKCA die version is obsolete as of the date of this revision.

Die ordering information (1)		
PIN	Manufacturer	
	43611	34156
2N2221A 2N2222A	JANHCB2N2221A JANHCB2N2222A	JANHCC2N2221A JANHCC2N2222A

(1) For JANKC level, replace JANHC with JANKC.

6.6 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 11
NASA - NA
DLA - CC

Review activities:
Army - AR, MI, SM
Navy - AS, MC
Air Force - 19, 71, 99

Preparing activity:
DLA - CC

(Project 5961-2007-036)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http://assist.daps.dla.mil .