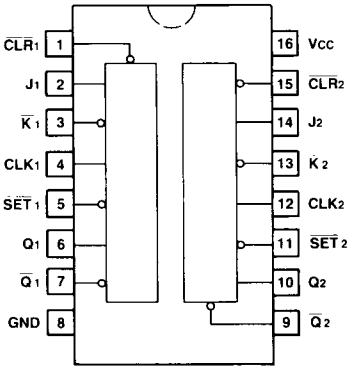
Dual J-$\overline{K}$ Positive-Edge-Triggered Flip-Flop

The LS109 is a bipolar, NPN, sealed-junction, silicon integrated circuit. It is manufactured in low-power Schottky technology and is available in a wire-bonded, 16-pin plastic DIP or surface mount package.



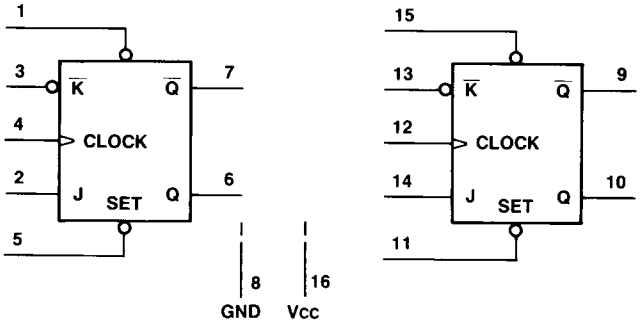
Truth Table

Inputs					Outputs	
Set	Clear	Clock	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q	$\overline{Q}_0$

* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level

H = High level (steady state)
L = Low level (steady state)
↑ = Transition from low to high level
X = Irrelevant (any input, including transitions)
Q_0 = Level of Q before the indicated steady-state input conditions were established
$\overline{Q}_0$ = Complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established
TOGGLE = Each output changes to the complement of its previous level on each active transition indicated by ↑

Logic Diagram



Electrical Characteristics

V_{CC} = 5.0 ±0.5 V, T_A = −55 to +125°C (WA-LS)
V_{CC} = 5.0 ±0.25 V, T_A = 0 to 70°C (WP90224L13)
V_{CC} = 5.0 ±0.5 V, T_A = −40 to +85°C (WA-LSD, WP91398L4)

		WA-LS		WP, WA-LSD		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Units**
Output Voltage, V_{CC} = 4.5 V						
Low, I_{OL} = 4.0 mA	V_{OL}	—	0.4	—	0.4	V
I_{OL} = 8.0 mA	V_{OL}	—	0.5	—	0.5	V
High, I_{OH} = −0.4 mA	V_{OH}	2.5	—	2.7	—	V
Input Voltage, V_{CC} = 4.5 V						
Low	V_{IL}	—	0.7	—	0.8*	V
High	V_{IH}	2.0	7.5	2.0	5.5	V
Clamp, I_{IN} = −18.0 mA	V_{IK}	—	−1.5	—	−1.5	V
Input Current, V_{CC} = 5.5 V						
Low, V_{IL} = 0.4 V						
J, K	I_{IL}	—	−0.4	—	−0.4	mA
Clock, Set	I_{IL}	—	−0.8	—	−0.8	mA
Clear	I_{IL}	—	−1.6	—	−1.6	mA
High, V_{IH} = 2.7 V						
J, K	I_{IH}	—	20.0	—	20.0	µA
Clock, Set	I_{IH}	—	40.0	—	40.0	µA
Clear	I_{IH}	—	80.0	—	80.0	µA
@ V_I max, V_I = 7.0 V, V_I = 5.5 V (WP, WA-LSD)						
J, K	I_I	—	0.1	—	0.1	mA
Clock, Set (Set, V_I = 5.5 V, WA-LS)	I_I	—	0.2	—	0.2	mA
Clear (V_I = 5.5 V, WA-LS)	I_I	—	0.4	—	0.4	mA
Output Current, V_{CC} = 5.5 V						
Short-Circuit	I_{OS}	−20.0	−100.0	−20.0	−100.0	mA
Supply Current, V_{CC} = 5.5 V	I_{CC}	—	8.0	—	8.0	mA

* WA-LSD, WP91398L4: V_{IL} = 0.7 V

Timing Characteristics

V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF

		WA-LS		WP, WA-LSD		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Units**
Propagation Delay						
Clock-to-Output, Low-to-High	t_{PLH}	—	20.0	—	25	ns
High-to-Low	t_{PHL}	—	30.0	—	40	ns
Clear- or Set-to-Output, Low-to-High	t_{PLH}	—	18.0	—	25	ns
Clear- or Set-to-Output (Clock Low), High-to-Low	t_{PHL}	—	24.0	—	40	ns
Clear- or Set-to-Output (Clock High), High-to-Low	t_{PHL}	—	35.0	—	40	ns
Operating Conditions						
Clock, Clear, Set Pulse Width	$t_{W\varnothing H}$	25.0	—	25	—	ns
Setup Time, Low	t_{DSL}	20.0	—	25	—	ns
High	t_{DSH}	20.0	—	35	—	ns
Hold Time, Low	t_{DHL}	5.0	—	5	—	ns
High	t_{DHH}	5.0	—	5	—	ns
Maximum Clock Frequency	f_{max}	30.0	—	25	—	ns

Maximum Ratings

Power supply voltage (V_{CC}) . . . . . 7.0 V
Operating temperature (T_A) . . . . . WA-LS: −55 to +125°C
WP90224L13: 0 to 70°C
WA-LSD, WP91398L4: −40 to +85°C
Storage temperature (T_{stg}) . . . . . −65 to +150°C

Maximum ratings are defined as the limiting conditions that the user can apply to the device under all variations of circuit and environmental conditions. If any rating is exceeded, permanent damage to the device may result.

Bonding or soldering of the external leads of this device can be performed safely at temperatures up to 300°C.

Timing Diagrams

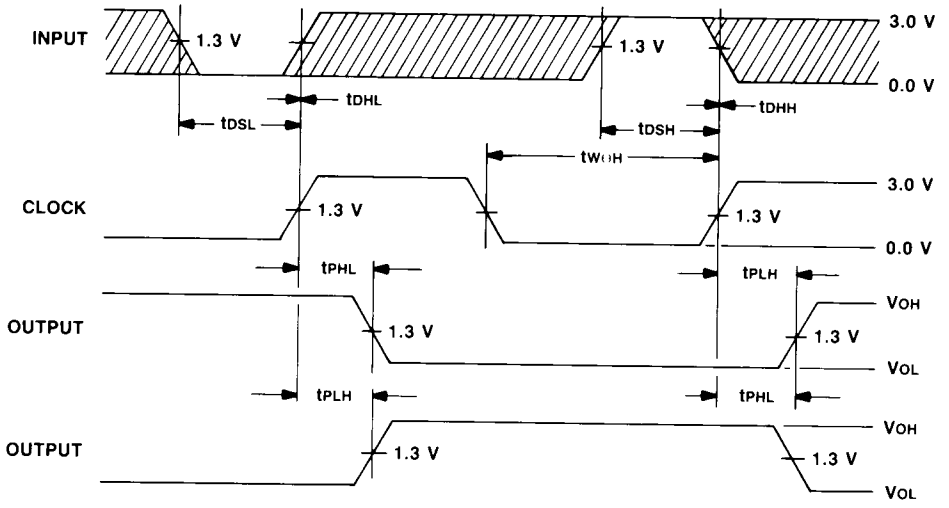


Figure 1. Clock to Output Delays, Data Set-Up and Hold Times, Clock Pulse Width (Note 1)

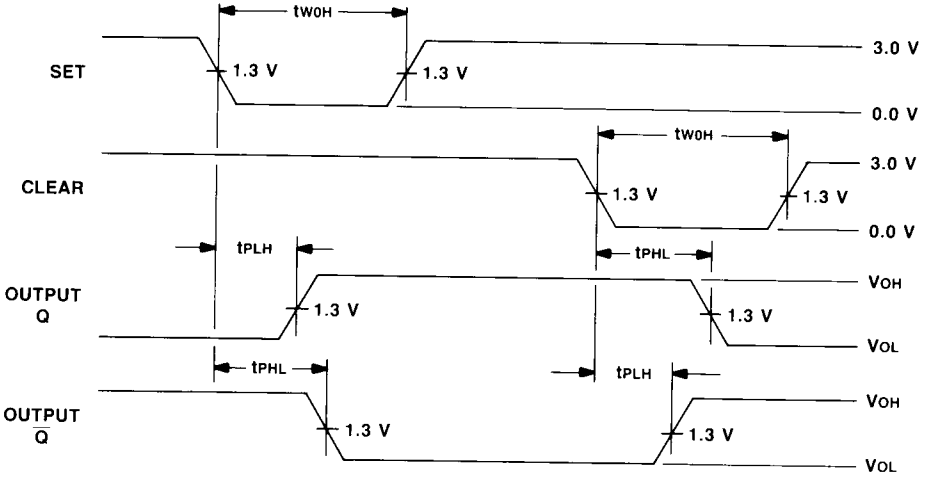


Figure 2. Set and Clear to Output Delays, Set and Clear Pulse Widths (Note 2)

Notes:

1. This waveform is for an output with internal conditions such that the output is low except when disabled by the output control.
2. This waveform is for an output with internal conditions such that the output is high except when disabled by the output control.