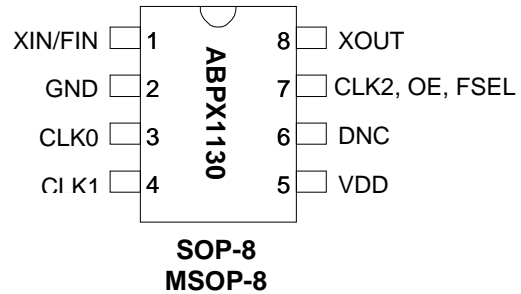


## Advanced Programmable Clock

### FEATURES

- Advanced programmable PLL design
- Very low Jitter and Phase Noise (< 40ps Pk-Pk typical)
- Output frequency up to 375MHz CMOS.
- Supports differential CMOS output to produce PECL, LVDS inputs.
- Crystal inputs:
  - Fundamental crystal: 10MHz-30MHz
  - 3<sup>RD</sup> overtone crystal: Up to 75MHz
  - Reference input: Up to 200MHz
- Accepts <1.0V reference signal input voltage
- One programmable I/O pin can be configured as Output Enable (OE), or Frequency Selection input (FSEL), or Reference clock.
- Single 3.3V ± 10% power supply
- Operating temperature range from -40°C to 85°C
- Available in 8-pin MSOP/SOIC, 6-pin SOT Green/RoHS compliant packages.

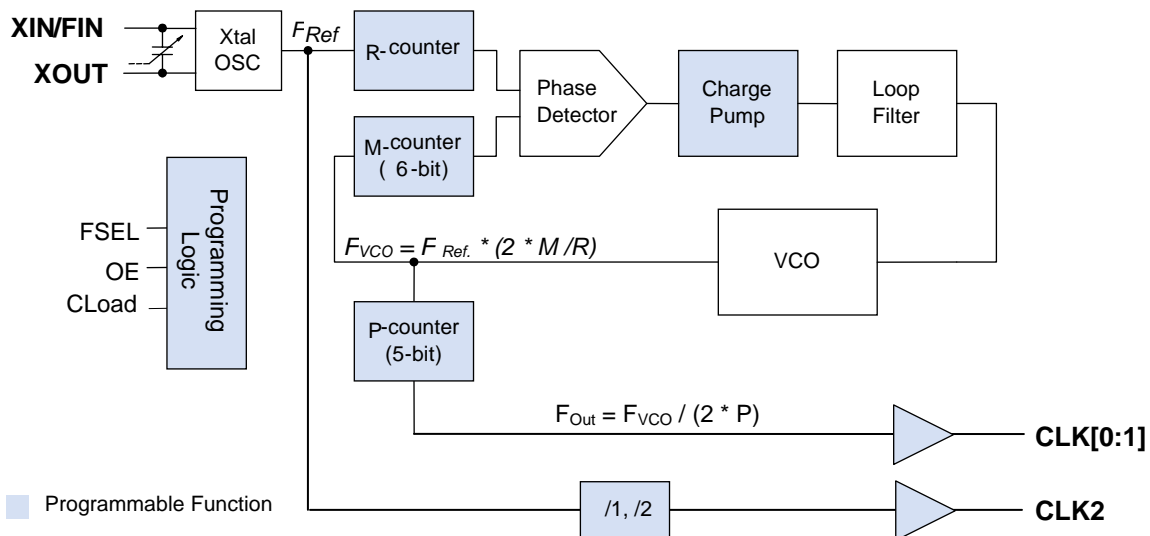
### PIN CONFIGURATION



### DESCRIPTION

The ABPX1130 is a low-cost general purpose frequency synthesizer and a member of Abracon's Advanced Programmable Clock family. Abracon's ABPX1130 product family can generate any output frequency up to 375 MHz from fundamental crystal input between 10 MHz - 30 MHz, or a 3rd overtone crystal of up to 75MHz. The ABPX1130 produces differential CMOS outputs to support PECL, LVDS, and CMOS inputs.

### BLOCK DIAGRAM



**Advanced Programmable Clock**
**KEY PROGRAMMING PARAMETERS**

CLK[ 0:2 ] Output Frequency	Output Drive Strength	Crystal Load	Programmable Input/Output (pin #7)	# of Register Banks	Charge-Pump Current
$F_{out} = FIN * M / (R * P)$ where M= 6 bit R= 1 P= 5 bit 1. CLK[0:1]= VCO / 2 * P 2. CLK[2]= FIN or FIN/2	Std: 10mA (default)  High: 24mA	+/- 200ppm tuning.	One output pin can be configured as 1. CLK2 = FIN or FIN/2 2. FSEL - input 3. OE - input	2	4 levels of pump current setting

**PIN DESCRIPTION**

Name	Pin #	Type	Description									
	(M)SOP-8											
XIN/FIN	1	I	Crystal or Reference input pin									
GND	2	P	GND connection									
CLK[0:1]	3,4	O	Programmable Clock Output [note:CLK0=~CLK1]									
VDD	5	P	VDD connection									
DNC	6	-	Do No Connect									
CLK2, OE, FSEL	7	B	This programmable I/O pin can be configured as CLK2 (FIN or FIN/2) output, or OE input, or Frequency Selection (FSEL) input pin. This pin has an internal 60KΩ pull up resistor. <table border="1" data-bbox="792 1285 1377 1503" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>State</th> <th>OE</th> <th>FSEL</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Tristate CLK[0:1]</td> <td>Select Bank '0' ROM</td> </tr> <tr> <td>1 (default)</td> <td>Normal mode</td> <td>Select Bank '1' ROM</td> </tr> </tbody> </table>	State	OE	FSEL	0	Tristate CLK[0:1]	Select Bank '0' ROM	1 (default)	Normal mode	Select Bank '1' ROM
State	OE	FSEL										
0	Tristate CLK[0:1]	Select Bank '0' ROM										
1 (default)	Normal mode	Select Bank '1' ROM										
XOUT	8	O	Crystal output pin									

**Advanced Programmable Clock**
**ELECTRICAL SPECIFICATIONS**
**ABSOLUTE MAXIMUM RATINGS**

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	$V_{DD}$	-0.5	4.6	V
Input Voltage Range	$V_I$	-0.5	$V_{DD}+0.5$	V
Output Voltage Range	$V_O$	-0.5	$V_{DD}+0.5$	V
Data Retention @ 85° C		10		Years
Soldering Temperature			260	°C
Storage Temperature	$T_S$	-65	150	°C
Ambient Operating Temperature		-40	+85	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

**AC SPECIFICATIONS**

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Input Frequency	Fundamental Crystal	10		30	MHz
	3 <sup>rd</sup> Overtone Crystal			75	MHz
Settling Time	At power-up (after VDD increases over 1.62V)			10	ms
VDD Sensitivity	Frequency vs. VDD +/-10%	-2		2	ppm
Output Rise Time	15pF Load, 10/90%VDD, Standard drive		2.5	3.5	ns
	15pF Load, 10/90%VDD, High drive		1.0	1.5	ns
Output Fall Time	15pF Load, 90/10%VDD, Standard drive		2.5	3.5	ns
	15pF Load, 90/10%VDD, High drive		1.0	1.5	ns
Duty Cycle	At VDD/2	45	50	55	%
Max. output skew between same frequency clocks	Equal loading (15 pF). Equal frequency & drive strength			500	ps
Period Jitter, peak-to-peak* (measured from 10,000 samples)	With capacitive decoupling between VDD and GND. Operating only one output.		40		ps

\* Note: Jitter performance depends on the programming parameters.

**Advanced Programmable Clock**
**DC SPECIFICATIONS**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic, with Loaded Outputs	$I_{DD}$	At 10MHz, load=15pF			15	mA
Operating Voltage	$V_{DD}$		2.25		3.63	V
Output Low Voltage	$V_{OL}$	$I_{OL} = +4\text{mA}$ (Standard drive)			0.4	V
Output High Voltage	$V_{OH}$	$I_{OH} = -4\text{mA}$ (Standard drive)	$V_{DD} - 0.4$			V
Output Current	$I_{OSD}$	$V_{OL} = 0.4\text{V}$ , $V_{OH} = 2.4\text{V}$ (Standard drive)		10		mA
	$I_{OHD}$	$V_{OL} = 0.4\text{V}$ , $V_{OH} = 2.4\text{V}$ (High Drive)		24		mA
Short-circuit Current	$I_S$			$\pm 50$		mA

**CRYSTAL SPECIFICATIONS**

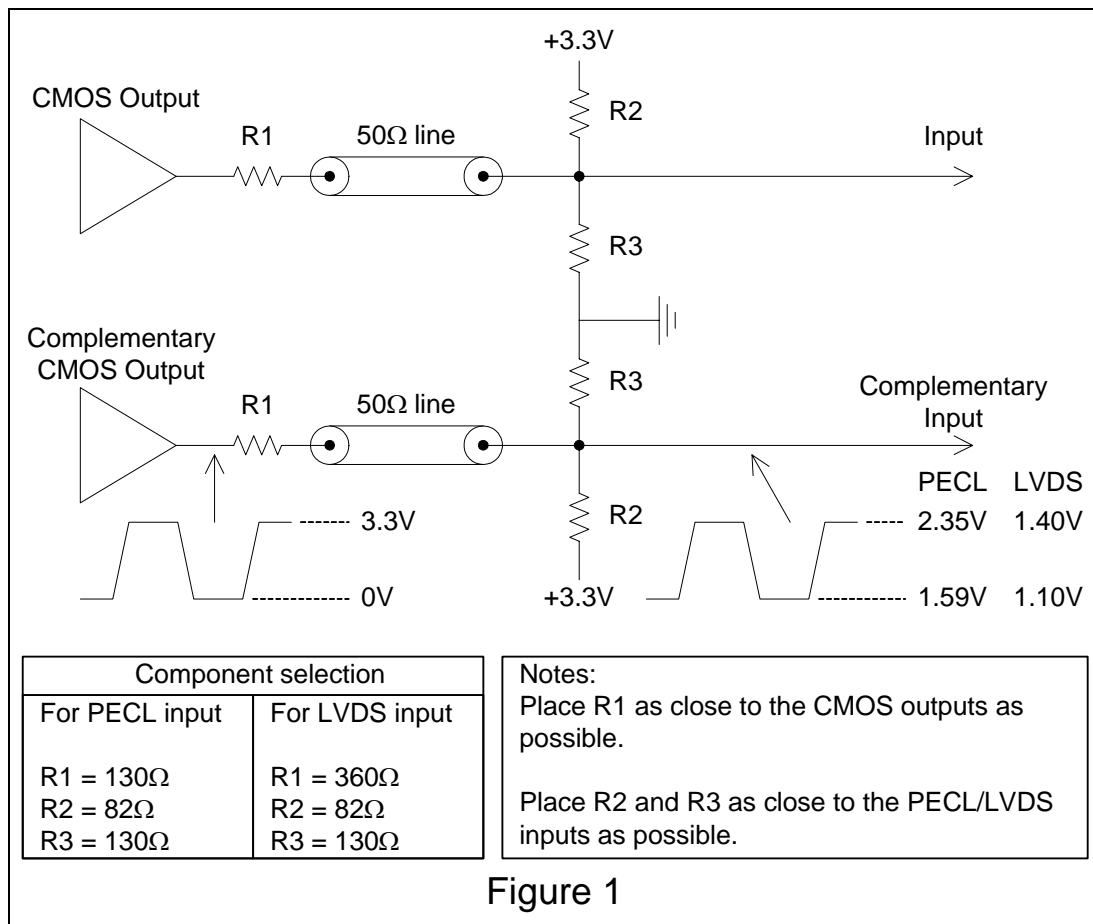
PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS
Fundamental Crystal Resonator Frequency	$F_{XIN}$	10		30	MHz
3 <sup>rd</sup> Overtone Crystal Resonator Frequency	$F_{XIN}$			75	MHz
Crystal Loading Rating (The IC can be programmed for any value in this range.)	$C_L$ (xtal)	5		20	pF
Maximum Sustainable Drive Level				500	$\mu\text{W}$
Operating Drive Level			100		$\mu\text{W}$
Crystal Shunt Capacitance	$C_0$			6	pF
Effective Series Resistance, Fundamental, 10-30MHz	$R_s$			30	$\Omega$
Effective Series Resistance, 3 <sup>rd</sup> Overtone, 30-50MHz [ $C_0 < 4\text{pF}$ , $C_L = 5\text{pF}/8\text{pF}$ ]	ESR			100/70	$\Omega$
Effective Series Resistance, 3 <sup>rd</sup> Overtone, 50-65MHz, [ $C_0 < 4\text{pF}$ , $C_L = 5\text{pF}/8\text{pF}$ ]	ESR			60/40	$\Omega$
Effective Series Resistance, 3 <sup>rd</sup> Overtone, 65-75MHz [ $C_0 < 4\text{pF}$ , $C_L = 5\text{pF}/8\text{pF}$ ]	ESR			45/30	$\Omega$

Note: A detailed crystal specification document is also available for this part

## Advanced Programmable Clock

Figure 1 below describes how to terminate the differential CMOS outputs of Abracon's ABPX1130 Programmable QTC clock for use with PECL or LVDS inputs.

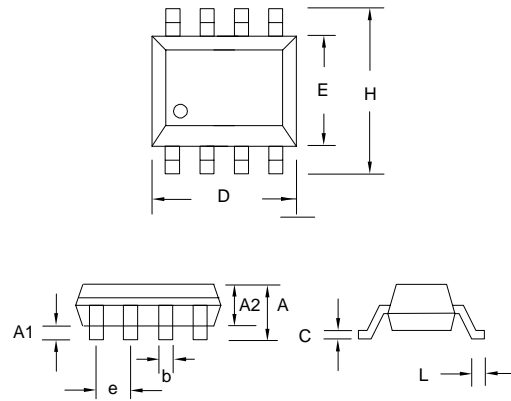
The unique feature of differential CMOS outputs allows great flexibility for board designers. By standardizing on one termination scheme you can use the ABPX1130 for all your LVDS and PECL clock requirements up to 375MHz.



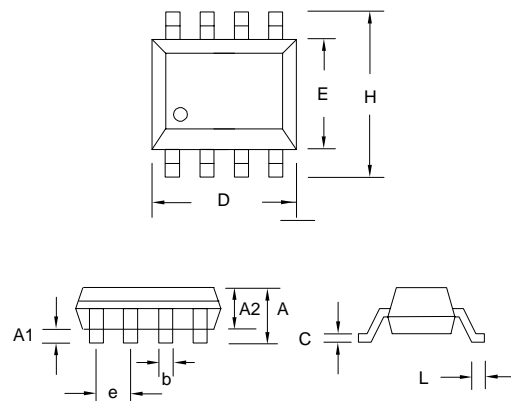
The above layout allows the ABPX1130 to drive either a PECL or LVDS input by simply changing the value of R1.

**Advanced Programmable Clock**
**PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)**
**MSOP 8L**

Symbol	Dimension in MM	
	Min.	Max.
A	---	1.10
A1	0.05	0.15
A2	0.81	0.91
B	0.25	0.40
C	0.13	0.23
D	2.90	3.10
E	2.90	3.10
H	4.90 BSC	
L	0.445	0.648
e	0.65 BSC	


**SOP 8L**

Symbol	Dimension in MM	
	Min.	Max.
A	1.35	1.75
A1	0.10	0.25
A2	1.25	1.50
B	0.33	0.53
C	0.19	0.27
D	4.80	5.00
E	3.80	4.00
H	5.80	6.20
L	0.40	0.89
e	1.27 BSC	



**Advanced Programmable Clock**

**ORDERING INFORMATION**

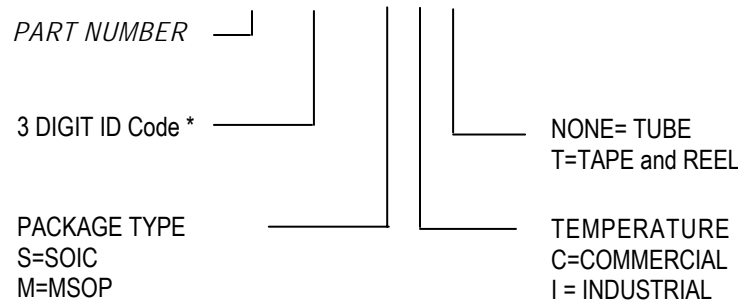
***For part ordering, please contact our Sales Department:***

30332 Esperanza., Rancho Santa Margarita, Ca 92688  
 Ph: 949-546-8000 Fax: 949-546-8001

***PART NUMBER***

The order number for this device is a combination of the following:  
 Device number, Package type and Operating temperature range

**APBX1130-XXX X X-I**



- \* PhaseLink will assign a unique 3-digit ID code for each approved programmed part number.
- \* PhaseLink offers Green Package Only for this product family.

Part / Order Number	Marking	Package Option
ABPX1130-XXXSC	A3XXX	8-Pin SOIC (Tube)
ABPX1130-XXXSC-T	A3XXX	8-Pin SOIC (Tape and Reel)
ABPX1130-XXXMC	A3XXX	8-Pin MSOP (Tube)
ABPX1130-XXXMC-T	A3XXX	8-Pin MSOP (Tape and Reel)

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