

M5M5408BFP/TP/RT

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5408B is a family of 4-Mbit static RAMs organized as 524,288-words by 8-bit, fabricated by Mitsubishi's high-performance 0.25 μ m CMOS technology.

The M5M5408B is suitable for memory applications where a simple interfacing, battery operating and battery backup are the important design objectives.

M5M5408B is packaged in 32-pin plastic SOP and 32-pin plastic TSOP packages. Two types of TSOPs are available, M5M5408BTP (normal-lead-bend TSOP) and M5M5408BRT (reverse-lead-bend TSOP). These two types TSOPs are suitable for a surface mounting on double-sided printed circuit boards.

From the point of operating temperature, the family is divided into three versions; "Standard", "W-version", and "I-version". Those are summarized in the part name table below.

FEATURES

- Single +5V power supply
- Small stand-by current: 0.4 μ A(3V,typ.)
- No clocks, No refresh
- Data retention supply voltage=2.0V to 5.5V
- All inputs and outputs are TTL compatible.
- Easy memory expansion by \bar{S}
- Common Data I/O
- Three-state outputs: OR-tie capability
- \bar{OE} prevents data contention in the I/O bus
- Process technology: 0.25 μ m CMOS
- Package:
 - M5M5408BFP: 32 pin 525 mil SOP
 - M5M5408BTP/RT: 32 pin 400 mil TSOP(II)

PART NAME TABLE

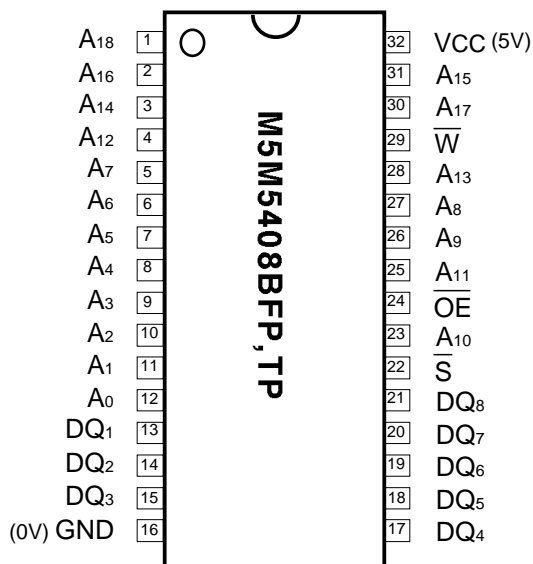
Version, Operating temperature	Part name (## stands for "FP","TP","RT")	Power Supply	Access time max.	Stand-by current I _{cc} (PD), V _{cc} =3.0V			Active current I _{cc} 1 (5.0V, typ.)
				typical *	Ratings (max.)		
				25°C	70°C	85°C	
Standard 0 ~ +70°C	M5M5408B## -55L	5.0V	55ns	---	50 μ A	---	50mA (10MHz) 25mA (1MHz)
	M5M5408B## -70L		70ns				
	M5M5408B## -55H	5.0V	55ns	0.4 μ A	15 μ A	---	
	M5M5408B## -70H		70ns				
W-version -20 ~ +85°C	M5M5408B## -55LW	5.0V	55ns	---	---	100 μ A	
	M5M5408B## -70LW		70ns				
	M5M5408B## -55HW	5.0V	55ns	0.4 μ A	---	30 μ A	
	M5M5408B## -70HW		70ns				
I-version -40 ~ +85°C	M5M5408B## -55LI	5.0V	55ns	---	---	100 μ A	
	M5M5408B## -70LI		70ns				
	M5M5408B## -55HI	5.0V	55ns	0.4 μ A	---	30 μ A	
	M5M5408B## -70HI		70ns				

* "typical" parameter is sampled, not 100% tested.

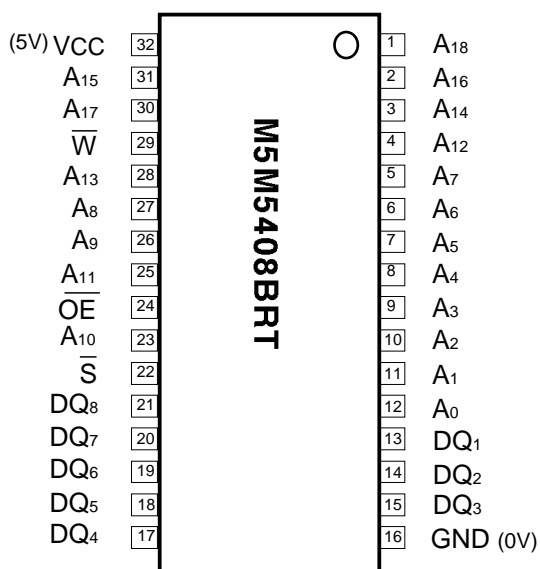
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PIN CONFIGURATION (TOP VIEW)



Outline 32P2M-A (FP)
32P3Y-H (TP)



Outline 32P3Y-J (RT)

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Units
V _{CC}	Supply voltage	With respect to GND	-0.3* ~ +7	V
V _I	Input voltage	With respect to GND	-0.3* ~ V _{CC} + 0.3	
V _O	Output voltage	With respect to GND	0 ~ V _{CC}	
P _d	Power dissipation	T _a =25°C	700	mW
T _a	Operating temperature	Standard (-L, -H)	0 ~ +70	°C
		W-version (-LW, -HW)	-20 ~ +85	
		I-version (-LI, -HI)	-40 ~ +85	
T _{stg}	Storage temperature		-65 ~ 150	°C

* -3.0V in case of AC (Pulse width 30ns)

DC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Units	
			Min	Typ	Max		
V _{IH}	High-level input voltage		2.2		V _{CC} +0.3V	V	
V _{IL}	Low-level input voltage		-0.3*		0.8		
V _{OH1}	High-level output voltage 1	I _{OH} = -1mA	2.4				
V _{OH2}	High-level output voltage 2	I _{OH} = -0.1mA	V _{CC} -0.5V				
V _{OL}	Low-level output voltage	I _{OL} =2mA			0.4		
I _I	Input leakage current	V _I =0 ~ V _{CC}			±1	µA	
I _O	Output leakage current	$\bar{S}=V_{IH}$ or $\bar{OE}=V_{IH}$, V _{I/O} =0 ~ V _{CC}			±1		
I _{CC1}	Active supply current (AC, MOS level)	\bar{S} 0.2V Output-open Other inputs 0.2V or V _{CC} -0.2V	f= 10MHz	-	50	80	mA
			f= 1MHz	-	25	30	
I _{CC2}	Active supply current (AC, TTL level)	$\bar{S}=V_{IL}$ Output-open Other inputs=V _{IH} or V _{IL}	f= 10MHz	-	60	90	
			f= 1MHz	-	30	40	
I _{CC3}	Stand by supply current (AC, MOS level)	\bar{S} V _{CC} -0.2V Other inputs=0~V _{CC}	-LW, -LI	-	-	200	µA
			-L	-	-	100	
			-HW, -HI	-	1.0	60	
			-H	-	1.0	30	
I _{CC4}	Stand by supply current (AC, TTL level)	$\bar{S}=V$,Other inputs= 0 ~ V _{CC}	-	-	3	mA	

Note 1: Direction for current flowing into IC is indicated as positive (no mark)

* -3.0V in case of AC (Pulse width 50ns)

Note 2: Typical value is for V_{CC}=5.0V and T_a=25°C

CAPACITANCE

(V_{CC}=5.0V±10%, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
C _I	Input capacitance	V _I =GND, V _I =25mVrms, f=1MHz			8	pF
C _O	Output capacitance	V _O =GND, V _O =25mVrms, f=1MHz			10	

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AC ELECTRICAL CHARACTERISTICS (V_{CC}=5.0V±10%, unless otherwise noted)

(1) TEST CONDITIONS

Supply voltage	5.0V
Input pulse	V _{IH} =2.4V, V _{IL} =0.6V (FP,TP,RT-70) V _{IH} =3.0V, V _{IL} =0V (FP,TP,RT-55)
Input rise time and fall time	5ns
Reference level	V _{OH} =V _{OL} =1.5V Transition is measured ±500mV from steady state voltage. (for t _{en} , t _{dis})
Output loads	Fig.1, CL=100pF (FP,TP,RT-70) CL=30pF (FP,TP,RT-55) CL=5pF (for t _{en} , t _{dis})

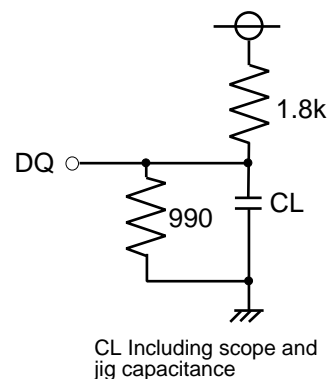


Fig.1 Output load

(2) READ CYCLE

Symbol	Parameter	Limits				Units
		M5M5408BFP,TP,RT-55		M5M5408BFP,TP,RT-70		
		Min	Max	Min	Max	
t _{CR}	Read cycle time	55		70		ns
t _{a(A)}	Address access time		55		70	ns
t _{a(S)}	Chip select access time		55		70	ns
t _{a(OE)}	Output enable access time		25		35	ns
t _{dis(S)}	Output disable time after \bar{S} high		20		25	ns
t _{dis(OE)}	Output disable time after \overline{OE} high		20		25	ns
t _{en(S)}	Output enable time after \bar{S} low	10		10		ns
t _{en(OE)}	Output enable time after \overline{OE} low	5		5		ns
t _{v(A)}	Data valid time after address	10		10		ns

(3) WRITE CYCLE

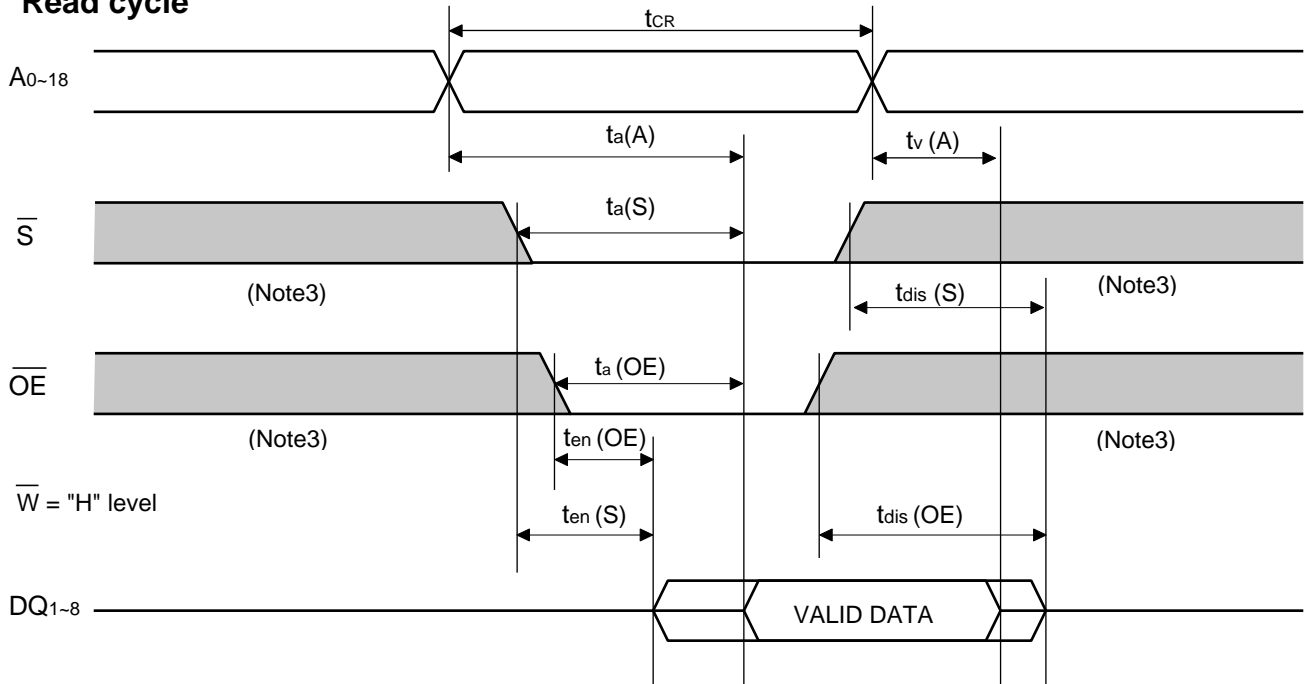
Symbol	Parameter	Limits				Units
		M5M5408BFP,TP,RT-55		M5M5408BFP,TP,RT-70		
		Min	Max	Min	Max	
t _{cw}	Write cycle time	55		70		ns
t _{w(W)}	Write pulse width	40		50		ns
t _{su(A)}	Address set up time	0		0		ns
t _{su(A-WH)}	Address set up time with respect to \bar{W} high	50		60		ns
t _{su(S)}	Chip select set up time	50		60		ns
t _{su(D)}	Data set up time	25		30		ns
t _{h(D)}	Data hold time	0		0		ns
t _{rec(W)}	Write recovery time	0		0		ns
t _{dis(W)}	Output disable time after \bar{W} low		20		25	ns
t _{dis(OE)}	Output disable time after \overline{OE} high		20		25	ns
t _{en(W)}	Output enable time after \bar{W} high	5		5		ns
t _{en(OE)}	Output enable time after \overline{OE} low	5		5		ns

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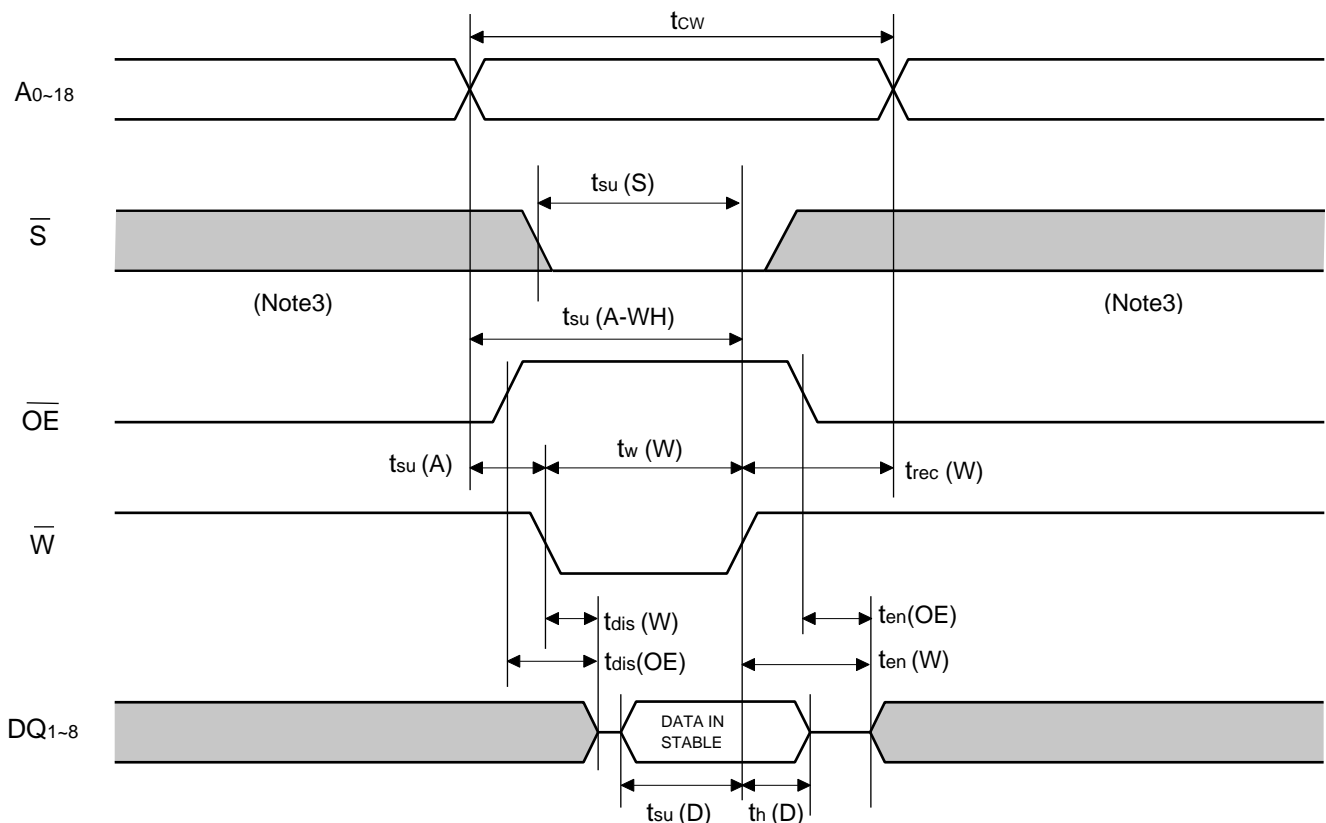
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(4)TIMING DIAGRAMS

Read cycle



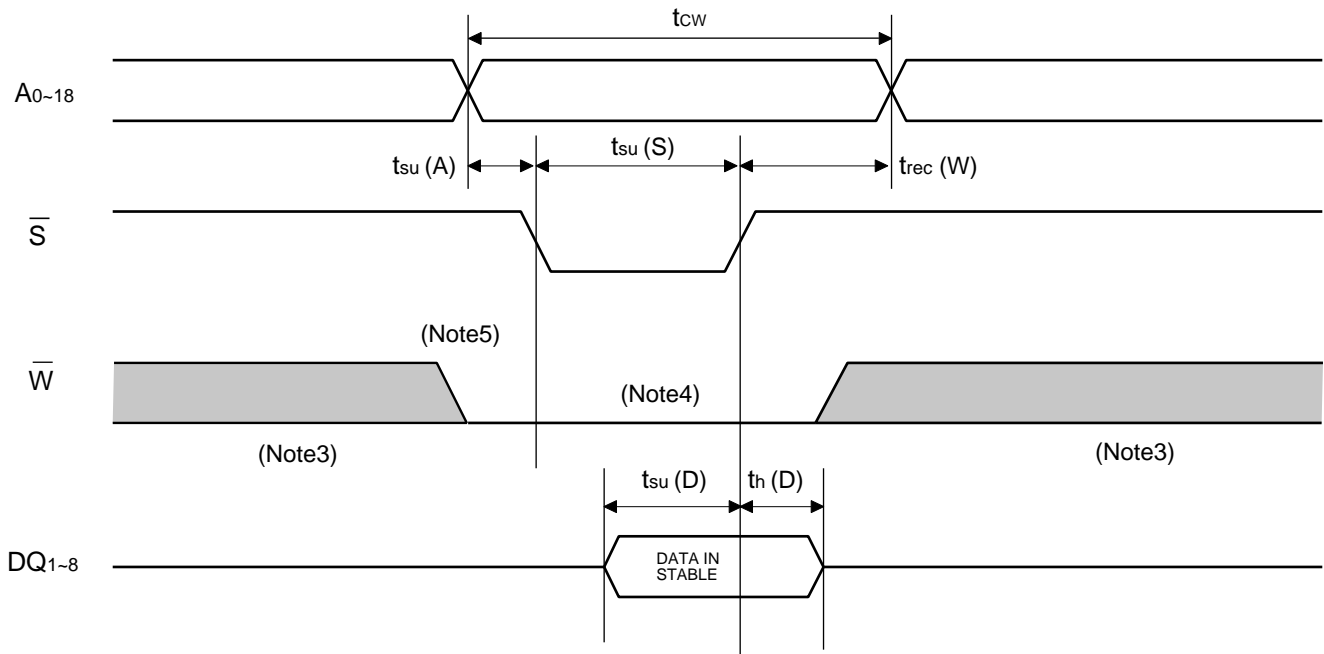
Write cycle (\bar{W} control mode)



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Write cycle (\overline{S} control mode)



Note 3: Hatching indicates the state is "don't care".

Note 4: A Write occurs during the overlap of a low \overline{S} and a low \overline{W} .

Note 5: If \overline{W} goes low simultaneously with or prior to \overline{S} , the output remains in the high impedance state.

Note 6: Don't apply inverted phase signal externally when DQ pin is in output mode.

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POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Units	
			Min	Typ.	Max		
V _{cc} (PD)	Power down supply voltage		2	-	-	V	
V _I (\bar{S})	Chip select input \bar{S}	V _{cc} (PD) 2.2V	2.2	-	-	V	
		2.2V V _{cc} (PD) 2.0V	-	V _{cc} (PD)	-	V	
I _{cc} (PD)	Power down supply current	V _{cc} =3.0V, \bar{S} V _{cc} -0.2V, Other inputs=0 ~ V _{cc}	-LW, -LI	-	-	100	μA
			-L	-	-	50	μA
			-HW, -HI	-	0.4	30	μA
			-H	-	0.4	15	μA

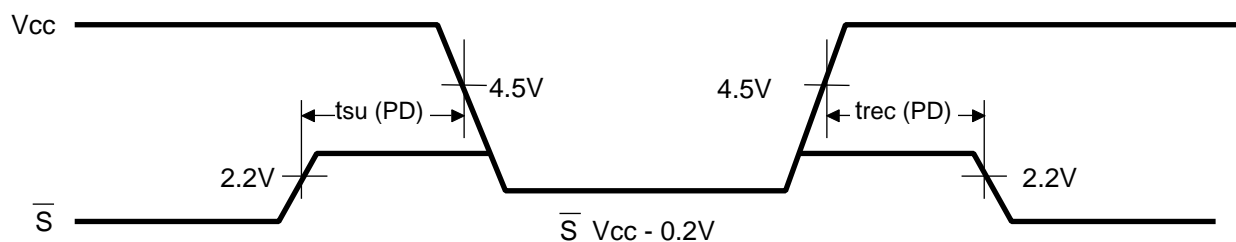
Typical value is for Ta=25°C

(2) TIMING REQUIREMENTS

Symbol	Parameter	Test conditions	Limits			Units
			Min	Typ	Max	
t _{su} (PD)	Power down set up time		0			ns
t _{rec} (PD)	Power down recovery time		5			ms

(3) TIMING DIAGRAM

\bar{S} control mode



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Revision History

<u>Revision No.</u>	<u>History</u>	<u>Date</u>	
K0.1e	The first edition	'98.7.30	Preliminary
K0.2e	1) Icc3 limit revised	'99.6.3	Preliminary
	2) Icc(PD) limit revised	'98.6.3	Preliminary
	3) Icc1,Icc2 conditions revised	'98.6.3	Preliminary
K0.3e	1) Vcc Level in the Block Diagram revised	'99.6.28	Preliminary
	2) Icc3 limit (typ) revised	'99.6.28	Preliminary
K1.0e	The first product version	'99.10.12	---
K1.1e	Product Lineup Revised	'99.10.21	---

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