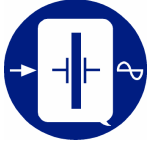


REVISIONS			
REVISION	DESCRIPTION	DATE	APPROVED
-	Initial release		
A	Change to microcircuit manufacturer, paragraph 3.3.3.1. Update frequency range, Table III	10/06/08	E.Jackson
B	Para 2.1, remove referenced revision letter from general specification number	05/20/09	C. Albright
C	Change paragraph 3.3.3.1 for use of AC191, Table II maximum voltage, Table III frequency range, current and tr/ff.	9/19/12	C. Albright

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SPECIFICATION CONTROL DRAWING			Q-TECH CORPORATION 10150 W. JEFFERSON BLVD. CULVER CITY, CA. 90232-3510				
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.  TOLERANCES: 3 PLACE DECIMAL = .005 2 PLACE DECIMAL = .02 1 PLACE DECIMAL = .1  FRACTIONS = ± 1/16 ANGLES = 2 DEGREES	PREPARED BY	DATE	<b>HYBRID CRYSTAL OSCILLATOR +5V, CLASS S, DETAIL SPECIFICATION FOR</b>				
	Curtis Hooper	9/17/12					
	CHECKED BY	DATE	DRAWING NO.		REV.		
	Minh Dao	9/17/12	<b>QT641C</b>		<b>C</b>		
	RELEASED BY	DATE	SCALE:	SIZE	CAGE CODE	SHEET 1 of 5	
	Peter Steinblums	9/20/12	<b>NONE</b>	<b>A</b>	<b>51774</b>		

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**1 SCOPE**

- 1.1 Scope. This specification establishes the detail requirements for hybrid, hermetically sealed, crystal oscillators for use in space flight missions.
- 1.2 Part number. The part number shall be as specified in Table I herein.

**2 APPLICABLE DOCUMENTS**

- 2.1 Specifications and standards. Unless otherwise specified, the following documents shall be applicable to this specification to the extent specified herein.

**SPECIFICATIONS**

401-0298-001                      Hybrid Crystal Oscillators, Class S, General Specification For

**3 REQUIREMENTS**

- 3.1 General requirements. The individual item requirements shall be as specified in the General Specification with the exceptions, modifications, and additions specified herein.
- 3.2 Approved manufacturer. Hybrid crystal oscillators shall be supplied from the manufacturer specified in paragraph 7.1 herein.
- 3.3 Design and construction.
  - 3.3.1. Outline dimensions and terminal connections. The outline dimensions and terminal connections shall be as shown in Figure 1 herein.
  - 3.3.2. Package body and lead finish. The package body and lead finish shall be gold in accordance with MIL-PRF-38534.
  - 3.3.3. Active Devices. The microcircuit used in this part shall use CMOS technology and shall be from a wafer proven to be radiation tolerant to 100 kRad (Si) total ionizing dose.
  - 3.3.3.1 CMOS microcircuit usage. For frequencies below 16 MHZ the CMOS output microcircuit shall be 54AC191, see DSCC SMD 5962-89749. For frequencies greater than or equal to 16 MHZ, the CMOS microcircuit shall be 54AC00, see DSCC SMD 5962-87549. These microcircuits are specified to be *single event latchup free* for LET up to 93 MeV-cm<sup>2</sup>/mg. The manufacturer shall be ST Microelectronics Corporation.
- 3.4 Performance requirements.
  - 3.4.1. Maximum ratings. The maximum ratings shall be as specified in Table II herein.
  - 3.4.2. Electrical performance characteristics and limits. The electrical performance requirements and limits shall be in accordance with Table III herein.
  - 3.4.3. Delta limits. Except for frequency aging (refer to Table III), delta limits shall be in accordance with the General Specification.
  - 3.4.4. Total dose radiation limits. Hybrid crystal oscillators supplied in accordance with this specification shall be capable of meeting the performance requirements after being exposed to 100 krad total dose radiation levels.

**4 QUALITY ASSURANCE PROVISIONS**

- 4.1 General. The quality assurance provisions shall be in accordance with the General Specification with the exceptions, modifications, and additions specified herein.
- 4.2 Screening tests. The screening tests shall be in accordance with the General Specification.

4.3 Quality Conformance Inspection. Quality Conformance Inspection shall be in accordance with the General Specification and shall be required only when specified by the purchase order.

**5 PACKAGING**

5.1 Preservation, packaging and packing. Hybrid crystal oscillators shall be prepared for delivery in accordance with the General specification.

**6 NOTES**

6.1 Notes. The notes of the General Specification are applicable to this drawing.

6.2 Ordering information. The procuring activity shall advise Q-Tech Corporation at the time of Request for Quotation if quality conformance inspection is to be required.

6.3 Part number. QT641 C B 1 M - 16.000000 MHZ  
 Model # \_\_\_\_\_  
 Supply voltage: C: + 5.0 volts \_\_\_\_\_  
 Temp stability - see Table I \_\_\_\_\_  
 Duty cycle: 1: 60/40% \_\_\_\_\_  
                   2: 45/55% (available up to 100 MHz) \_\_\_\_\_  
 Screening: E: engineering model; M: flight model \_\_\_\_\_  
 Frequency (8 digits) \_\_\_\_\_

<b>TABLE I. STABILITY / TEMPERATURE OPTIONS</b>	
<b>OPTION</b>	<b>TEMP STABILITY</b>
<b>A</b>	± 65 PPM, - 55 °C TO + 125 °C
<b>B</b>	± 50 PPM, - 55 °C TO + 125 °C
<b>C</b>	± 50 PPM, - 55 °C TO + 105 °C
<b>D</b>	± 40 PPM, - 55 °C TO + 105 °C
<b>E</b>	± 30 PPM, - 40 °C TO + 85 °C
<b>F</b>	± 50 PPM, - 20 °C TO + 70 °C
<b>G</b>	± 25 PPM, - 20 °C TO + 70 °C
<b>H *</b>	± 5 PPM, 0 °C TO + 55 °C

\* Frequency/Temperature stability (tolerance) shall be referenced to the specified nominal output frequency, except for temp code H, in which case it is with reference to room temperature (T = 25 ± 2 °C). For temp code H, room temperature tolerance shall be ±10 PPM.

**7 SOURCE OF SUPPLY**

7.1 Approved manufacturer.

Q-Tech Corporation  
 10150 W. Jefferson Blvd.  
 Culver City, Ca. 90232 U.S.A.

**TABLE II. MAXIMUM RATINGS**

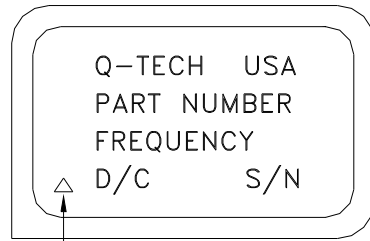
Parameter	Symbol	Min	Max	Units
Supply voltage	V <sub>CC</sub>	0	6	Volts
Operating temperature	T <sub>c</sub>	-55	125	°C
Storage temperature	T <sub>stg</sub>	-65	150	°C
Lead solder temperature/time			250/10	°C/seconds
Package thermal resistance	θ <sub>jc</sub>		50	°C/W

**TABLE III. ELECTRICAL PERFORMANCE CHARACTERISTICS**

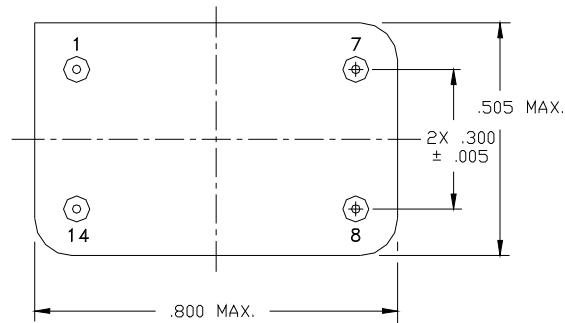
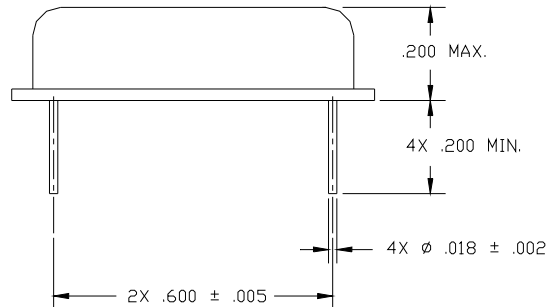
ELECTRICAL PARAMETER	TEST CONDITIONS 2/,3/	LIMITS				NOTES
		MIN.	NOM.	MAX.	UNITS	
FREQUENCY RANGE		1		100	MHz	
FREQUENCY/TEMPERATURE STABILITY		See Table I				1/, 4/
SUPPLY VOLTAGE		4.5	5	5.5	Vdc	
INPUT CURRENT	<b>Output frequency:</b>					
Measured without load at 5.5 Vdc	< 10 MHZ			15	mA	
	10 MHZ - 59.99 MHZ			25	mA	
	60 MHZ - 100 MHZ			45	mA	
LOAD			CMOS		-	6/
OUTPUT VOLTAGE - LOGIC "0"				V <sub>CC</sub> x 0.1	Vdc	5/
OUTPUT VOLTAGE - LOGIC "1"		V <sub>CC</sub> x 0.9			Vdc	5/
OUTPUT WAVEFORM		Squarewave			N/A	
RISE / FALL TIME @ worst case, V <sub>CC</sub> = 4.5, T = 125 °C	<b>Output frequency:</b>					
	< 80 MHZ			3.5	nS	6/
	> 80 MHZ			2.5	nS	6/
DUTY CYCLE (See Table I)	Option 1:	60/40 or better			%	
	Option 2:	45/55 or better			%	
FREQUENCY AGING (AFTER 30 DAYS)	70 °C ± 3°C			±1.5	ppm	
FREQUENCY AGING (AFTER 1 YEAR)	70 °C ± 3°C			±10	ppm	
STARTUP TIME				10	ms	

**NOTES**

1. The limit for frequency/temperature stability (tolerance) shall be referenced to the specified nominal output frequency, except for temp code H as noted above.
1. Unless otherwise specified, the limits are over the full operating temperature range and under specified load conditions.
2. Unless otherwise specified, all measurements are in accordance with MIL-PRF-55310.
3. Up to 30 days after shipment.
4. Voltage values are with respect to network ground terminal.
5. A standard CMOS load of 10 kOhm || 15 pF shall be used. See MIL-PRF-55310/26 for CMOS waveform measurement definitions.



ESD SYMBOL FOR PIN NO. 1



**NOTES:**

1. Dimensions are in inches.
2. Lead numbers are for reference only and are not marked on the unit.
3. A triangle symbol is marked on the corner of the package to indicate Pin 1.
4. All pins with function NC and/or ITP may not be connected as external tie or connections.

TERMINAL NO	CONNECTION	TERMINAL NO	CONNECTION
1	N/C	8	OUTPUT
7	GND/CASE	14	V <sub>cc</sub>

**PACKAGE DIMENSIONS AND TERMINAL CONNECTIONS**