Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS 10-BIT BUFFERS AND BUS DRIVERS

ADVANCE INFORMATION
IDT54/74FBT827A/B/C
IDT54/74FBT828A/B/C

FEATURES:

- Functionally equivalent to 54/74BCT827A/828A
- **IDT54/74FBT827B/828B 25% faster than the 827A/828A**
- **IDT54/74FBT827C/828C 10% faster than the 827B/828B**
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- Low power in all three states
- ± 10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

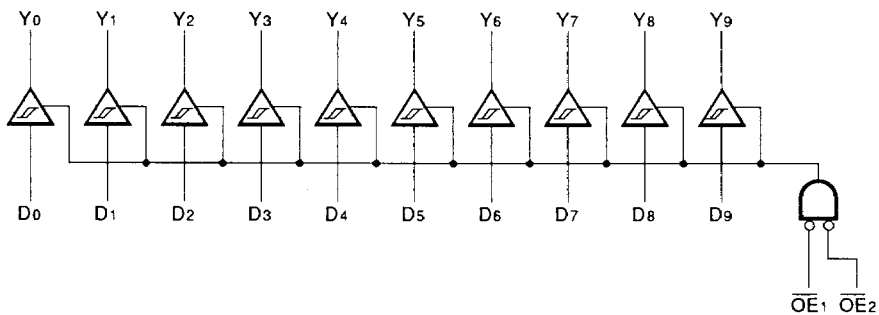
DESCRIPTION:

The FBT series of BiCMOS buffers and bus drivers are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is desgined to supply the highest device speeds while maintaining CMOS power levels.

The IDT54/74FBT827 and IDT54/74FBT828 are 3-state, 10-bit bus drivers. They provide bus interface to wide data/address paths or buses carrying parity. The output buffers are enabled when the two active-low output enable pins are both logic low.

The FBT series of buffers are ideal for use in designs needing to drive large capacitive loads with low static (DC) current loading. All data inputs have a 200mV typical input hysteresis for improved noise rejection.

FUNCTIONAL BLOCK DIAGRAM[1]



2598 drw 01

NOTE:
1. Non-inverting part shown.

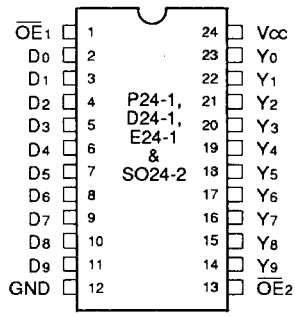
PRODUCT SELECTOR GUIDE

	10-Bit Buffers
Non-inverting	IDT54/74FBT827A/B/C
Inverting	IDT54/74FBT828A/B/C

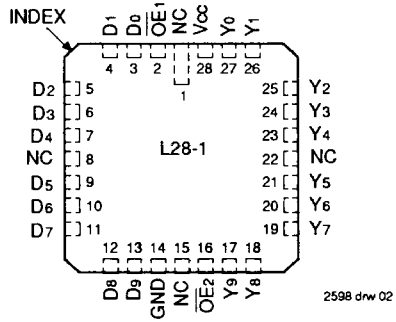
2598 tbl 01

BiCEMOS is a trademark of Integrated Device Techology, Inc.

PIN CONFIGURATIONS



DIP/CERPACK/SOIC
TOP VIEW



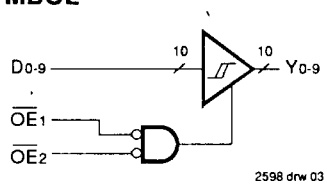
LCC
TOP VIEW

PIN DESCRIPTION

Name	I/O	Description
$\overline{OE}_{1, 2}$	I	When both are LOW the outputs are enabled. When either one or both are HIGH the outputs are High Z.
D_0 - D_9	I	10-bit data input.
Y_0 - Y_9	O	10-bit data output.

2598 tbl 02

LOGIC SYMBOL



2598 drw 03

FUNCTION TABLES

IDT54/74FBT827A/B/C (NON-INVERTING)(1)

Inputs			Output	
$\overline{OE}_1$	$\overline{OE}_2$	D_I	Y_I	Function
L	L	L	L	Transparent
L	L	H	H	
H	X	X	Z	Three-state
X	H	X	Z	

NOTE:
1.H = HIGH, L = LOW, X = Don't Care, Z = High Impedance.

2598 tbl 03

IDT54/74FBT828A/B/C (INVERTING)(1)

Inputs			Output	
$\overline{OE}_1$	$\overline{OE}_2$	D_I	Y_I	Function
L	L	L	H	Transparent
L	L	H	L	
H	X	X	Z	Three-state
X	H	X	Z	

NOTE:
1. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance.

2598 tbl 04

6

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2598 tbl 05

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2598 tbl 06

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = 2.7V		—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = 0.5V		—	—	-10	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_O = 2.7V	—	—	50	µA
I_{OZL}	Output Current		V_O = 0.5V	—	—	-50	
I_I	Input HIGH Current	V_{CC} = Max., V_I = 5.5V		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND(3)		-75	-150	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -12mA MIL. I_{OH} = -15mA COM'L.	2.4	3.3	—	V
			I_{OH} = -18mA MIL. I_{OH} = -24mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage		I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	V_{CC} = 5V		—	200	—	mV
I_{OFF}	Bus Leakage Current	V_{CC} = 0V, V_O = 4.5V		—	—	100	µA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

NOTES: 2598 tbl 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max. V_{IN} = 3.4V[3]		—	—	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE_1}$ = $\overline{OE_2}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	4.0	mA
		$\overline{OE_1}$ = $\overline{OE_2}$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	5.0	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	7.8[5]	
		$\overline{OE_1}$ = $\overline{OE_2}$ = GND Ten Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	17.8[5]	

2598 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient, and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz..

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE – IDT54/74FBT827A/B/C

Symbol	Parameter	Condition[1]	54/74FBT827A				54/74FBT827B				54/74FBT827C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPHL tPLH	Propagation Delay DI to YI	CL = 50pF RL = 500Ω	—	7.0	—	—	—	5.0	—	—	—	4.4	—	—	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to YI		—	12.0	—	—	—	8.0	—	—	—	7.0	—	—	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to YI		—	12.0	—	—	—	7.0	—	—	—	6.0	—	—	ns

SWITCHING CHARACTERISTICS OVER OPERATING RANGE – IDT54/74FBT828A/B/C

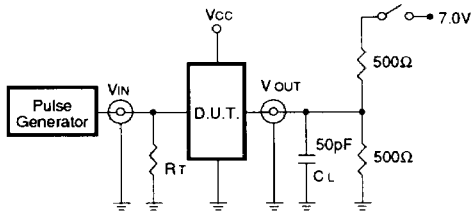
Symbol	Parameter	Condition[1]	54/74FBT828A				54/74FBT828B				54/74FBT828C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPHL tPLH	Propagation Delay DI to YI	CL = 50pF RL = 500Ω	—	7.0	—	—	—	5.5	—	—	—	4.4	—	—	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to YI		—	11.0	—	—	—	8.0	—	—	—	7.0	—	—	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to YI		—	10.0	—	—	—	7.0	—	—	—	6.0	—	—	ns

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed, but not tested.

2598 tbl 07

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

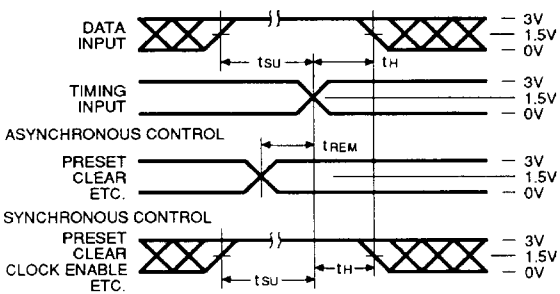
2598 tbl 08

DEFINITIONS:

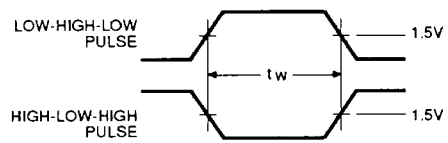
C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

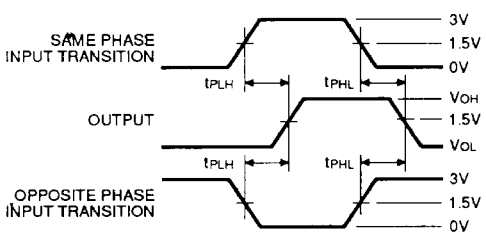
SET-UP, HOLD AND RELEASE TIMES



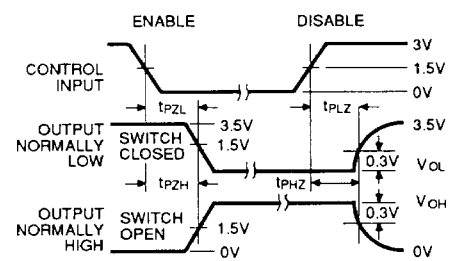
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



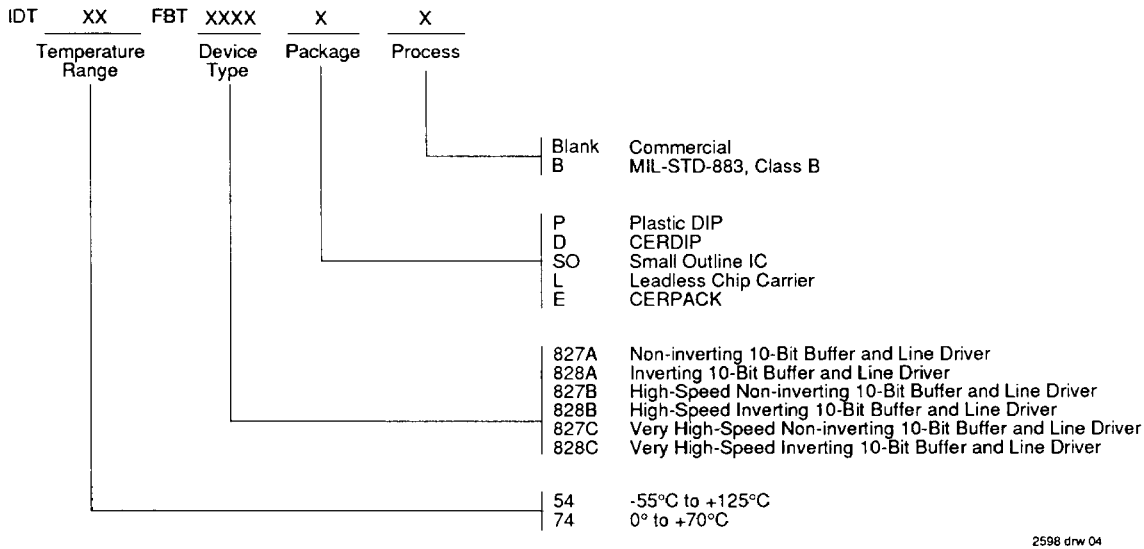
2598 drw 04

NOTES

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Z_O ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

6

ORDERING INFORMATION



2598 drw 04