

**TMS426160, TMS426160P**  
**1 048 576-WORD BY 16-BIT HIGH-SPEED**  
**LOW VOLTAGE DYNAMIC RANDOM-ACCESS MEMORIES**

SMKS266-DECEMBER 1992

- **Organization . . . 1 048 576 × 16**
- **Single 3.3-V Supply (± 0.3 V Tolerance)**

• **Performance Ranges:**

|              | ACCESS TIME          | ACCESS TIME          | ACCESS TIME         | READ OR WRITE CYCLE |
|--------------|----------------------|----------------------|---------------------|---------------------|
|              | t <sub>RAC</sub> MAX | t <sub>CAC</sub> MAX | t <sub>AA</sub> MAX | MIN                 |
| '426160/P-70 | 70 ns                | 18 ns                | 35 ns               | 130 ns              |
| '426160/P-80 | 80 ns                | 20 ns                | 40 ns               | 150 ns              |

- **Enhanced Page Mode Operation With CAS-Before-RAS Refresh**
- **Long Refresh Period . . . 4096-Cycle Refresh in 64 ms (Max) 512 ms Max for Low-Power, Self-Refresh Version (TMS426160P)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
  - 100 µA CMOS Standby
  - 100 µA Extended Refresh Battery Backup
- **Self-Refresh with Low Power**
- **All Inputs, Outputs, and Clocks are TTL Compatible**
- **High-Reliability Plastic 42-Lead 400-Mil-Wide Surface Mount (SOJ) Package, and 44/50-Lead Thin Small Outline Package (TSOP)**
- **Operating Free-Air Temperature Range 0°C to 70°C**
- **Texas Instruments EPIC™ CMOS Process**

**description**

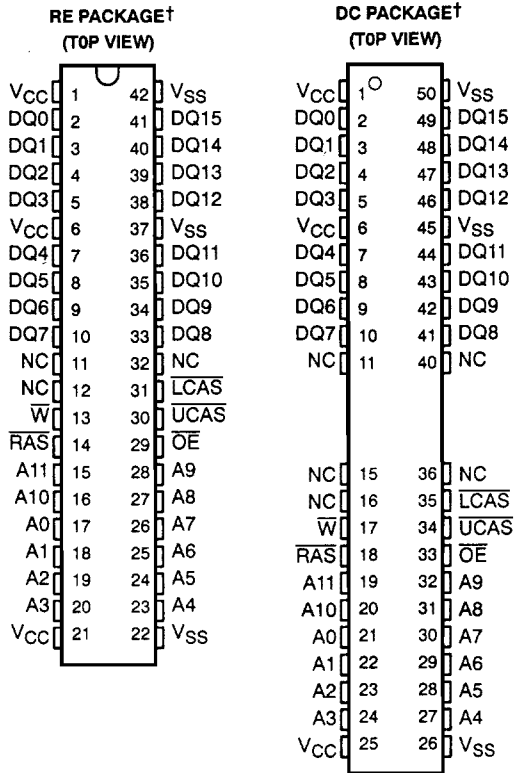
The TMS426160 series are high-speed, low voltage, 16 777 216-bit dynamic random-access memories organized as 1 048 576 words of sixteen bits each.

The TMS426160P series are high-speed, low voltage, low-power, self-refresh, 16 777 216-bit dynamic random-access memories organized as 1 048 576 words of sixteen bits each.

They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at low cost.

These devices feature maximum RAS access times of 70 ns and 80 ns. Maximum power dissipation is as low as 0.36 mW standby and battery backup on 80-ns devices.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.



† Packages are shown for pinout reference only.

| PIN NOMENCLATURE |                             |
|------------------|-----------------------------|
| A0-A11           | Address Inputs              |
| DQ0-DQ15         | Data In/Data Out            |
| <u>LCAS</u>      | Lower Column-Address Strobe |
| <u>UCAS</u>      | Upper Column-Address Strobe |
| NC               | No Internal Connection      |
| <u>OE</u>        | Output Enable               |
| <u>RAS</u>       | Row-Address Strobe          |
| <u>W</u>         | Write Enable                |
| V <sub>CC</sub>  | 3.3-V Supply                |
| V <sub>SS</sub>  | Ground                      |

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# TMS426160, TMS426160P

## 1 048 576-WORD BY 16-BIT HIGH-SPEED LOW VOLTAGE DYNAMIC RANDOM-ACCESS MEMORIES

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The TMS426160 and TMS426160P are each offered in a 42-lead plastic surface mount SOJ (RE suffix) package, and a 44/50-lead plastic surface mount TSOP (DC suffix). These packages are characterized for operation from 0°C to 70°C.

### operation

#### dual $\overline{\text{CAS}}$

Two  $\overline{\text{CAS}}$  pins ( $\overline{\text{LCAS}}$ – $\overline{\text{UCAS}}$ ) are provided to give independent control of the sixteen data I/O pins (DQ0–DQ15), with  $\overline{\text{LCAS}}$  corresponding to DQ0–DQ7 and  $\overline{\text{UCAS}}$  corresponding to DQ8–DQ15. For read or write cycles, the column address is latched on the first  $\overline{\text{xCAS}}$  falling edge. Each  $\overline{\text{xCAS}}$  pin going low enables its corresponding DQ pin with data coming from the column address to be latched on the first falling  $\overline{\text{xCAS}}$  edge. All address setup and hold parameters are referenced to the first falling  $\overline{\text{xCAS}}$  edge. The delay time from  $\overline{\text{xCAS}}$  low to valid data out (see parameter  $t_{\text{CAC}}$ ) is measured from each individual  $\overline{\text{CAS}}$  to its corresponding DQx pin.

In order to latch in a new column address, all  $\overline{\text{xCAS}}$  pins must be brought high. The column precharge time (see parameter  $t_{\text{CP}}$ ) is measured from the last  $\overline{\text{xCAS}}$  rising edge to the first falling  $\overline{\text{xCAS}}$  edge of the new cycle. Keeping a column address valid while toggling  $\overline{\text{xCAS}}$  requires a minimum setup time,  $t_{\text{CLCH}}$ . During  $t_{\text{CLCH}}$ , at least one  $\overline{\text{xCAS}}$  must be brought low before the other  $\overline{\text{xCAS}}$  is taken high.

For early write cycles, the data is latched on the first falling  $\overline{\text{xCAS}}$  edge. Only the DQs that have the corresponding  $\overline{\text{xCAS}}$  low will be written into. Each  $\overline{\text{xCAS}}$  will have to meet  $t_{\text{CAS min}}$  in order to ensure writing into the storage cell. In order to latch a new address and new data, all  $\overline{\text{xCAS}}$  pins need to come high and meet  $t_{\text{CP}}$ .

#### enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum  $\overline{\text{RAS}}$  low time and the  $\overline{\text{xCAS}}$  page-mode cycle time used. With minimum  $\overline{\text{xCAS}}$  page cycle time, all 256 columns specified by column addresses A0 through A7 can be accessed without intervening  $\overline{\text{RAS}}$  cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of  $\overline{\text{RAS}}$ . The buffers act as transparent or flow-through latches while  $\overline{\text{xCAS}}$  is high. The falling edge of the first  $\overline{\text{xCAS}}$  latches the column addresses. This feature allows the devices to operate at a higher data bandwidth than conventional page-mode parts, because data retrieval begins as soon as column address is valid rather than when  $\overline{\text{xCAS}}$  transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after  $t_{\text{RAH}}$  (row address hold time) has been satisfied, usually well in advance of the falling edge of  $\overline{\text{xCAS}}$ . In this case, data is obtained after  $t_{\text{CAC max}}$  (access time from  $\overline{\text{xCAS}}$  low) if  $t_{\text{AA max}}$  (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time  $\overline{\text{xCAS}}$  goes high, minimum access time for the next cycle is determined by  $t_{\text{CPA}}$  (access time from rising edge of the last  $\overline{\text{xCAS}}$ ).

#### address (A0–A11)

Twenty address bits are required to decode 1 of 1 048 576 storage cell locations. Twelve row-address bits are set up on pins A0 through A11 and latched onto the chip by  $\overline{\text{RAS}}$ . Then, eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the first  $\overline{\text{xCAS}}$ . All addresses must be stable on or before the falling edge of  $\overline{\text{RAS}}$  and  $\overline{\text{xCAS}}$ .  $\overline{\text{RAS}}$  is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder.  $\overline{\text{xCAS}}$  is used as a chip select, activating its corresponding output buffer and latching the address bits into the column-address buffers.

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### write enable ( $\overline{W}$ )

The read or write mode is selected through the  $\overline{W}$  input. A logic high on the  $\overline{W}$  input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from the standard TTL circuits without a pullup resistor. The data inputs are disabled when the read mode is selected. When  $\overline{W}$  goes low prior to  $\overline{xCAS}$  (early write), data out will remain in the high-impedance state for the entire cycle permitting a write operation with  $\overline{OE}$  grounded.

### data in (DQ0–DQ15)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of  $\overline{xCAS}$  or  $\overline{W}$  strobes data into the on-chip data latch. In an early-write cycle,  $\overline{W}$  is brought low prior to  $\overline{xCAS}$  and the data is strobed in by the first occurring  $\overline{xCAS}$  with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle,  $\overline{xCAS}$  will already be low, thus the data will be strobed in by  $\overline{W}$  with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle,  $\overline{OE}$  must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

### data out (DQ0–DQ15)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until  $\overline{xCAS}$  and  $\overline{OE}$  are brought low. In a read cycle, the output becomes valid after the access time interval  $t_{CAC}$  (which begins with the negative transition of  $\overline{xCAS}$ ) as long as  $t_{RAC}$  and  $t_{AA}$  are satisfied.

### output enable ( $\overline{OE}$ )

$\overline{OE}$  controls the impedance of the output buffers. When  $\overline{OE}$  is high, the buffers will remain in the high-impedance state. Bringing  $\overline{OE}$  low during a normal cycle will activate the output buffers, putting them in the low-impedance state. It is necessary for both  $\overline{RAS}$  and  $\overline{xCAS}$  to be brought low for the output buffers to go into low-impedance state, they will remain in the low-impedance state until either  $\overline{OE}$  or  $\overline{xCAS}$  is brought high.

### $\overline{RAS}$ -only refresh

A refresh operation must be performed at least once every sixty-four milliseconds (512 ms for TMS426160P) to retain data. This can be achieved by strobing each of the 4096 rows (A0–A11). A normal read or write cycle will refresh all bits in each row that is selected. A  $\overline{RAS}$ -only operation can be used by holding all  $\overline{xCAS}$  at the high (inactive) level, thus conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a  $\overline{RAS}$ -only refresh.

### hidden refresh

Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding  $\overline{xCAS}$  at  $V_{IL}$  after a read operation and cycling  $\overline{RAS}$  after a specified precharge period, similar to a  $\overline{RAS}$ -only refresh cycle.

### $\overline{xCAS}$ -before- $\overline{RAS}$ refresh

$\overline{xCAS}$ -before- $\overline{RAS}$  refresh is utilized by bringing at least one  $\overline{xCAS}$  low earlier than  $\overline{RAS}$  (see parameter  $t_{CSR}$ ) and holding it low after  $\overline{RAS}$  falls (see parameter  $t_{CHR}$ ). For successive  $\overline{xCAS}$ -before- $\overline{RAS}$  refresh cycles,  $\overline{xCAS}$  can remain low while cycling  $\overline{RAS}$ . The external address is ignored and the refresh address is generated internally. The external address is also ignored during the hidden refresh option.

A low-power battery-backup refresh mode that requires less than 100  $\mu A$  refresh current is available on the TMS426160P. Data integrity is maintained using  $\overline{xCAS}$ -before- $\overline{RAS}$  refresh with a period of 125  $\mu s$  while holding  $\overline{RAS}$  low for less than 1  $\mu s$ . To minimize current consumption, all input levels need to be at CMOS levels ( $V_{IL} < 0.2 V$ ,  $V_{IH} > V_{CC} - 0.2 V$ ).

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**self refresh (TMS426160P)**

The self-refresh mode is entered by dropping  $\overline{xCAS}$  low prior to  $\overline{RAS}$  going low. Then  $\overline{xCAS}$  and  $\overline{RAS}$  are both held low for a minimum of 100  $\mu s$ . The chip is then refreshed internally by an on-board oscillator. No external address is required since the CBR counter is used to keep track of the address. To exit the self-refresh mode both  $\overline{RAS}$  and  $\overline{xCAS}$  are brought high to satisfy  $t_{CHS}$ . Upon exiting self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. The burst refresh ensures the DRAM is fully refreshed.

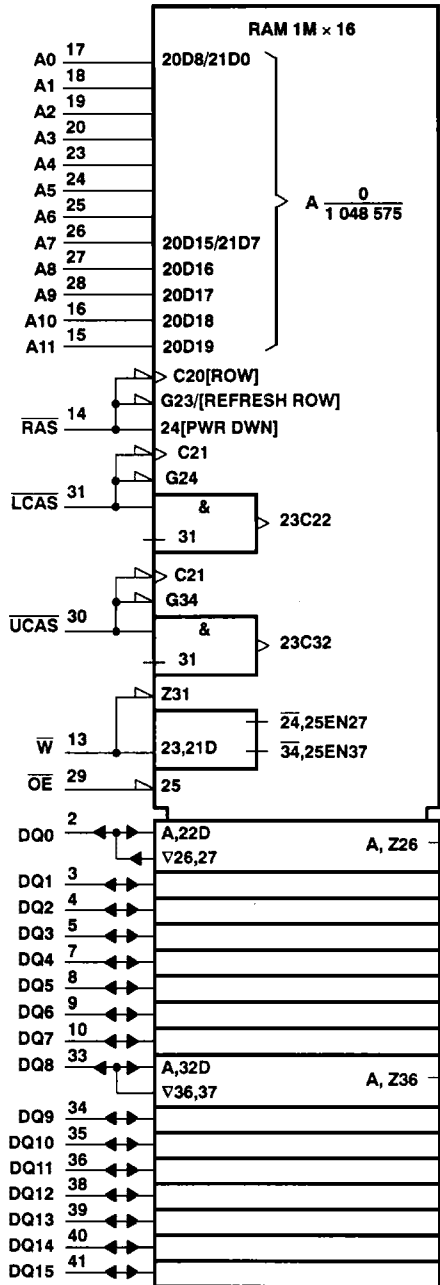
**power up**

To achieve proper device operation, an initial pause of 200  $\mu s$  followed by a minimum of eight  $\overline{RAS}$  cycles is required after power up to the full  $V_{CC}$  level.

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logic symbol†

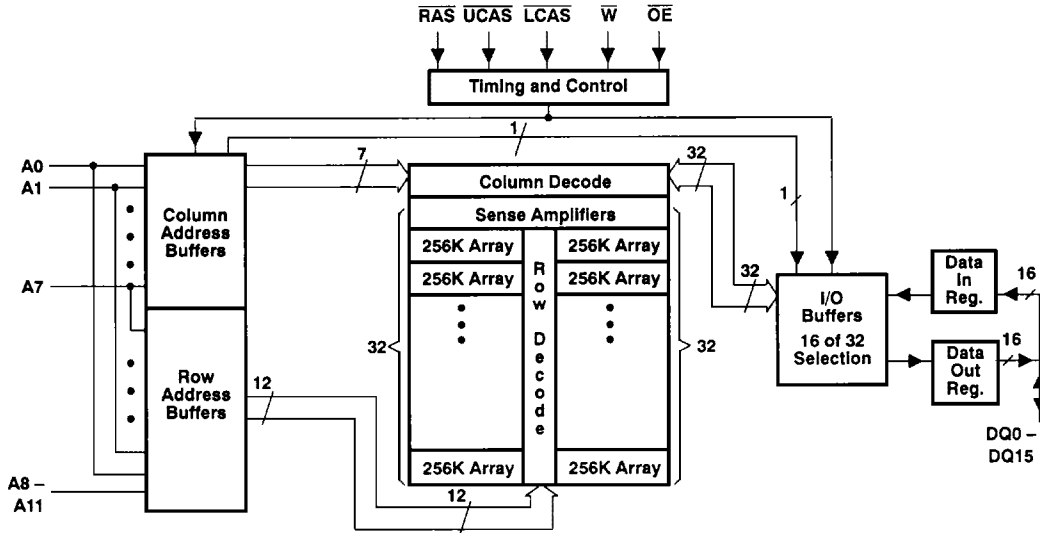


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† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
 The pin numbers shown correspond to the RE package.

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**functional block diagram**



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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

|  |                  |
|--|------------------|
| Supply voltage range on any pin (see Note 1) | - 0.5 V to 4.6 V |
| Supply voltage range on V <sub>CC</sub>      | - 0.5 V to 4.6 V |
| Short circuit output current                 | 50 mA            |
| Power dissipation                            | 1 W              |
| Operating free-air temperature               | 0°C to 70°C      |
| Storage temperature range                    | - 55°C to 125°C  |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V<sub>SS</sub>.

**recommended operating conditions**

|  | MIN   | NOM                  | MAX | UNIT |
|--|-------|----------------------|-----|------|
| V <sub>CC</sub> Supply voltage                       | 3.0   | 3.3                  | 3.6 | V    |
| V <sub>SS</sub> Supply voltage                       |       | 0                    |     | V    |
| V <sub>IH</sub> High-level input voltage             | 2.0   | V <sub>CC</sub> +0.3 |     | V    |
| V <sub>IL</sub> Low-level input voltage (see Note 2) | - 0.3 |                      | 0.8 | V    |
| T <sub>A</sub> Operating free-air temperature        | 0     |                      | 70  | °C   |

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

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**electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)**

| PARAMETER  | TEST CONDITIONS   | '426160-70<br>'426160P-70 |      | '426160-80<br>'426160P-80 |      | UNIT |
|--|---|---------------------------|------|---------------------------|------|------|
|  |   | MIN                       | MAX  | MIN                       | MAX  |      |
| V <sub>OH</sub> High-level output voltage  | I <sub>OH</sub> = -2 mA   | 2.4                       |      | 2.4                       |      | V    |
| V <sub>OL</sub> Low-level output voltage   | I <sub>OL</sub> = 2 mA  |                           | 0.4  |                           | 0.4  | V    |
| V <sub>OH</sub> Option   | I <sub>OH</sub> = -100 μA   | V <sub>CC</sub> -0.2      |      | V <sub>CC</sub> -0.2      |      | V    |
| V <sub>OL</sub> Option   | I <sub>OL</sub> = 100 μA  |                           | 0.2  |                           | 0.2  | V    |
| I <sub>I</sub> Input current (leakage)   | V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = 0 to 3.9 V,<br>All other pins = 0 V to V <sub>CC</sub>  |                           | ± 10 |                           | ± 10 | μA   |
| I <sub>O</sub> Output current (leakage)  | V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 0 to V <sub>CC</sub> , $\overline{x}CAS$ high   |                           | ± 10 |                           | ± 10 | μA   |
| I <sub>CC1</sub> †‡ Read or write cycle current  | V <sub>CC</sub> = 3.6 V, Minimum cycle  |                           | 80   |                           | 70   | mA   |
| I <sub>CC2</sub> Standby current   | V <sub>IH</sub> = 2 V (LVTTTL),<br>After 1 memory cycle,<br>$\overline{RAS}$ and $\overline{x}CAS$ high   |                           | 1    |                           | 1    | mA   |
|  | V <sub>IH</sub> = V <sub>CC</sub> - 0.2 V (LVCMOS),<br>After 1 memory cycle,<br>$\overline{RAS}$ and $\overline{x}CAS$ high   | '426160                   | 300  |                           | 300  | μA   |
|  |   | '426160P                  | 100  |                           | 100  | μA   |
| I <sub>CC3</sub> ‡ Average refresh current ( $\overline{RAS}$ -only or CBR)                          | V <sub>CC</sub> = 3.6 V, Minimum cycle,<br>$\overline{RAS}$ cycling, $\overline{x}CAS$ high ( $\overline{RAS}$ only)<br>$\overline{RAS}$ low after $\overline{x}CAS$ low (CBR)                                      |                           | 80   |                           | 70   | mA   |
| I <sub>CC4</sub> †§ Average page current   | V <sub>CC</sub> = 3.6 V, t <sub>PC</sub> = minimum,<br>$\overline{RAS}$ low, $\overline{x}CAS$ cycling  |                           | 80   |                           | 70   | mA   |
| I <sub>CC6</sub> ¶ Self refresh  | $\overline{CAS} < 0.2 V$ , $\overline{RAS} < 0.2 V$ ,<br>Measured after t <sub>RASS</sub> minimum   |                           | 100  |                           | 100  | μA   |
| I <sub>CC7</sub> † Standby current, outputs enabled  | $\overline{RAS} = V_{IH}$ , $\overline{x}CAS = V_{IL}$ ,<br>Data out = enabled  |                           | 5    |                           | 5    | mA   |
| I <sub>CC10</sub> ¶ Battery back-up operating current (equivalent refresh time is 512 ms), CBR only. | t <sub>RC</sub> = 125 μs, t <sub>RAS</sub> ≤ 1 μs,<br>V <sub>CC</sub> - 0.2 V ≤ V <sub>IH</sub> ≤ 3.9 V,<br>0 V ≤ V <sub>IL</sub> ≤ 0.2 V, $\overline{W}$ and $\overline{OE} = V_{IH}$ ,<br>Address and Data stable |                           | 100  |                           | 100  | μA   |

† Measured with outputs open.

‡ Measured with a maximum of one address change while  $\overline{RAS} = V_{IL}$ .

§ Measured with a maximum of one address change while  $\overline{x}CAS = V_{IH}$ .

¶ For TMS426160P only.

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capacitance over recommended ranges of supply voltage and operating free-air temperature,  $f = 1$  MHz (see Note 3)

| PARAMETER |                                       | MIN | TYP | MAX | UNIT |
|-----------|---------------------------------------|-----|-----|-----|------|
| $C_i(A)$  | Input capacitance, address inputs     |     |     | 5   | pF   |
| $C_i(OE)$ | Input capacitance, output enable      |     |     | 7   | pF   |
| $C_i(RC)$ | Input capacitance, strobe inputs      |     |     | 7   | pF   |
| $C_i(W)$  | Input capacitance, write-enable input |     |     | 7   | pF   |
| $C_O$     | Output capacitance                    |     |     | 7   | pF   |

NOTE 3:  $V_{CC}$  equal to  $3.3\text{ V} \pm 0.3\text{ V}$  and the bias on pins under test is 0 V.

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**switching characteristics over recommended ranges of supply voltage and operating free-air temperature**

| PARAMETER   | '426160-70<br>'426160P-70 |     | '426160-80<br>'426160P-80 |     | UNIT |
|---|---------------------------|-----|---------------------------|-----|------|
|   | MIN                       | MAX | MIN                       | MAX |      |
| t <sub>CAC</sub> Access time from $\overline{\text{xCAS}}$ low                        | 18                        |     | 20                        |     | ns   |
| t <sub>AA</sub> Access time from column address                                       | 35                        |     | 40                        |     | ns   |
| t <sub>RAC</sub> Access time from $\overline{\text{RAS}}$ low                         | 70                        |     | 80                        |     | ns   |
| t <sub>OEa</sub> Access time from $\overline{\text{OE}}$ low                          | 18                        |     | 20                        |     | ns   |
| t <sub>CPA</sub> Access time from column precharge                                    | 40                        |     | 45                        |     | ns   |
| t <sub>CLZ</sub> Delay time, $\overline{\text{xCAS}}$ low to output in low Z          | 0                         |     | 0                         |     | ns   |
| t <sub>OH</sub> Output data hold time (from $\overline{\text{xCAS}}$ )                | 3                         |     | 3                         |     | ns   |
| t <sub>OH0</sub> Output data hold time (from $\overline{\text{OE}}$ )                 | 3                         |     | 3                         |     | ns   |
| t <sub>OFF</sub> Output disable time after $\overline{\text{xCAS}}$ high (see Note 4) | 0                         | 18  | 0                         | 20  | ns   |
| t <sub>OEZ</sub> Output disable time after $\overline{\text{OE}}$ high (see Note 4)   | 0                         | 18  | 0                         | 20  | ns   |

NOTE 4: t<sub>OFF</sub> and t<sub>OEZ</sub> are specified when the output is no longer driven.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 5)**

|   | '426160-70<br>'426160P-70 |         | '426160-80<br>'426160P-80 |         | UNIT |
|---|---------------------------|---------|---------------------------|---------|------|
|   | MIN                       | MAX     | MIN                       | MAX     |      |
| t <sub>RC</sub> Read cycle time (see Note 6)  | 130                       |         | 150                       |         | ns   |
| t <sub>WC</sub> Write cycle time  | 130                       |         | 150                       |         | ns   |
| t <sub>RWC</sub> Read-write/read-modify-write cycle time                                    | 181                       |         | 205                       |         | ns   |
| t <sub>PRWC</sub> Page-mode read-modify-write cycle time                                    | 96                        |         | 105                       |         | ns   |
| t <sub>RASP</sub> Page-mode pulse duration, $\overline{\text{RAS}}$ low (see Note 8)        | 70                        | 100 000 | 80                        | 100 000 | ns   |
| t <sub>RAS</sub> Non-page-mode pulse duration, $\overline{\text{RAS}}$ low (see Note 8)     | 70                        | 10 000  | 80                        | 10 000  | ns   |
| t <sub>CAS</sub> Pulse duration, $\overline{\text{xCAS}}$ low (see Note 9)                  | 18                        | 10 000  | 20                        | 10 000  | ns   |
| t <sub>CP</sub> Pulse duration, $\overline{\text{xCAS}}$ high (precharge)                   | 10                        |         | 10                        |         | ns   |
| t <sub>RP</sub> Pulse duration, $\overline{\text{RAS}}$ high (precharge)                    | 50                        |         | 60                        |         | ns   |
| t <sub>WP</sub> Write pulse duration  | 15                        |         | 15                        |         | ns   |
| t <sub>ASC</sub> Column-address setup time before $\overline{\text{xCAS}}$ low              | 0                         |         | 0                         |         | ns   |
| t <sub>ASR</sub> Row-address setup time before $\overline{\text{RAS}}$ low                  | 0                         |         | 0                         |         | ns   |
| t <sub>DS</sub> Data setup time before $\overline{\text{W}}$ low (see Note 10)              | 0                         |         | 0                         |         | ns   |
| t <sub>RCS</sub> Read setup time before $\overline{\text{xCAS}}$ low                        | 0                         |         | 0                         |         | ns   |
| t <sub>CWL</sub> $\overline{\text{W}}$ -low setup time before $\overline{\text{xCAS}}$ high | 18                        |         | 20                        |         | ns   |

NOTES: 5. Timing measurements are referenced to V<sub>IL</sub> max and V<sub>IH</sub> min.

6. All cycle times assume t<sub>T</sub> = 5 ns.

7. t<sub>PC</sub> > t<sub>CP</sub> min + t<sub>CAS</sub> min + 2t<sub>T</sub>.

8. In a read-modify-write cycle, t<sub>RWD</sub> and t<sub>RWL</sub> must be observed. Depending on the user's transition times, this may require additional  $\overline{\text{RAS}}$  low time (t<sub>RAS</sub>).

9. In a read-modify-write cycle, t<sub>CWD</sub> and t<sub>CWL</sub> must be observed. Depending on the user's transition times, this may require additional  $\overline{\text{xCAS}}$  low time (t<sub>CAS</sub>).

10. Reference to the first  $\overline{\text{xCAS}}$  or  $\overline{\text{W}}$ , whichever occurs last.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued) (see Note 5)

|   | '426160-70<br>'426160P-70 |     | '426160-80<br>'426160P-80 |     | UNIT |
|---|---------------------------|-----|---------------------------|-----|------|
|   | MIN                       | MAX | MIN                       | MAX |      |
| t <sub>RWL</sub> $\bar{W}$ -low setup time before $\bar{RAS}$ high              | 18                        |     | 20                        |     | ns   |
| t <sub>WCS</sub> $\bar{W}$ -low setup time before $\bar{x}CAS$ low              | 0                         |     | 0                         |     | ns   |
| t <sub>CAH</sub> Column-address hold time after $\bar{x}CAS$ low                | 15                        |     | 15                        |     | ns   |
| t <sub>DH</sub> Data hold time after $\bar{x}CAS$ low (see Note 10)             | 15                        |     | 15                        |     | ns   |
| t <sub>RAH</sub> Row-address hold time after $\bar{RAS}$ low                    | 10                        |     | 10                        |     | ns   |
| t <sub>RCH</sub> Read hold time after $\bar{x}CAS$ high (see Note 13)           | 0                         |     | 0                         |     | ns   |
| t <sub>RRH</sub> Read hold time after $\bar{RAS}$ high (see Note 13)            | 5                         |     | 5                         |     | ns   |
| t <sub>WCH</sub> Write hold time after $\bar{x}CAS$ low (see Note 12)           | 15                        |     | 15                        |     | ns   |
| t <sub>CLCH</sub> Hold time, $\bar{x}CAS$ low to $\bar{x}CAS$ high              | 5                         |     | 5                         |     | ns   |
| t <sub>AWD</sub> Delay time, column address to $\bar{W}$ low (see Note 14)      | 63                        |     | 70                        |     | ns   |
| t <sub>CHR</sub> Delay time, $\bar{RAS}$ low to $\bar{x}CAS$ high (see Note 11) | 20                        |     | 20                        |     | ns   |
| t <sub>CRP</sub> Delay time, $\bar{x}CAS$ high to $\bar{RAS}$ low               | 5                         |     | 5                         |     | ns   |
| t <sub>CSH</sub> Delay time, $\bar{RAS}$ low to $\bar{x}CAS$ high               | 70                        |     | 80                        |     | ns   |
| t <sub>CSR</sub> Delay time, $\bar{x}CAS$ low to $\bar{RAS}$ low (see Note 11)  | 10                        |     | 10                        |     | ns   |
| t <sub>CWD</sub> Delay time, $\bar{x}CAS$ low to $\bar{W}$ low (see Note 14)    | 46                        |     | 50                        |     | ns   |
| t <sub>OEH</sub> $\bar{OE}$ command hold time                                   | 18                        |     | 20                        |     | ns   |
| t <sub>OED</sub> Delay time, $\bar{OE}$ high before data at DQ                  | 18                        |     | 20                        |     | ns   |
| t <sub>ROH</sub> Delay time, $\bar{OE}$ low to $\bar{RAS}$ high                 | 10                        |     | 10                        |     | ns   |
| t <sub>RAD</sub> Delay time, $\bar{RAS}$ low to column address (see Note 15)    | 15                        | 35  | 15                        | 40  | ns   |
| t <sub>RAL</sub> Delay time, column address to $\bar{RAS}$ high                 | 35                        |     | 40                        |     | ns   |
| t <sub>CAL</sub> Delay time, column address to $\bar{x}CAS$ high                | 35                        |     | 40                        |     | ns   |
| t <sub>RCD</sub> Delay time, $\bar{RAS}$ low to $\bar{x}CAS$ low (see Note 15)  | 20                        | 52  | 20                        | 60  | ns   |
| t <sub>RPC</sub> Delay time, $\bar{RAS}$ high to $\bar{x}CAS$ low               | 0                         |     | 0                         |     | ns   |
| t <sub>RSH</sub> Delay time, $\bar{x}CAS$ low to $\bar{RAS}$ high               | 18                        |     | 20                        |     | ns   |
| t <sub>RWD</sub> Delay time, $\bar{RAS}$ low to $\bar{W}$ low (see Note 14)     | 98                        |     | 110                       |     | ns   |
| t <sub>CPW</sub> Delay time, $\bar{W}$ from $\bar{x}CAS$ precharge              | 68                        |     | 75                        |     | ns   |
| t <sub>CPRH</sub> $\bar{RAS}$ hold time from $\bar{x}CAS$ precharge             | 40                        |     | 45                        |     | ns   |
| t <sub>CPR</sub> $\bar{x}CAS$ precharge before self refresh                     | 0                         |     | 0                         |     | ns   |
| t <sub>RPS</sub> $\bar{RAS}$ precharge after self refresh                       | 130                       |     | 150                       |     | ns   |

- NOTES: 5. Timing measurements are referenced to  $V_{IL}$  max and  $V_{IH}$  min.  
10. Reference to the first  $\bar{x}CAS$  or  $\bar{W}$ , whichever occurs last.  
11.  $\bar{x}CAS$ -before- $\bar{RAS}$  refresh only.  
12. Early write operation only.  
13. Either t<sub>RRH</sub> or t<sub>RCH</sub> must be satisfied for a read cycle.  
14. Read-modify-write operation only.  
15. Maximum value specified only to assure access time.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded) (see Note 5)

|  | '426160-70<br>'426160P-70 |     | '426160-80<br>'426160P-80 |     | UNIT    |
|--|---------------------------|-----|---------------------------|-----|---------|
|  | MIN                       | MAX | MIN                       | MAX |         |
| $t_{RASS}$ Self refresh entry from $\overline{RAS}$ low                              | 100                       |     | 100                       |     | $\mu$ s |
| $t_{CHS}$ $\overline{xCAS}$ low hold time after $\overline{RAS}$ high (self refresh) | - 50                      |     | - 50                      |     | ns      |
| $t_{REF}$ Refresh time interval (TMS426160)  |                           | 64  |                           | 64  | ms      |
| $t_{REF}$ Refresh time interval, low power (TMS426160P only)                         |                           | 512 |                           | 512 | ms      |
| $t_T$ Transition time  | 3                         | 30  | 3                         | 30  | ns      |

NOTE 5: Timing measurements are referenced to  $V_{IL}$  max and  $V_{IH}$  min.

### PARAMETER MEASUREMENT INFORMATION

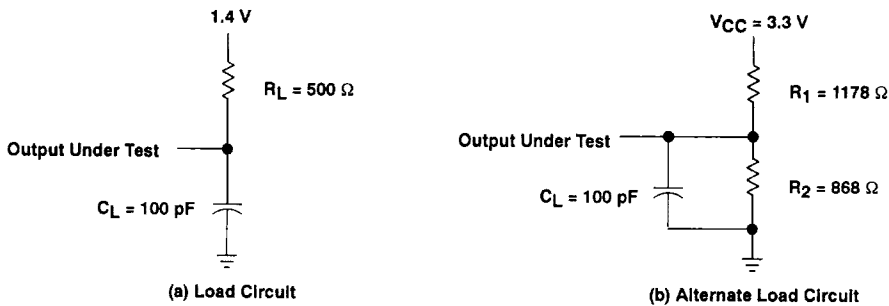
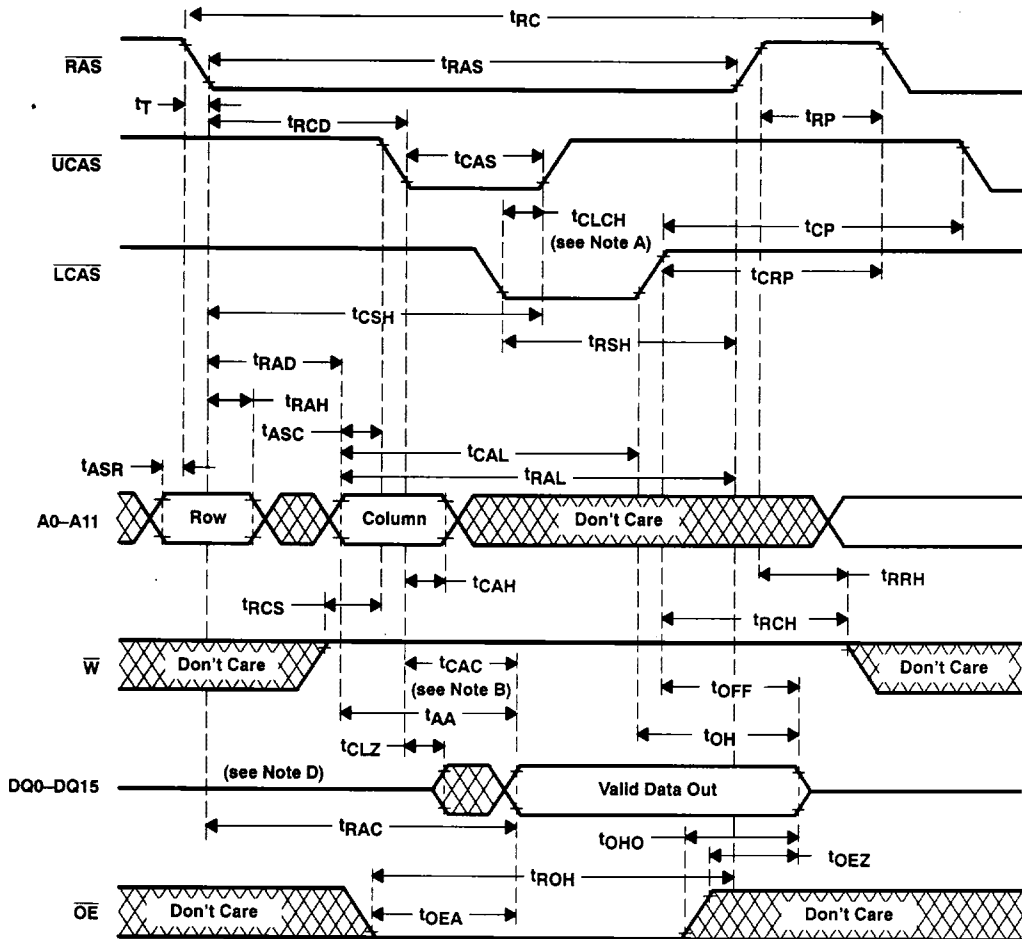


Figure 1. Load Circuits for Timing Parameters

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PARAMETER MEASUREMENT INFORMATION

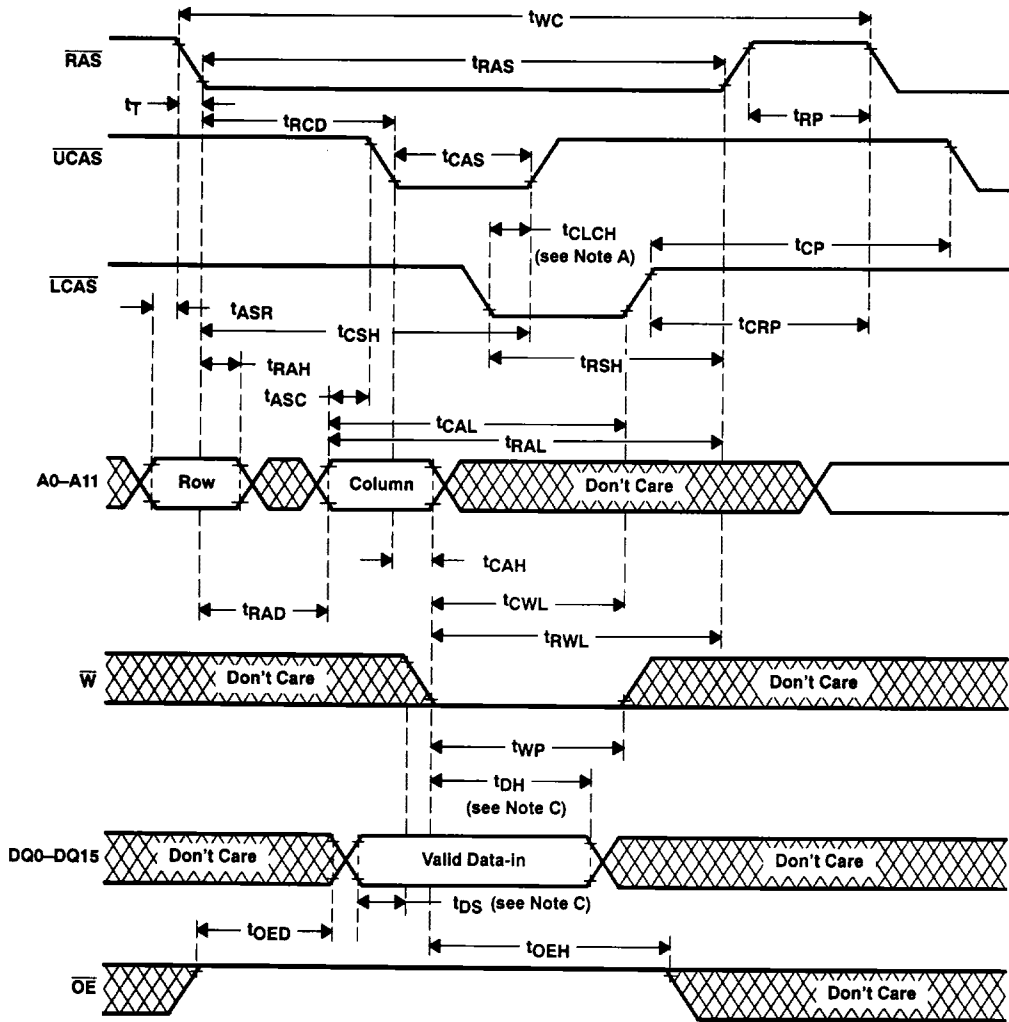


- NOTES: A. In order to hold the address latched by the first  $\overline{xCAS}$  going low, the parameter  $t_{CLCH}$  must be met.  
 B.  $t_{CAC}$  is measured from  $\overline{xCAS}$  to its corresponding DQx.  
 C.  $\overline{xCAS}$  order is arbitrary.  
 D. Output may go from high-impedance to an invalid data state prior to the specified access time.

Figure 2. Read Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

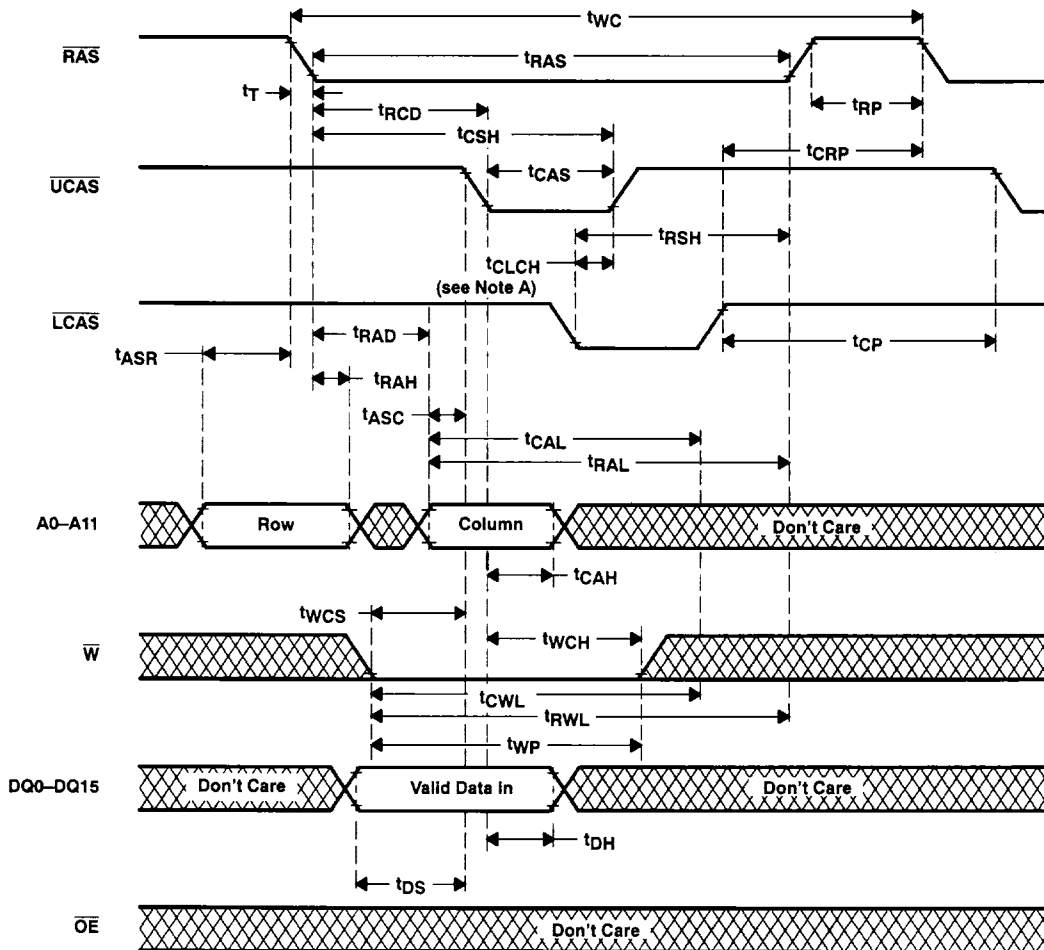


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- NOTES: A. In order to hold the address latched by the first  $\overline{x}CAS$  going low, the parameter  $t_{CLCH}$  must be met.  
 B.  $\overline{x}CAS$  order is arbitrary.  
 C. Reference to the first  $\overline{x}CAS$  or  $\overline{W}$ , whichever occurs last.

Figure 3. Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

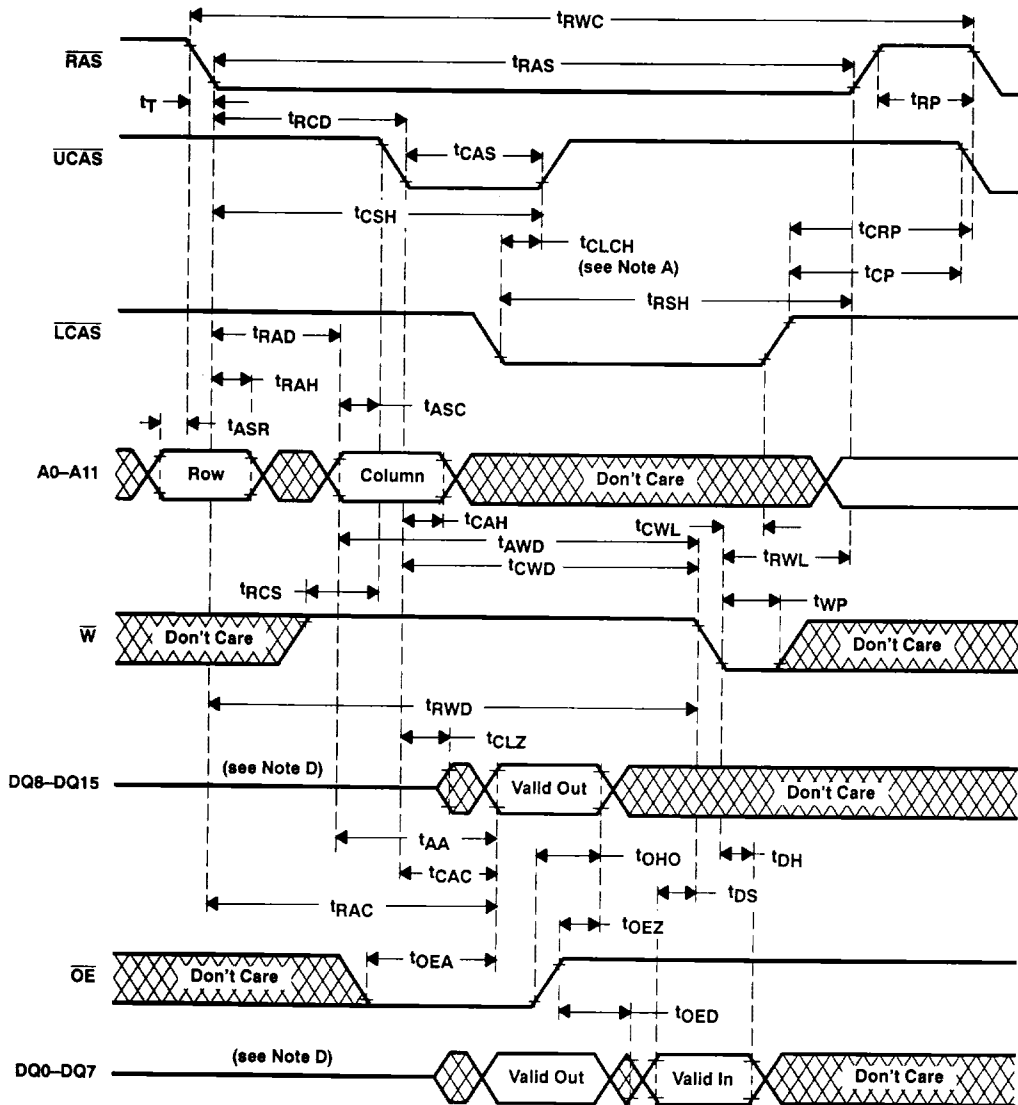


NOTES: A. In order to hold the address latched by the first  $\overline{x}CAS$  going low, the parameter  $t_{CLCH}$  must be met.  
 B.  $\overline{x}CAS$  order is arbitrary.

Figure 4. Early Write Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

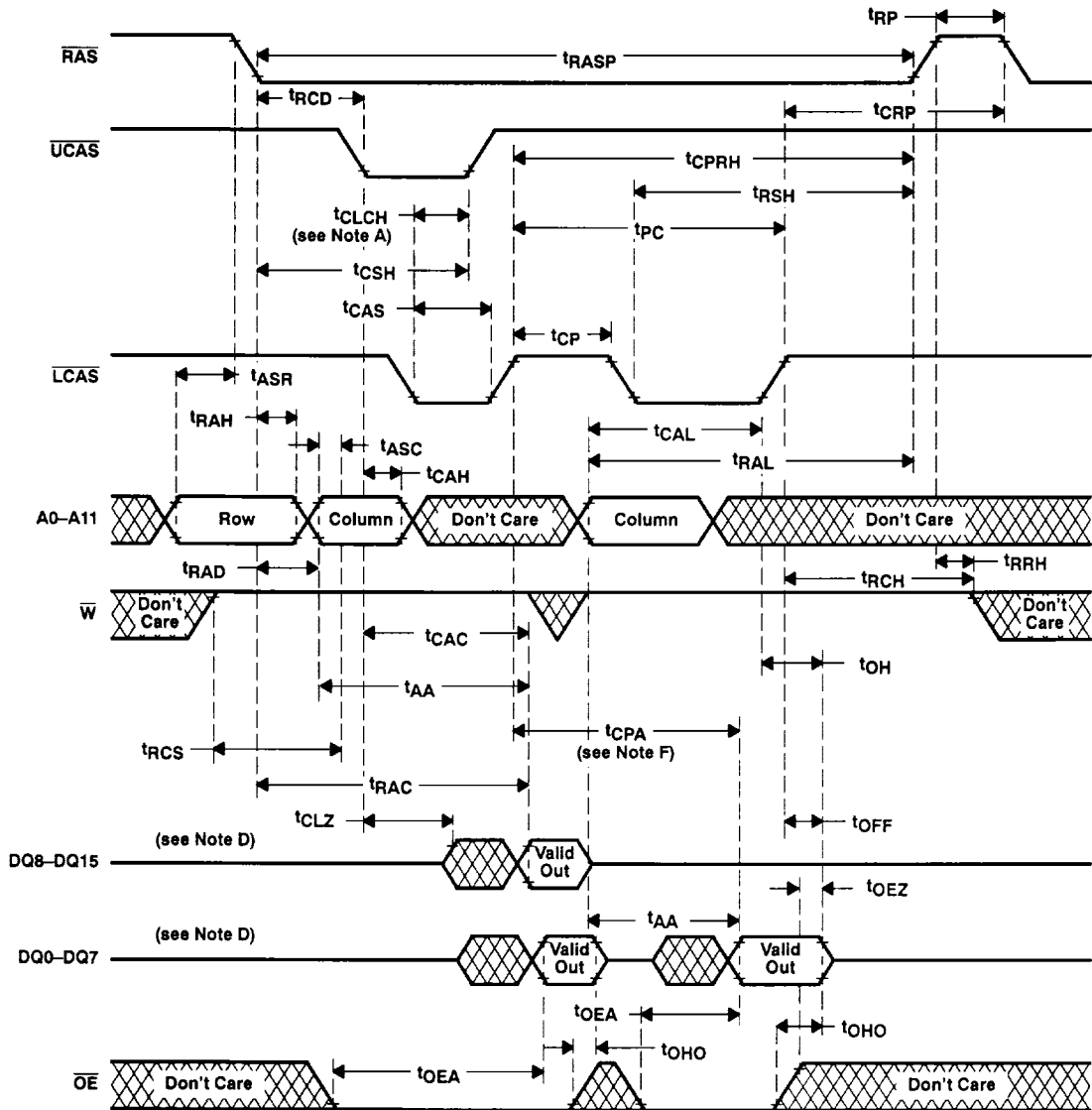


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- NOTES: A. In order to hold the address latched by the first xCAS going low, the parameter  $t_{CLCH}$  must be met.  
 B. xCAS order is arbitrary.  
 C.  $t_{CAC}$  is measured from xCAS to its corresponding DQx.  
 D. Output might go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 5. Read-Modify-Write Cycle Timing

**PARAMETER MEASUREMENT INFORMATION**



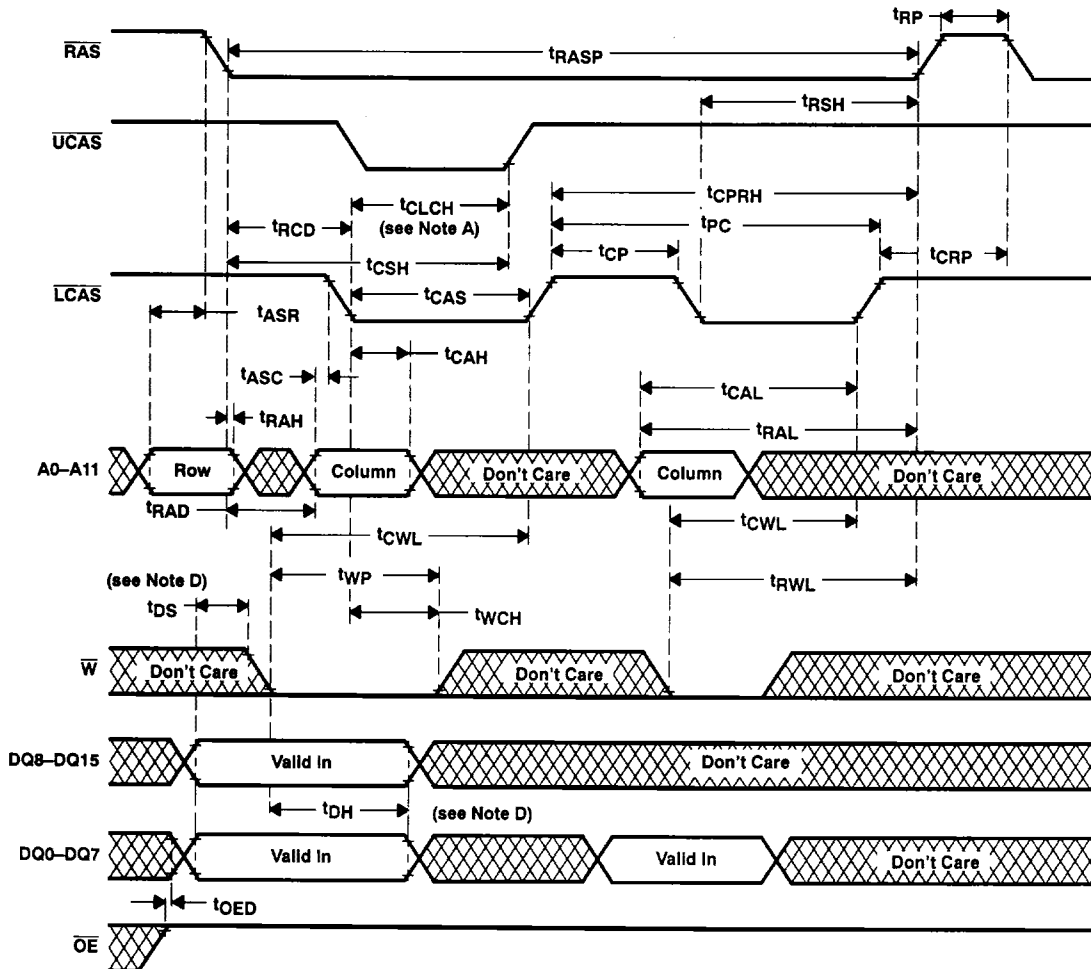
- NOTES:
- In order to hold the address latched by the first  $\overline{x}CAS$  going low, the parameter  $t_{CLCH}$  must be met.
  - $t_{CAC}$  is measured from  $\overline{x}CAS$  to its corresponding  $DQx$ .
  - $\overline{x}CAS$  order is arbitrary.
  - Output may go from high-impedance to an invalid data state prior to the specified access time.
  - A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
  - Access time is  $t_{CPA}$  or  $t_{AA}$  dependent.

**Figure 6. Enhanced Page-Mode Read Cycle Timing**

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PARAMETER MEASUREMENT INFORMATION

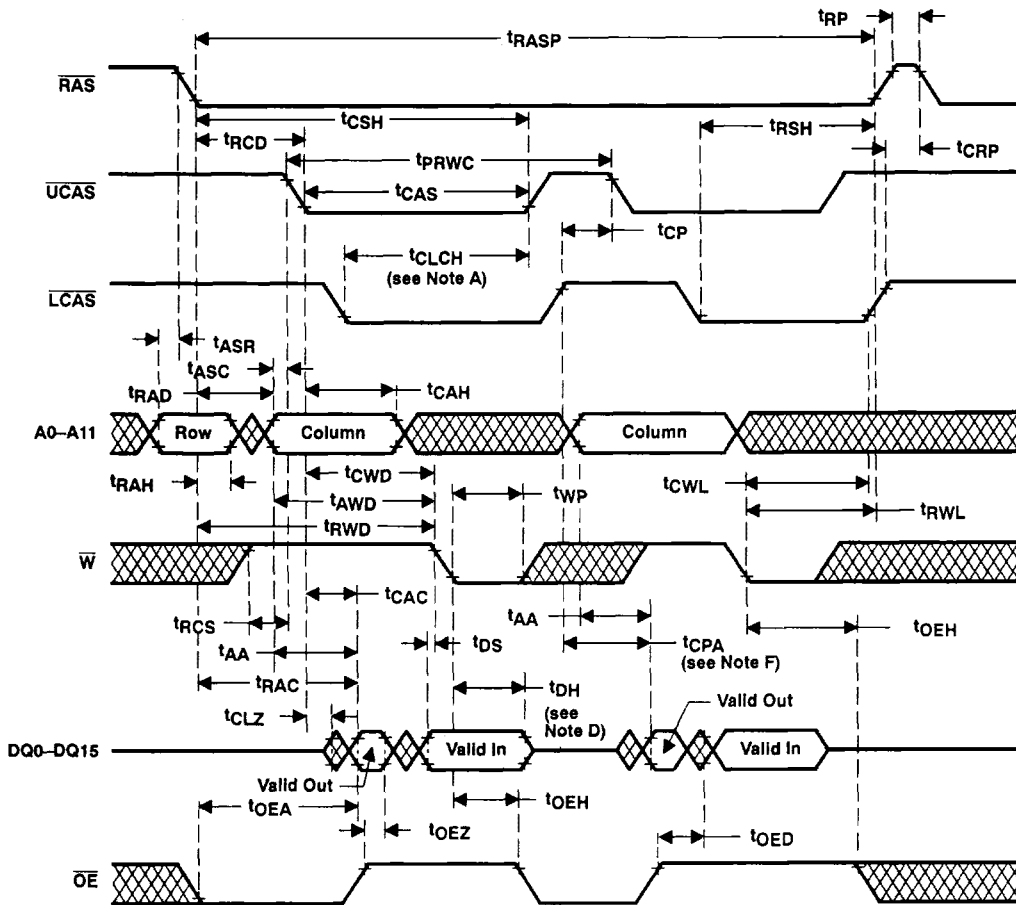


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- NOTES: A. In order to hold the address latched by the first  $\overline{x}CAS$  going low, the parameter  $t_{CLCH}$  must be met.  
 B.  $\overline{x}CAS$  order is arbitrary.  
 C. A read cycle or read-modify-write cycle can be mixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.  
 D. Referenced to the first  $\overline{x}CAS$  or  $\overline{W}$ , whichever occurs last.

Figure 7. Enhanced Page-Mode Write Cycle Timing

**PARAMETER MEASUREMENT INFORMATION**

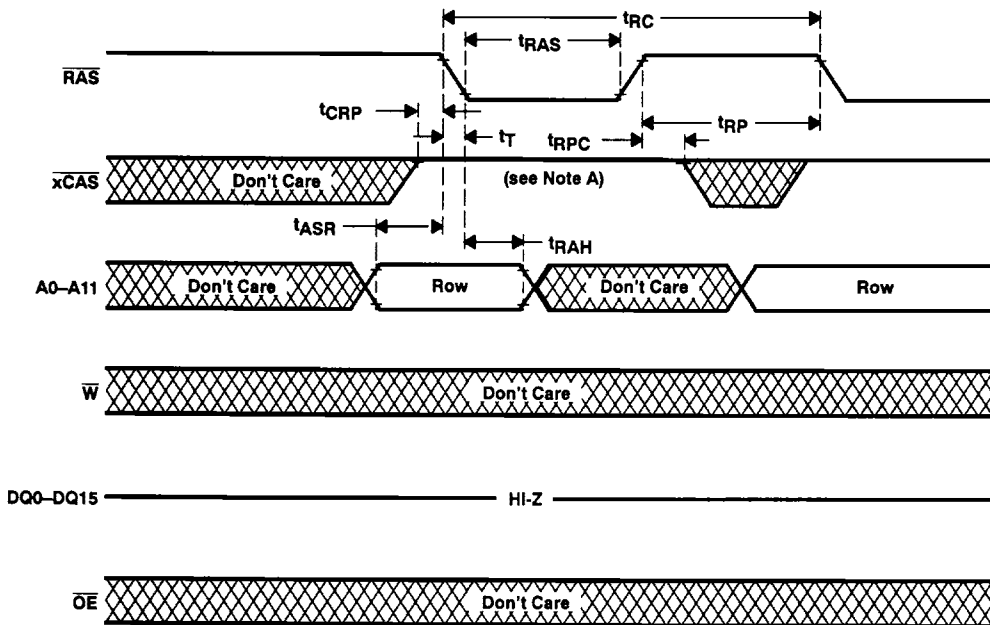


- NOTES: A. In order to hold the address latched by the first  $\overline{x}CAS$  going low, the parameter  $t_{CLCH}$  must be met.  
 B.  $t_{CAC}$  is measured from  $\overline{x}CAS$  to its corresponding DQx.  
 C.  $\overline{x}CAS$  order is arbitrary.  
 D. Output may go from high-impedance to an invalid data state prior to the specified access time.  
 E. A read or write cycle can be intermixed with read-modify-write cycles as long as the read and write cycle timing specifications are not violated.  
 F. Access time is  $t_{CPA}$  or  $t_{AA}$  dependent.

**Figure 8. Enhanced Page-Mode Read-Modify-Write Cycle Timing**

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PARAMETER MEASUREMENT INFORMATION



NOTE A: All  $\overline{xCAS}$  must be high.

Figure 9.  $\overline{RAS}$ -Only Refresh Timing

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PARAMETER MEASUREMENT INFORMATION

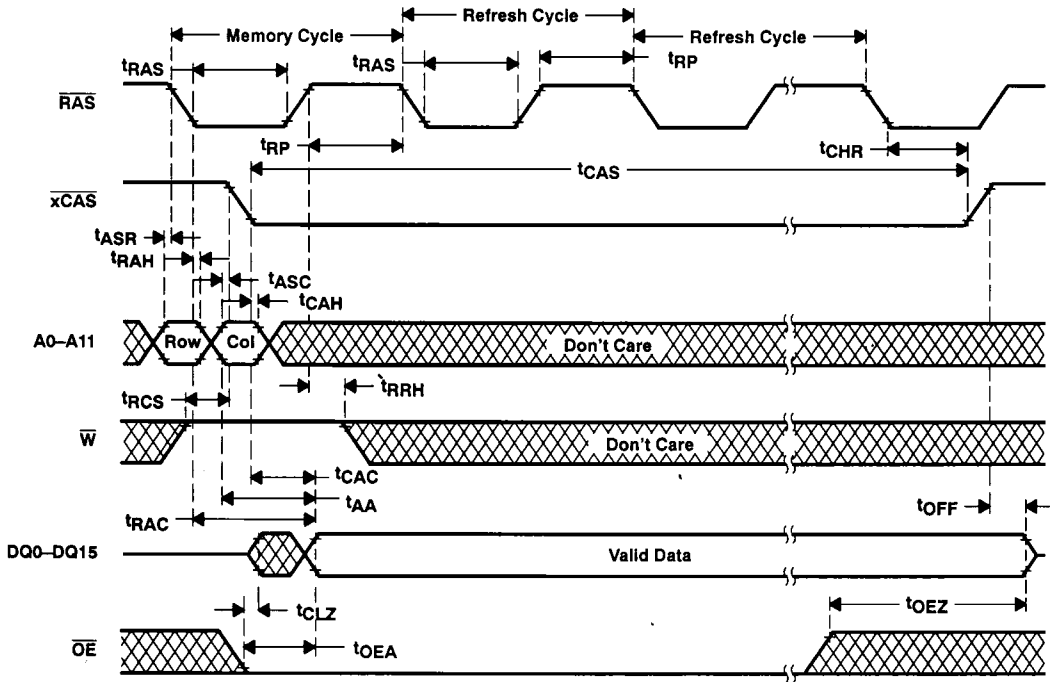
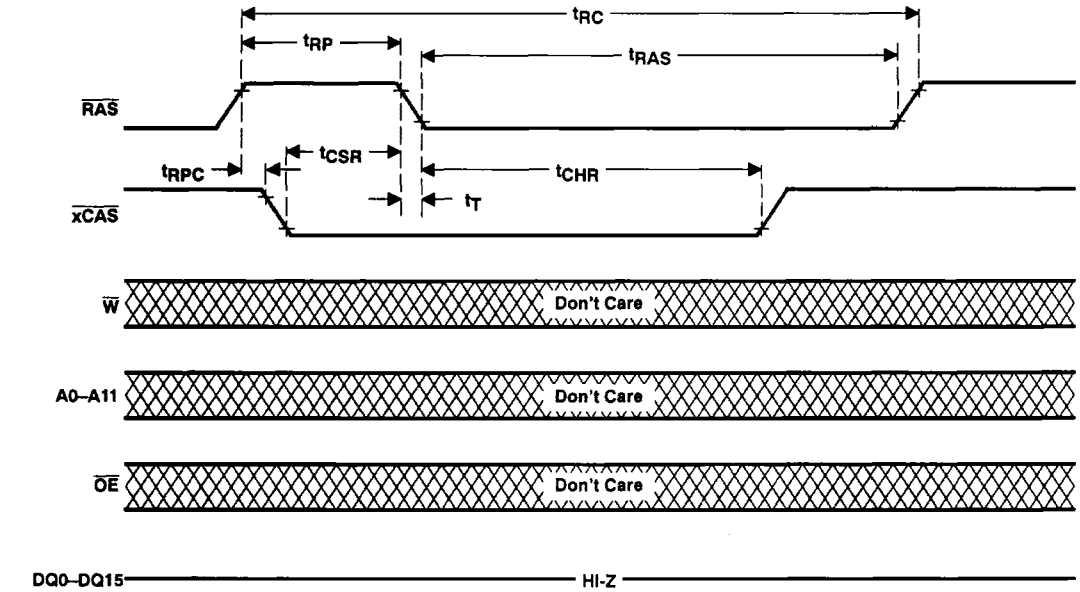


Figure 10. Hidden Refresh Cycle Timing

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**PARAMETER MEASUREMENT INFORMATION**



NOTES: A. Any  $\overline{\text{xCAS}}$  may be used.

**Figure 11. Automatic (CAS-Before-RAS) Refresh Cycle Timing**

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**PARAMETER MEASUREMENT INFORMATION**

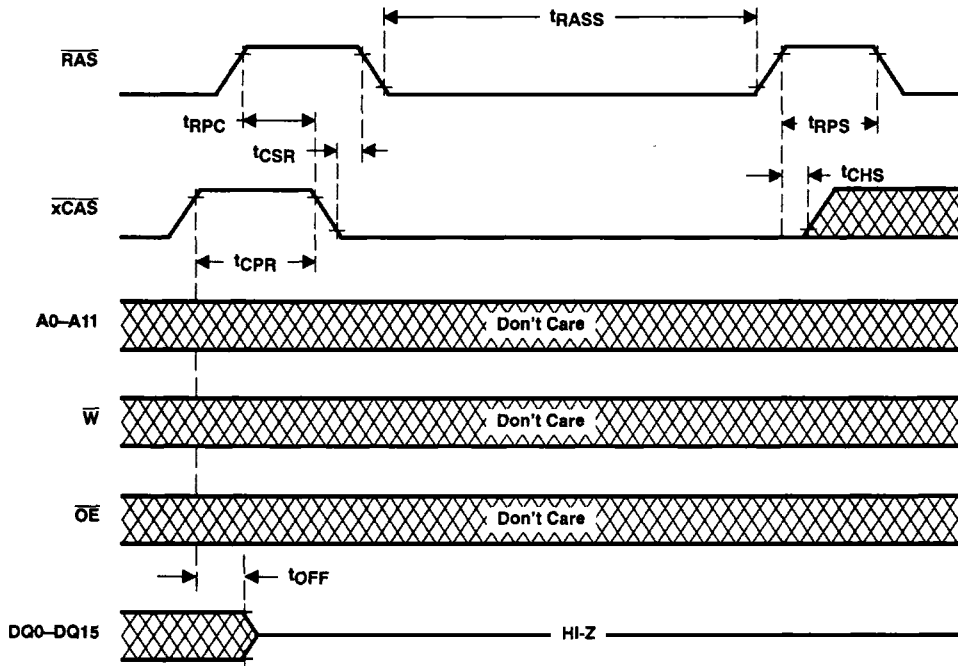


Figure 12. Self Refresh Timing

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device symbolization

