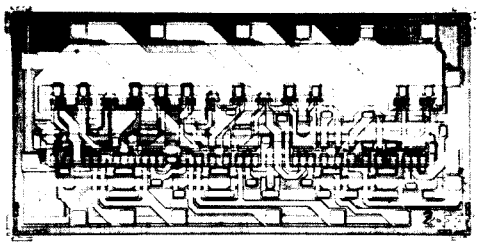
ECL2500 SERIES EMITTER-COUPLED-LOGIC (ECL) BISTABLE MODULES FOR APPLICATION IN ULTRA-HIGH-SPEED DIGITAL SYSTEMS

description

The ECL2500 series is a compatible family of ECL functions with basic gate delays of 2 to 3 ns per stage. The family is specifically designed for operation from 0°C to 70°C.

The ECL2500 family includes:



- Basic Gate Modules
- Multifunction Gate Modules
- **Bistable Modules**
- Arithmetic Modules
- Interface Modules
- Memory Module

family features

- High speed . . . typical gate propagation delay time of 2.5 ns
- Complementary OR/NOR outputs with capability for wired-OR connections
- Designed for use with transmission lines to ensure maximum signal transmission without noise. Characterized for 50-ohm lines
- High noise immunity: ±225 mV typical at 25°C

This data sheet covers the bistable modules.
Separate data sheets cover the balance of the ECL2500 modules.

ECL2500 series bistable modules

The ECL2500 series bistable modules are summarized in the table below. These modules contain the ECL circuits shown in the schematics of Figures A, B, and C on pages 6 and 7. Logic diagrams of ECL2540 through ECL2542 are shown on page 4.

SUMMARY OF BISTABLE MODULES

MODULE	GATES PER MODULE	LATCHES PER MODULE	OUTPUTS PER BISTABLE CIRCUIT	
			Q (LATCH)	$\overline{Q}$ (LATCH COMPLEMENT)
ECL2540	4	2	1	1
ECL2541	9	2	1	2
ECL2542	13	2		1

APPLICATION INFORMATION

general

The bistable modules specified in this data sheet contain dual latches. Each half of the ECL2540 is a latch with a separate data input. Two clock inputs, C and C′, feed both latches. Q and $\overline{Q}$ outputs are provided from each latch. Each half of the ECL2541 is a latch with additional circuitry which provides a data input and a gate input to control the input data. Common clock, set, and reset inputs are included. One Q and two $\overline{Q}$ outputs are provided for each latch. Each half of the ECL2542 is a latch with additional circuitry which provides two data inputs each with a gate input to control the input data. Common clock, set, and reset inputs serve both latches. Only $\overline{Q}$ outputs are provided.

Each latch has the possibility to operate in the following modes:

Register – The mode in which the data input controls the state of the latch. Q is high when data is high.

Storage – The mode in which the latch stores data received during the register mode. Input data is locked out from changing the latch state.

Set – The mode whereby Q is set high (or $\overline{Q}$ low) which is normally done when the clock is high.

Reset – The mode whereby Q is set low (or $\overline{Q}$ high) which is normally done when the clock is high (low for ECL2540).

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The ECL2541 and ECL2542 have the register mode subdivided:

Register Mode/Clock Control – The mode whereby the gate input is low, allowing the data to set the latch when the clock goes low.

Register Mode/Gate Control – The mode whereby the clock input is low, allowing the data to set the latch when the gate is low.

Each Q and $\overline{Q}$ output must be terminated in a pull-down resistor.

The Q terminal of the ECL2541 must have a termination resistor (in addition to the pull-down resistor) on the output at all times (whether the output is used for fan-out or not), because internal feedback occurs from this point.

For full-temperature-range operation of all devices, data must be present before the clock pulse and the minimum width of the clock pulse is 4.5 ns. For the ECL2541 and ECL2542, the data pulse must extend beyond the clock pulse to allow for the delay associated with the clock-buffering gate.

For the ECL2540, latching occurs on either the leading or trailing edge of the C or C′ pulse. For the ECL2541 and ECL2542, latching occurs on the leading edge of the clock pulse.

Multiple V_{CC} terminals have been supplied to reduce crosstalk noise. All V_{CC} terminals should be connected even if all gates in a module are not used.

General loading for fan-out may be divided into two classes:

CLASS I **Short-Line or Cluster Loading.**
Loads which can be connected within two inches of any source can be treated as lumped capacitive loads which include the gate inputs and stub-line capacitances. Switching times can be interpolated accordingly. No two dotted outputs can be more than two inches apart for this case.

CLASS II **Long-Line or Distributive Loading.**
These loads must be treated as lumped loads along a transmission line and termination should be at the end of the transmission chain. No more than 20 pF of load is recommended per 4.5 inches of 50-ohm printed line (with dielectric constant of 4.5) in order that the reflection coefficient be no greater than 20%. If the loads are lumped loads of 20 pF, they must be 4.5 inches apart. If individual gates and **CLASS I** loads are distributed, they must not exceed the 20 pF per 4.5 inches of line.

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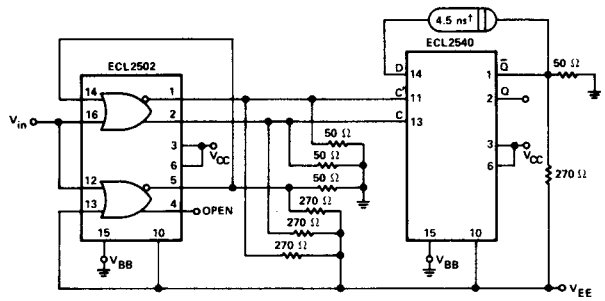
APPLICATION INFORMATION

ECL2540

The ECL2540 requires two clock inputs. Faulty operation occurs if the C′ input lags behind C by more than 0.5 ns. The interval between the transition of the two clocks is referred to as skew. C′ can be skewed ahead of C by as much as 1.5 ns.

The ECL2540 can be used as a toggle as shown in Figure 1. However, the delay from $\overline{Q}$ to D must be greater than the clock pulse width. Thus, when pulse widths are very long, this becomes impractical unless a technique such as that shown in Figure 1 is used. This technique uses two gates of an ECL2502 as a pulse-shaping network to allow operation of a toggle from 100 megacycles per second down to cycles per second.



†Delay between $\overline{Q}$ and D must be greater than 4.5 ns based on the propagation delay characteristics of the ECL2502 and its feedback loop.

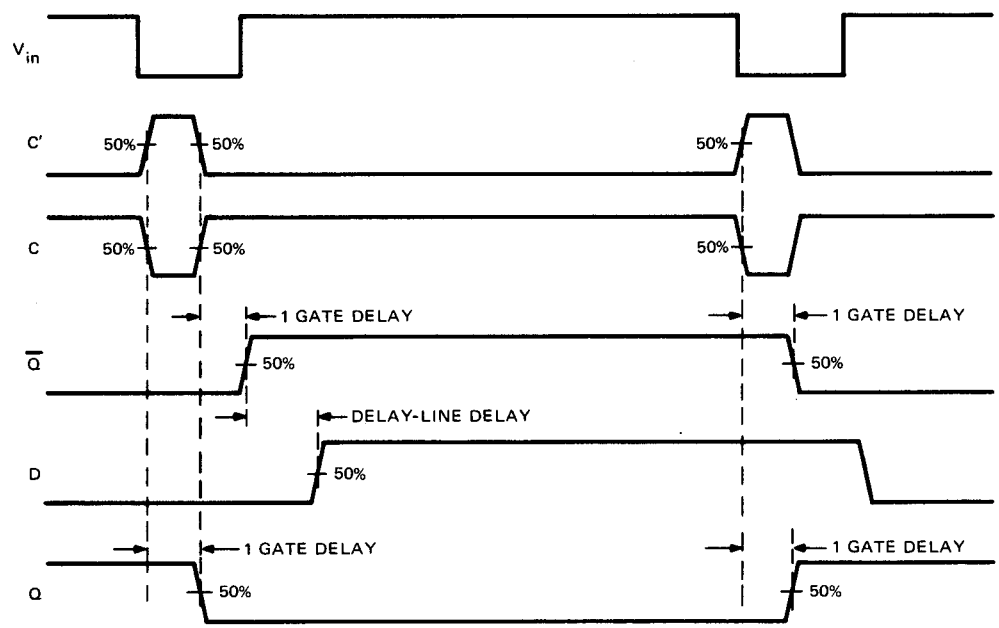
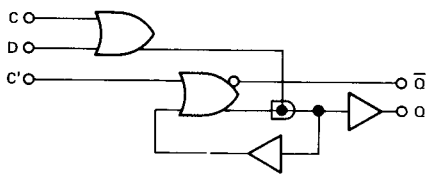


FIGURE 1—ECL2540 USED AS A TOGGLE (WITHOUT SKEW)

logic†

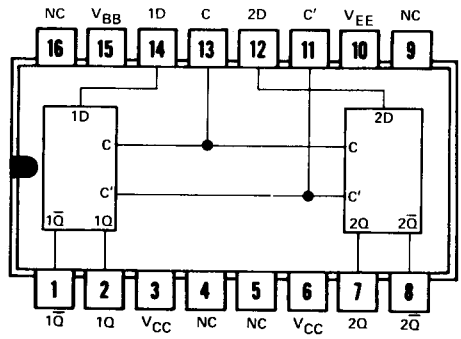
ECL2540



$Q_{n+1} = (C+D)(Q_n+C')$

$\bar{Q}_{n+1} = (\bar{C}\bar{D}+\bar{Q}_n)\bar{C}'$

NC—No internal connection



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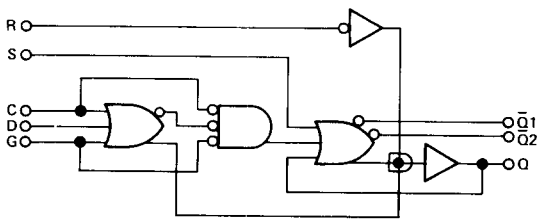
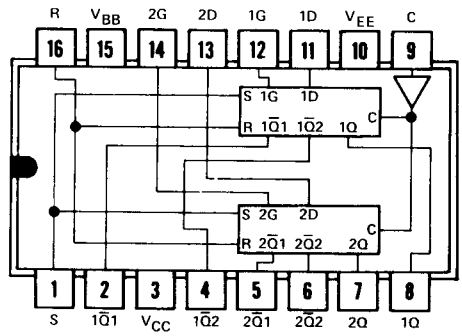
ECL2541

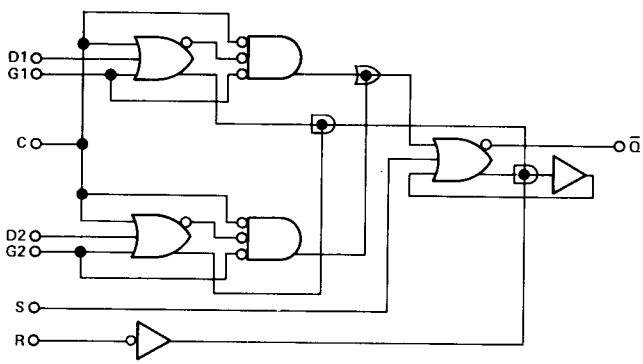


$Q_{n+1} = \bar{R}[(C+D+G)(Q_n+S)+\bar{C}D\bar{G}]$

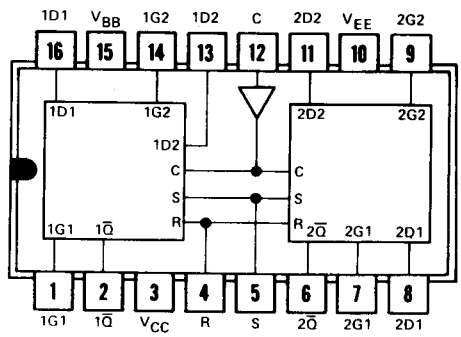
$\bar{Q}_{n+1} = \bar{S}(C+\bar{D}+G)(\bar{Q}_n+R+\bar{C}\bar{D}\bar{G})$



ECL2542



$\bar{Q}_{n+1} = \bar{S}[C+(\bar{D}1+G1)(\bar{D}2+G2)]\,[\bar{Q}_n+R+\bar{C}(\bar{D}1\bar{G}1+\bar{D}2\bar{G}2)]$



†One half of each bistable module is shown in the logic diagrams.

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truth tables (for this series, H = positive voltage, L = negative voltage, X = irrelevant)

ECL2540

MODE	INPUTS			OUTPUTS	
	CLOCK		DATA	LATCH	LATCH COMPLEMENT
	C	C′	D	Q_{n+1}	$\overline{Q}_{n+1}$
Register	L	H	H	H	L
	L	H	L	L	(L)†
Clock-controlled storage	H	L	X	Q_n	$\overline{Q}_n$
Set	H	H	X	H	L
Reset	L	L	L	L	H
Forbidden (see Note 1)	L	L	H	Q_n	$\overline{Q}_n$

ECL2541

MODE	INPUTS					OUTPUTS	
	SET	RESET	CLOCK	GATE	DATA	LATCH	LATCH COMPLEMENT
	S	R	C	G	D	Q_{n+1}	$\overline{Q}_{n+1}$
Register	L	L	L	L	H	H	L
	L	L	L	L	L	L	H
Clock-controlled storage	L	L	H	X	X	Q_n	$\overline{Q}_n$
Gate-controlled storage	L	L	X	H	X	Q_n	$\overline{Q}_n$
Set	H	L	H	X	X	H	L
	H	L	X	H	X	H	L
Reset	L	H	H	X	X	L	H
	L	H	X	H	X	L	H
Forbidden	H	L	L	L	H	H	L
	H	L	L	L	L	L	L
	L	H	L	L	H	L	L
	L	H	L	L	L	L	H
	H	H	X	X	X	L	L

ECL2542

MODE	INPUTS							OUTPUT
	SET	RESET	CLOCK	GATE		DATA		LATCH COMPLEMENT
	S	R	C	G1	G2	D1	D2	$\overline{Q}_{n+1}$
Register	L	L	L	H	L	X	D2	$\overline{D2}$
	L	L	L	L	H	D1	X	$\overline{D1}$
	L	L	L	L	L	D1	D2	$\overline{D1 + D2}$
Clock-controlled storage	L	L	H	X	X	X	X	$\overline{Q}_n$
Gate-controlled storage	L	L	X	H	H	X	X	$\overline{Q}_n$
Set	H	L	H	X	X	X	X	L
	H	L	X	H	H	X	X	L
Reset	L	H	H	X	X	X	X	H
	L	H	X	H	H	X	X	H
Forbidden	H	L	L	L	X	X	X	See Note 2
	H	L	L	X	L	X	X	
	L	H	L	L	X	X	X	
	L	H	L	X	L	X	X	
	H	H	X	X	X	X	X	

†$\overline{Q}$ is made low by C′ being high. When C′ returns to its normal state (low) following the clock pulse, $\overline{Q}$ goes high (the complement of data).

NOTES: 1. This condition is data-controlled storage, whereas only clock-controlled storage is desired in the ECL2540. Hence, this condition is placed in the forbidden category.
2. The forbidden input combinations for ECL2542 may produce pseudo-stable output states which do not persist when a storage mode is subsequently selected or may produce outputs not in harmony with the normally used input patterns.

schematics

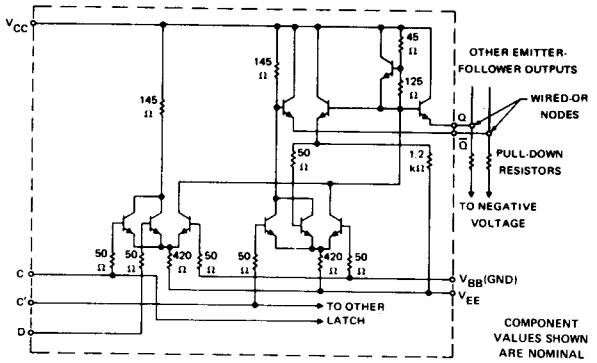

FIGURE A–SCHEMATIC OF HALF OF ECL2540

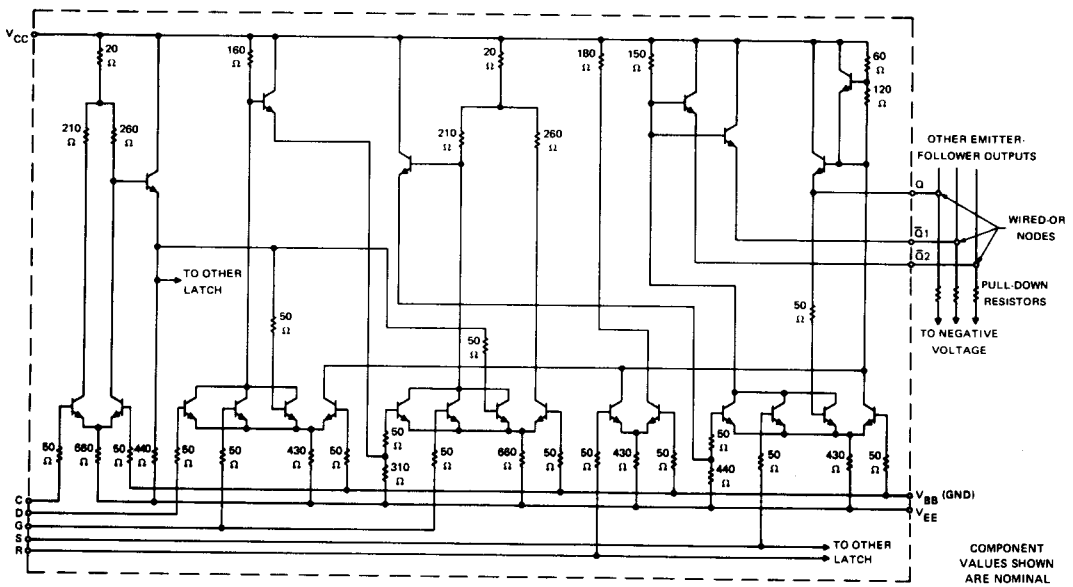

FIGURE B–SCHEMATIC OF HALF OF ECL2541

Emitter-follower outputs require an external pull-down resistor. The wired-OR function can be obtained by connecting the emitter-follower outputs of a bistable module to the emitter-follower outputs of other gates or other bistable modules. Only one pull-down resistor is required for each wire-OR node.

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schematic

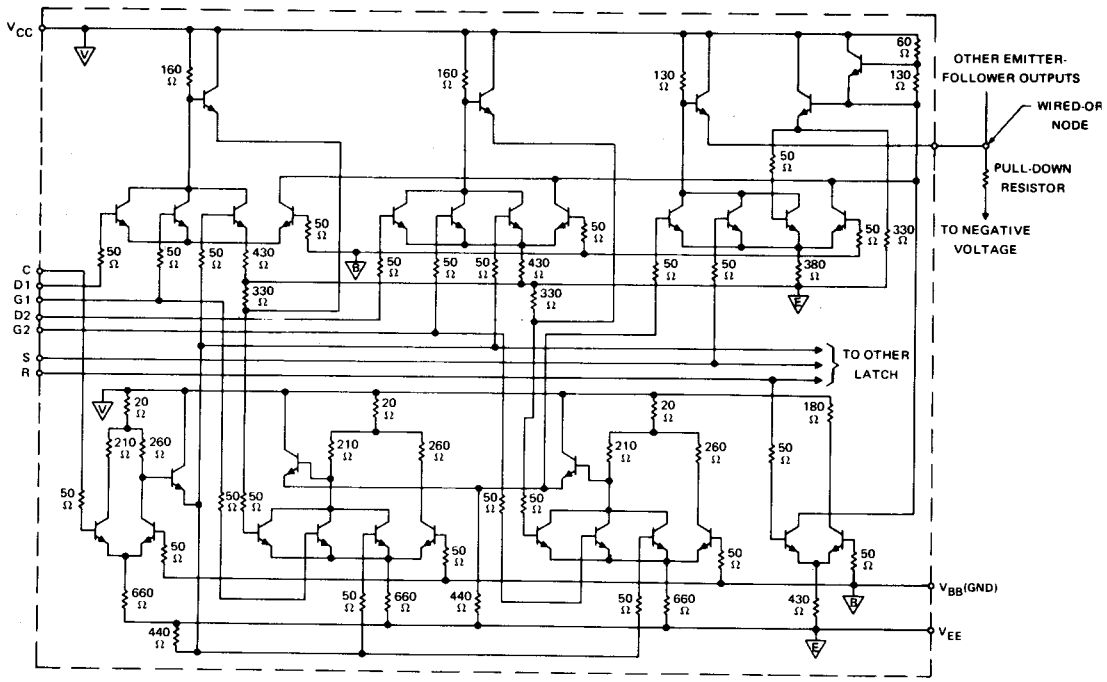

FIGURE C–SCHEMATIC OF HALF OF ECL2542

COMPONENT VALUES SHOWN ARE NOMINAL

▽ –V_{CC} bus
▽ –V_{BB} bus
▽ –V_{EE} bus (substrate)

4

absolute maximum ratings (see note 3)

Terminal voltages and currents	See table below
Storage temperature range	−40°C to 150°C
Free-air temperature range with supply and bias voltages applied	−40°C to 100°C

TERMINAL VOLTAGE AND/OR CURRENT, T_A = 0°C TO 75°C (SEE NOTES 4 AND 5)

TERMINAL	REMARKS	VOLTAGE		CURRENT
		CONTINUOUS	20-μs SURGE	
V_{CC}		2 V	4.5 V	
V_{EE}		−4 V	−7 V	
Each Input	All other inputs open	−3.5 V	−4 V	
		2 V	2 V	
Output Q	At high level			−40 mA
Output $\overline{Q}$	At high level			−40 mA

4

recommended operating conditions

Supply voltage V_{CC}	1.32 V ± 2%
Supply voltage V_{EE}	−3.2 V ± 2%
Reference voltage V_{BB}	0 V (GND)
Reverse bias on unused inputs	−1 V ± 0.5 V
Normalized d-c fan-out	0 to 35
Load on each output	characterized at 270 Ω to V_{EE}, 50 Ω to GND
Operating free-air temperature range	0°C to 75°C

NOTES: 3. Absolute maximum ratings are limits beyond which the life of individual devices may be impaired and are never to be exceeded in service or testing.
4. Maximum terminal conditions must be considered as mutually exclusive.
5. All voltages are referenced to V_{BB}, which is at GND.

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ECL2540 electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS*								MIN	TYP	MAX	UNIT
		TEST FIGURE	INITIAL CONDITIONS (SEE TABLE I)	VOLTAGE AT INPUT UNDER TEST	INPUT(S) UNDER TEST	OTHER INPUT TERMINALS 0.5 V	OTHER INPUT TERMINALS −0.5 V	OUTPUT TERMINAL Q	OUTPUT TERMINAL $\bar{Q}$	T_A	(SEE NOTE 6)		
V_{IH}	High-level input voltage									0°C	150	720	mV
										25°C	150	720	
										75°C	150	720	
V_{IL}	Low-level input voltage									0°C	−1500	−150	mV
										25°C	−1500	−150	
										75°C	−1500	−150	
$V_{OH(Q)}$	High-level output voltage at Q output, register mode	4	X	0.2 V	14	11	13	2		0°C	280		mV
										25°C	315		
					12	11	13	7		75°C			
$V_{OL(Q)}$	Low-level output voltage at Q output, register mode	4	X	−0.2 V	14	11	13	2		0°C			mV
										25°C		−330	
					12	11	13	7		75°C		−210	
$V_{OH(Q)}$	High-level output voltage at Q output, storage mode	4	S	0.2 V	13		11, 14	2		0°C	280	365	mV
										25°C	315	400 500	
					13		11, 12	7		75°C		470 580	
$V_{OL(Q)}$	Low-level output voltage at Q output, storage mode	4	R	−0.2 V	11	13, 14		2		0°C	−505	−440	mV
										25°C	−480	−400 −330	
					11	13, 12		7		75°C		−280 −210	
$V_{OH(\bar{Q})}$	High-level output voltage at $\bar{Q}$ output, storage mode	4	R	−0.2 V	11	13, 14			1	0°C	280	365	mV
										25°C	315	400 500	
					11	13, 12			8	75°C		470 580	
$V_{OL(\bar{Q})}$	Low-level output voltage at $\bar{Q}$ output, storage mode	4	S	0.2 V	13		11, 14		1	0°C	−505	−440	mV
										25°C	−490	−425 −350	
					13		11, 12		8	75°C		−390 −315	
$V_{OH(Q)}$	High-level output voltage at Q output, set mode	4	R	0.2 V	11, 13		14	2		0°C	280		mV
										25°C	315		
					11, 13		12	7		75°C			
$V_{OL(Q)}$	Low-level output voltage at Q output, reset mode	4	S	−0.2 V	11, 13		14	2		0°C			mV
										25°C		−330	
					11, 13		12	7		75°C		−210	
I_{IH}	High-level input current	5	X	0.5 V	14		11, 12, 13			0°C		255	μA
										25°C		235	
					12		11, 13, 14			75°C		200	
			X	0.5 V	11		12, 13, 14			0°C		510	μA
										25°C		470	
					13		11, 12, 14			75°C		400	
I_{IL}	Low-level input current	6	X	All inputs in parallel at −3.2 V						0°C		−0.5	μA
										25°C		−0.5	
										75°C		−0.6	
I_{CC} or $-I_{EE}$	Supply current	7	X	All inputs in parallel at −0.5 V						25°C	20	34	mA
C_{in}	Input capacitance (see Note 7)		X		Each					25°C		5	pF
Z_{out}	Output impedance (see Note 8)		X					2, 7	1, 8	25°C		5	Ω

NOTES: 6. The algebraic convention where the most-positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more-negative voltages.

7. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. C_{in} = Q/V. When a terminal is an input to more than one gate, multiply the value given by the number of gates to which this terminal is an input.

8. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

TABLE I—INITIAL CONDITIONS

Several of the parameters require the application of conditions which cause the outputs to assume definite states prior to applying test conditions specified above.

SYMBOL	DESCRIPTION	INPUT TERMINALS* 0.5 V	INPUT TERMINALS* −0.5 V
X	Irrelevant		
S	Set 1Q and 2Q high, 1$\bar{Q}$ and 2$\bar{Q}$ low	11, 13	14, 12
R	Reset 1Q and 2Q low, 1$\bar{Q}$ and 2$\bar{Q}$ high		11, 12, 13, 14

*V_{BB} (pin 15) = GND, V_{CC} (pins 3 and 6) = 1.32 V, V_{EE} (pin 10) = −3.2 V. Input and output terminals are open except as specified in these tables and in the d-c test figures.

ECL2541 electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS*									MIN	TYP (SEE NOTE 6)	MAX	UNIT
		TEST FIGURE	INITIAL CONDITIONS (SEE TABLE II)	VOLTAGE AT INPUT UNDER TEST	INPUT(S) UNDER TEST	OTHER INPUT TERMINALS 0.5 V	OTHER INPUT TERMINALS −0.5 V	OUTPUT TERMINAL Q	OUTPUT TERMINAL $\overline{Q}$	T_A				
V_{IH}	High-level input voltage									0°C	150		720	mV
										25°C	150		720	
										75°C	150		720	
V_{IL}	Low-level input voltage									0°C	−1500		−150	mV
										25°C	−1500		−150	
										75°C	−1500		−150	
$V_{OH(Q)}$	High-level output voltage at Q output, register mode	4	X	0.2 V	11		1, 9, 12, 16	8		0°C				mV
					13		1, 9, 14, 16	7						
				−0.2 V	12	11	1, 9, 16	8		0°C	280			
					14	13	1, 9, 16	7		25°C	315			
				−0.2 V	9	11	1, 12, 16	8		75°C				
					9	13	1, 14, 16	7						
$V_{OL(Q)}$	Low-level output voltage at Q output, register mode	4	X	−0.2 V	11		1, 9, 12, 16	8		0°C				mV
					13		1, 9, 14, 16	7						
				−0.2 V	12		1, 9, 11, 16	8		25°C			−330	
					14		1, 9, 13, 16	7		75°C			−210	
				−0.2 V	9		1, 11, 12, 16	8						
					9		1, 13, 14, 16	7						
$V_{OH(Q)}$	High-level output voltage at Q output, storage mode	4	S	0.2 V	12		1, 9, 11, 16	8		0°C	280	365		mV
					14		1, 9, 13, 16	7		25 C	315	400	500	
				0.2 V	9		1, 11, 12, 16	8		75°C		470	580	
					9		1, 13, 14, 16	7						
$V_{OL(Q)}$	Low-level output voltage at Q output, storage mode	4	R	0.2 V	12	11	1, 9, 16	8		0°C	−505	−440		mV
					14	13	1, 9, 16	7		25°C	−480	−400	−330	
				0.2 V	9	11	1, 12, 16	8		75°C		−280	−210	
					9	13	1, 14, 16	7						
$V_{OH(\overline{Q})}$	High-level output voltage at $\overline{Q}$ output, storage mode	4	R	0.2 V	12	11	1, 9, 16		2, 4	0°C	280	365		mV
					14	13	1, 9, 16		5, 6	25°C	315	400	500	
				0.2 V	9	11	1, 12, 16		2, 4	75°C		470	580	
					9	13	1, 14, 16		5, 6					
$V_{OL(\overline{Q})}$	Low-level output voltage at $\overline{Q}$ output, storage mode	4	S	0.2 V	12		1, 9, 11, 16		2, 4	0°C	−505	−440		mV
					14		1, 9, 13, 16		5, 6	25°C	−490	−425	−350	
				0.2 V	9		1, 11, 12, 16		2, 4	75°C		−390	−315	
					9		1, 13, 14, 16		5, 6					
$V_{OH(Q)}$	High-level output voltage at Q output, set mode	4	R	0.2 V	1	9	16	8		0°C	280			mV
					1	9	16	7		25°C	315			
										75°C				
$V_{OL(Q)}$	Low-level output voltage at Q output, reset mode	4	S	0.2 V	16	9	1	8		0°C				mV
					16	9	1	7		25°C			−330	
										75°C			−210	

(Continued on page 11)

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ECL2541 electrical characteristics at specified free-air temperature (continued)

PARAMETER		TEST CONDITIONS*								MIN	TYP	MAX (SEE NOTE 6)	UNIT
		TEST FIGURE	INITIAL CONDITIONS (SEE TABLE II)	VOLTAGE AT INPUT UNDER TEST	INPUT(S) UNDER TEST	OTHER INPUT TERMINALS 0.5 V	OTHER INPUT TERMINALS −0.5 V	OUTPUT TERMINAL Q	OUTPUT TERMINAL $\overline{Q}$	T_A			
I_{IH}	High-level input current	5	X	0.5 V	9		1, 11, 12 13,14,16			0°C		255	μA
					11		1, 9, 12, 13, 14, 16			25°C		235	
					13		1, 9, 11, 12, 14, 16			75°C		200	
					1		9, 11, 12 13, 14, 16			0°C		510	μA
					12		1, 9, 11 13, 14, 16			25°C		470	
					14		1, 9, 11 12, 13, 16			75°C		400	
					16		1, 9, 11 12, 13, 14						
I_{IL}	Low-level input current	6	X	All inputs in parallel at −3.2 V						0°C		−0.6	μA
										25°C		−0.8	
										75°C		−1.1	
I_{CC} or $-I_{EE}$	Supply current	7	X	All inputs in parallel at −0.5 V						25°C	60	124	mA
C_{in}	Input capacitance (see Note 7)		X		Each					25°C		5	pF
Z_{out}	Output impedance (see Note 8)		X					7, 8	2, 4, 5, 6	25°C		5	Ω

NOTES: 6. The algebraic convention where the most-positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more-negative voltages.

7. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Z. $C_{in} = Q/V$. When a terminal is an input to more than one gate, multiply the value given by the number of gates to which this terminal is an input.

8. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

TABLE II–INITIAL CONDITIONS

Several of the parameters require the application of conditions which cause the outputs to assume definite states prior to applying test conditions specified above.

SYMBOL	DESCRIPTION	INPUT TERMINALS* 0.5 V	INPUT TERMINALS* −0.5 V
X	Irrelevant		
S	Set 1Q and 2Q high, 1$\overline{Q}$1, 1$\overline{Q}$2, 2$\overline{Q}$1, and 2$\overline{Q}$2 low	1, 9	16
R	Reset 1Q and 2Q low, 1$\overline{Q}$1, 1$\overline{Q}$2, 2$\overline{Q}$1, and 2$\overline{Q}$2 high	9, 16	1

*V_{BB} (pin 15) = GND, V_{CC} (pin 3) = 1.32 V, V_{EE} (pin 10) = −3.2 V. Input and output terminals are open except as specified in these tables and in the d-c test figures.

ECL2542 electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS*									MIN	TYP (SEE NOTE 6)	MAX	UNIT
		TEST FIGURE	INITIAL CONDITIONS (SEE TABLE III)	VOLTAGE AT INPUT UNDER TEST	INPUT(S) UNDER TEST	OTHER INPUT TERMINALS 0.5 V	OTHER INPUT TERMINALS −0.5 V	OUTPUT TERMINAL $\overline{Q}$	T_A					
V_{IH}	High-level input voltage								0°C		150		720	mV
									25°C		150		720	
									75°C		150		720	
V_{IL}	Low-level input voltage								0°C		−1500		−150	mV
									25°C		−1500		−150	
									75°C		−1500		−150	
V_{OH}	High-level output voltage, register mode	4	X	−0.2 V	13	1, 16	4, 5, 12, 14	2	0°C		280			mV
					11	7, 8	4, 5, 9, 12	6						
					14	1, 16	4, 5, 12, 13	2						
					9	7, 8	4, 5, 11, 12	6						
					12	1, 16	4, 5, 13, 14	2						
					12	7, 8	4, 5, 9, 11	6	25°C		315			
					16	13, 14	1, 4, 5, 12	2						
					8	9, 11	4, 5, 7, 12	6	75°C					
					1	13, 14	4, 5, 12, 16	2						
					7	9, 11	4, 5, 8, 12	6						
					12	13, 14	1, 4, 5, 16	2						
					12	9, 11	4, 5, 7, 8	6						
V_{OL}	Low-level output voltage, register mode	4	X	0.2 V	13	1	4, 5, 12, 14, 16	2	0°C				−350	mV
					11	7	4, 5, 8, 9, 12	6						
				−0.2 V	14	1, 13	4, 5, 12, 16	2						
					9	7, 11	4, 5, 8, 12	6						
				−0.2 V	12	1, 13	4, 5, 14, 16	2	25°C					
					12	7, 11	4, 5, 8, 9	6						
				0.2 V	16	14	1, 4, 5, 12, 13	2	75°C				−315	
					8	9	4, 5, 7, 11, 12	6						
				−0.2 V	1	14, 16	4, 5, 12, 13	2						
					7	8, 9	4, 5, 11, 12	6						
				−0.2 V	12	14, 16	1, 4, 5, 13	2						
					12	8, 9	4, 5, 7, 11	6						
V_{OH}	High-level output voltage, storage mode	4	R	0.2 V	14	1, 13	4, 5, 12, 16	2	0°C		280	365		mV
					9	7, 11	4, 5, 8, 12	6						
					1	14, 16	4, 5, 12, 13	2	25°C		315	400	500	
					7	8, 9	4, 5, 11, 12	6						
					12		1, 4, 5, 13, 14, 16	2	75°C			470	580	
					12		4, 5, 7, 8, 9, 11	6						
V_{OL}	Low-level output voltage, storage mode	4	S	0.2 V	14	1	4, 5, 12, 13, 16	2	0°C		−505	−440		mV
					9	7	4, 5, 8, 11, 12	6						
					1	14	4, 5, 12, 13, 16	2	25°C		−490	−425	−350	
					7	9	4, 5, 8, 11, 12	6						
					12		1, 4, 5, 13, 14, 16	2	75°C			−390	−315	
					12		4, 5, 7, 8, 9, 11	6						
V_{OL}	Low-level output voltage, set mode	4	R	0.2 V	5	12	4	2	0°C				−350	mV
					5	12	4	6	25°C					
									75°C				−315	
V_{OH}	High-level output voltage, reset mode	4	S	0.2 V	4	12	5	2	0°C		280			mV
					4	12	5	6	25°C		315			
									75°C					

(Continued on page 13)

ECL2542 electrical characteristics at specified free-air temperature (continued)

PARAMETER		TEST CONDITIONS*								MIN TYP MAX (SEE NOTE 6)	UNIT
		TEST FIGURE	INITIAL CONDITIONS (SEE TABLE III)	VOLTAGE AT INPUT UNDER TEST	INPUT(S) UNDER TEST	OTHER INPUT TERMINALS 0.5 V	OTHER INPUT TERMINALS −0.5 V	OUTPUT TERMINAL $\overline{Q}$	T_A		
I_{IH}	High level input current	5	X	0.5 V	8		1, 4, 5, 7, 9 11, 12, 13, 14, 16		0°C 25°C 75°C	255 235 200	μA
					11		1, 4, 5, 7, 8 9, 12, 13, 14, 16				
					12		1, 4, 5, 7, 8 9, 11, 13, 14, 16				
					13		1, 4, 5, 7, 8 9, 11, 12, 14, 16				
					16		1, 4, 5, 7, 8 9, 11, 12, 13, 14				
					1		4, 5, 7, 8, 9 11, 12, 13, 14, 16		0°C 25°C 75°C	510 470 400	μA
					4		1, 5, 7, 8, 9 11, 12, 13, 14, 16				
					5		1, 4, 7, 8, 9 11, 12, 13, 14, 16				
					7		1, 4, 5, 8, 9 11, 12, 13, 14, 16				
					9		1, 4, 5, 7, 8 11, 12, 13, 14, 16				
					14		1, 4, 5, 7, 8 9, 11, 12, 13, 16				
I_{IL}	Low-level input current	6	X	All inputs in parallel at −3.2 V					0°C 25°C 75°C	−0.9 −1.2 −1.7	μA
I_{CC} or $-I_{EE}$	Supply current	7	X	All inputs in parallel at −0.5 V					25°C	81 165	mA
C_{in}	Input capacitance (see Note 7)		X		Each				25°C	5	pF
Z_{out}	Output impedance (see Note 8)		X					2, 6	25°C	5	Ω

NOTES: 6. The algebraic convention where the most-positive limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −350 mV is a maximum, the typical and minimum limits are more-negative voltages.

7. C_{in} is measured using peak-current techniques. A square-wave input pulse is applied, and the input current waveform is integrated with respect to time to determine Q. C_{in} = Q/V. When a terminal is an input to more than one gate, multiply the value given by the number of gates to which this terminal is an input.

8. Constant-current loads are used to determine the output impedance which is derived from the slope of a V_O vs I_O curve.

TABLE III—INITIAL CONDITIONS

Several of the parameters require the application of conditions which cause the outputs to assume definite states prior to applying test conditions specified above.

SYMBOL	DESCRIPTION	INPUT TERMINALS* 0.5 V	INPUT TERMINALS* −0.5 V
X	Irrelevant		
S	Set $1\overline{Q}$ and $2\overline{Q}$ low	5, 12	4
R	Reset $1\overline{Q}$ and $2\overline{Q}$ high	4, 12	5

*V_{BB} (pin 15) = GND, V_{CC} (pin 3) = −1.3 V, V_{EE} (pin 10) = −3.2 V. Input and output terminals are open except as specified in these tables and in the d-c test figures.

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operating characteristics at specified free-air temperature

MODE	C_L pF	t_{PHL} and/or t_{PLH} PROPAGATION TIMES—ns									t_{THL} and/or t_{TLH} TRANSITION TIMES—ns								
		T_A = 0°C			T_A = 25°C			T_A = 75°C			T_A = 0°C			T_A = 25°C			T_A = 75°C		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
ECL2540 (see Figure 2 and Table IV)																			
Register	4		2.5		1.6	2.4	3.5		2.5			3.8		2	3.7	5.2		3.9	
	50		3.6		2.4	3.6	4.5		3.6			4.7		2.5	4.6	6.7		4.4	
ECL2541 (see Figure 3 and Table V)																			
Register (Clock Controlled)	4		6.3		4.2	6.2	7.7		6.5			4.6		2	4.7	6.9		4.7	
	50		7.7		5.5	7.8	10.8		8.0			5.9		2.7	5.8	8.6		5.5	
Register (Gate Controlled)	4		4.3		2.3	4.2	5.8		4.3			4.6		2.3	4.6	6.5		4.6	
	50		5.6		3.4	5.7	8.5		5.7			5.6		2.7	5.4	7.8		5.1	
Set	4		2.7		1.9	2.7	3.5		2.8			4.5		2.9	4.5	6		4.6	
	50		3.8		2.7	3.8	4.7		3.8			4.7		2.7	4.6	7		4.5	
Reset	4		3.8		2.3	3.8	5.8		4.1			4.4		2.3	4.3	6.5		4.6	
	50		6.0		3.4	5.9	8.5		6.0			7.1		4.6	7.0	8.6		6.4	
ECL2542 (see Figure 3 and Table VI)																			
Register (Clock Controlled)	4		7.0		5.5	7.0	8.1		7.1			4.6		3	4.5	5.7		4.5	
	50		8.2		6.7	8.1	9.4		8.3			4.8		3	4.8	6.9		4.7	
Register (Gate Controlled)	4		4.5		3.3	4.4	5.7		4.4			4.2		3	4.1	5.7		4.1	
	50		5.7		4.5	5.6	6.8		5.5			4.7		3	4.7	6.9		4.6	
Set	4		2.9		1.7	2.7	3.1		2.6			4.6		3	4.5	5.7		4.6	
	50		4.0		3.2	4.0	4.7		3.9			5.4		4	5.6	6.9		5.5	
Reset	4		4.4		3.3	4.3	5.8		4.6			4.2		3	4.2	5.7		4.4	
	50		5.4		4.5	5.4	6.8		5.4			3.9		3	4.0	5		4.0	

4

PARAMETER MEASUREMENT INFORMATION

TABLE IV—ECL2540

INPUT TERMINALS		OUTPUT UNDER TEST		PARAMETER MEASURED
DATA GENERATOR	−0.5 V			
14	12	2	Q	t_{PLH}, t_{TLH}, t_{PHL}, and t_{THL}
14	12	1	$\overline{Q}$	
12	14	7	Q	
12	14	8	$\overline{Q}$	

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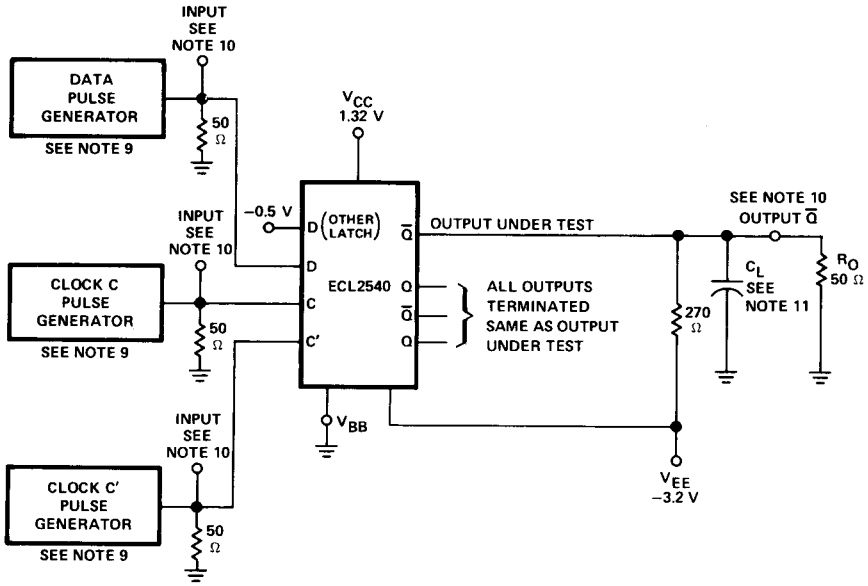
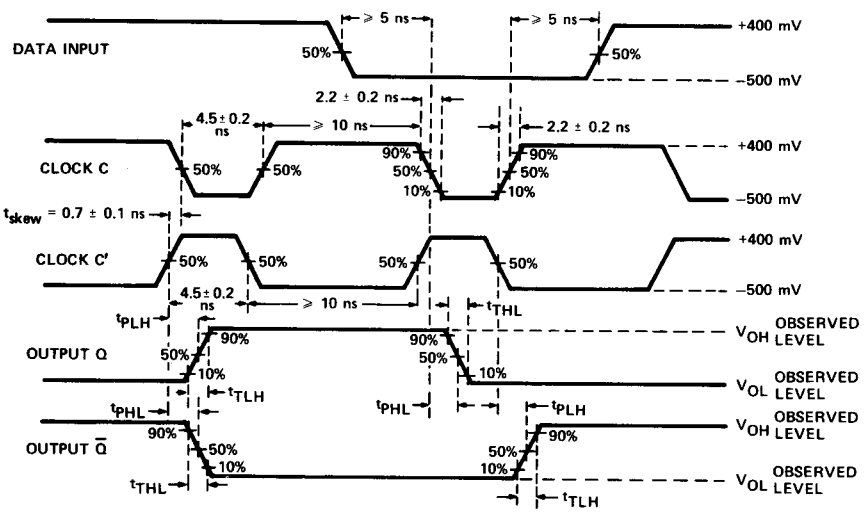
PARAMETER MEASUREMENT INFORMATION
ECL2540



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 2–ECL2540 PROPAGATION DELAY AND TRANSITION TIMES (WITH SKEW)

NOTES:
9. Each generator has a 50-Ω output impedance.
10. The waveforms are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. Either a high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF, or a 50-Ω impedance system can be used. The 50-Ω resistor designated R_O is the oscilloscope input resistance in the 50-Ω system or a discrete resistor with a high-impedance probe.
11. C_L includes probe and fixture capacitance. A capacitance of 50 pF can be used to approximate an a-c fan-out of 10.

PARAMETER MEASUREMENT INFORMATION

TABLE V–ECL2541

MODE	INPUT TERMINAL CONDITIONS				OUTPUT UNDER TEST	WAVEFORM	PARAMETER MEASURED
	PULSE GENERATOR NO. 1	PULSE GENERATOR NO. 2	0.5 V	−0.5 V			
REGISTER (Clock Controlled)	16	9	11	1, 12	8	LH	t_{PLH}, t_{TLH}
	1			11, 12, 16	8	HL	t_{PHL}, t_{THL}
	1			11, 12, 16	2, 4	LH	t_{PLH}, t_{TLH}
	16		11	1, 12	2, 4	HL	t_{PHL}, t_{THL}
	16	9	13	1, 14	7	LH	t_{PLH}, t_{TLH}
	1			13, 14, 16	7	HL	t_{PHL}, t_{THL}
	1			13, 14, 16	5, 6	LH	t_{PLH}, t_{TLH}
	16		13	1, 14	5, 6	HL	t_{PHL}, t_{THL}
REGISTER (Gate Controlled)	16	12	11	1, 9	8	LH	t_{PLH}, t_{TLH}
	1			9, 11, 16	8	HL	t_{PHL}, t_{THL}
	1			9, 11, 16	2, 4	LH	t_{PLH}, t_{TLH}
	16		11	1, 9	2, 4	HL	t_{PHL}, t_{THL}
	16	14	13	1, 9	7	LH	t_{PLH}, t_{TLH}
	1			9, 13, 16	7	HL	t_{PHL}, t_{THL}
	1			9, 13, 16	5, 6	LH	t_{PLH}, t_{TLH}
	16		13	1, 9	5, 6	HL	t_{PHL}, t_{THL}
SET TIME	16	1	9	All other input terminals open	8	LH	t_{PLH}, t_{TLH}
					2, 4	HL	t_{PHL}, t_{THL}
					7	LH	t_{PLH}, t_{TLH}
					5, 6	HL	t_{PHL}, t_{THL}
RESET TIME	1	16	9		2, 4	LH	t_{PLH}, t_{TLH}
					8	HL	t_{PHL}, t_{THL}
					5, 6	LH	t_{PLH}, t_{TLH}
					7	HL	t_{PHL}, t_{THL}

TABLE VI–ECL2542

MODE	INPUT TERMINAL CONDITIONS				OUTPUT UNDER TEST	WAVEFORM	PARAMETER MEASURED
	PULSE GENERATOR NO. 1	PULSE GENERATOR NO. 2	0.5 V	−0.5 V			
REGISTER (Clock Controlled)	5	12	1, 16	4, 13, 14	2	LH	t_{PLH}, t_{TLH}
			13, 14	1, 4, 16		LH	t_{PLH}, t_{TLH}
	4		1, 13, 16	5, 14		HL	t_{PHL}, t_{THL}
			13, 14, 16	1, 5		HL	t_{PHL}, t_{THL}
	5	12	7, 8	4, 9, 11	6	LH	t_{PLH}, t_{TLH}
			9, 11	4, 7, 8		LH	t_{PLH}, t_{TLH}
	4		7, 8, 11	5, 9		HL	t_{PHL}, t_{THL}
			8, 9, 11	5, 7		HL	t_{PHL}, t_{THL}
REGISTER (Gate Controlled)	5	14	1, 16	4, 12, 13	2	LH	t_{PLH}, t_{TLH}
		1	13, 14	4, 12, 16		LH	t_{PLH}, t_{TLH}
	4	14	1, 13, 16	5, 12		HL	t_{PHL}, t_{THL}
		1	13, 14, 16	5, 12		HL	t_{PHL}, t_{THL}
	5	9	7, 8	4, 11, 12	6	LH	t_{PLH}, t_{TLH}
		7	9, 11	4, 8, 12		LH	t_{PLH}, t_{TLH}
	4	9	7, 8, 11	5, 12		HL	t_{PHL}, t_{THL}
		7	8, 9, 11	5, 12		HL	t_{PHL}, t_{THL}
SET TIME	4	5	12	All other input terminals open	2, 6	HL	t_{PHL}, t_{THL}
RESET TIME	5	4	12		2, 6	LH	t_{PLH}, t_{TLH}

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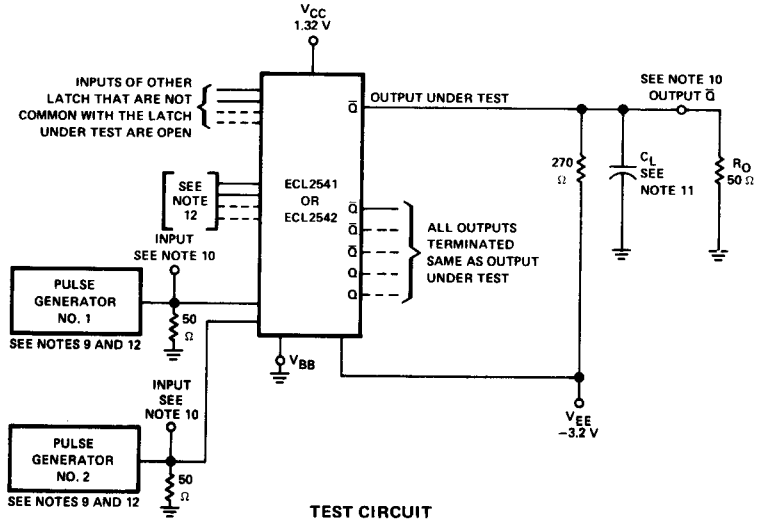
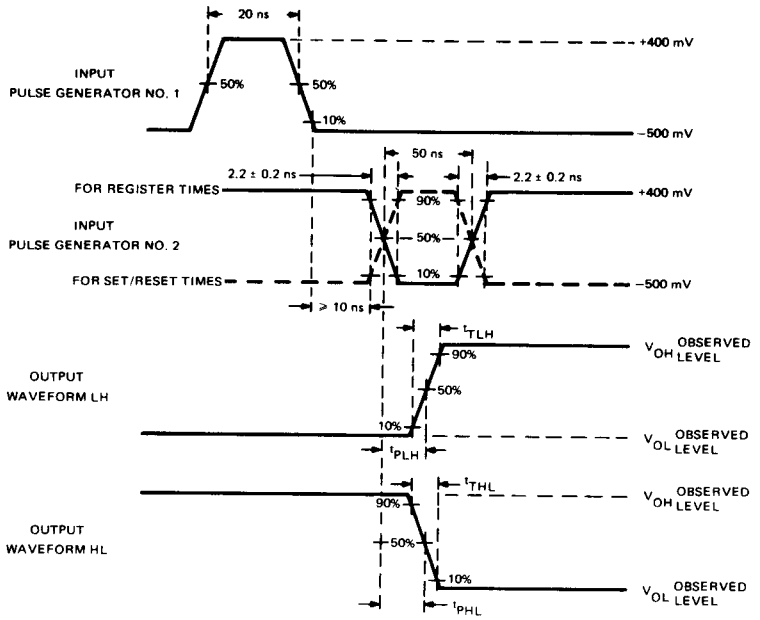
PARAMETER MEASUREMENT INFORMATION
ECL2541 AND ECL2542



TEST CIRCUIT

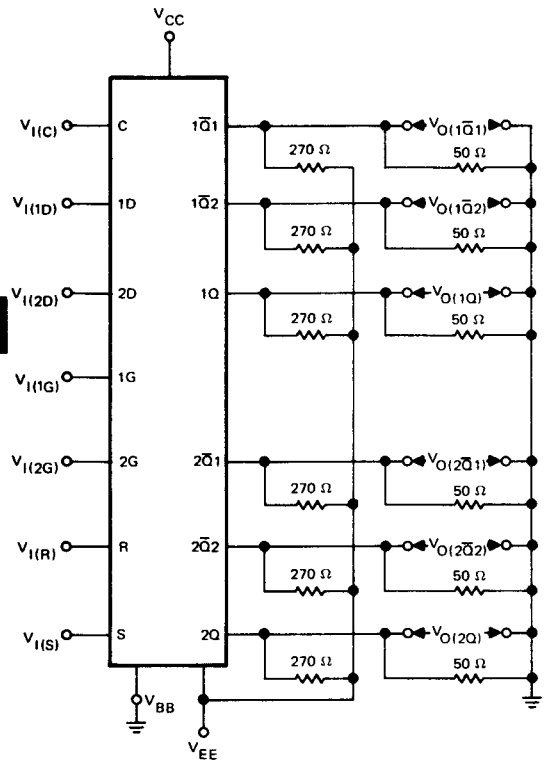


VOLTAGE WAVEFORMS

FIGURE 3–ECL2541 AND ECL2542 PROPAGATION DELAY AND TRANSITION TIMES

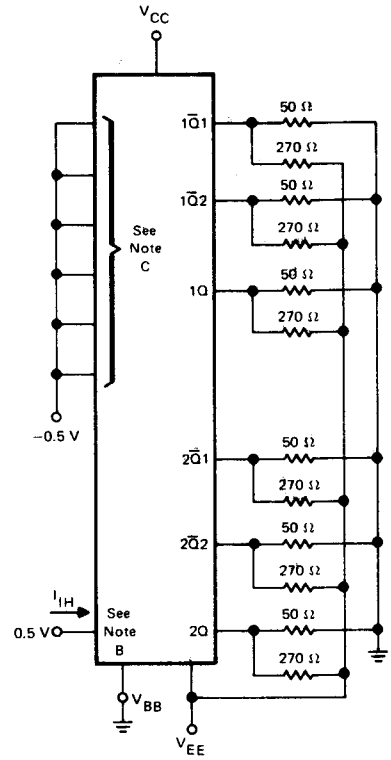
NOTES:
9. Each generator has a 50-Ω output impedance.
10. The waveforms are monitored on an oscilloscope with a rise time of less than or equal to 350 ps. Either a high-impedance probe with an input impedance of 100 kΩ paralleled by 2 pF, or a 50-Ω impedance system can be used. The 50-Ω resistor designated R_O is the oscilloscope input resistance in the 50-Ω system or a discrete resistor with a high-impedance probe.
11. C_L includes probe and fixture capacitance. A capacitance of 50 pF can be used to approximate an a-c fan-out of 10.
12. See Table V (ECL2541) or Table VI (ECL2542) for voltages to be applied to input terminals for each test.

PARAMETER MEASUREMENT INFORMATION†
ECL2541
(See Note 13)



V_I is applied to each input as specified in the electrical characteristics table.

FIGURE 4–V_{OH} AND V_{OL}



A. Each input is tested separately.
B. Any one of the following seven inputs: C, 1D, 1G, 2D, 2G, R, and S.
C. Other six inputs listed in note B that are not under test.

FIGURE 5–I_{IH}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.
NOTE 13: ECL2540 and ECL2542 are tested in a manner similar to that shown for ECL2541.

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PARAMETER MEASUREMENT INFORMATION†
ECL2541
(See Note 13)

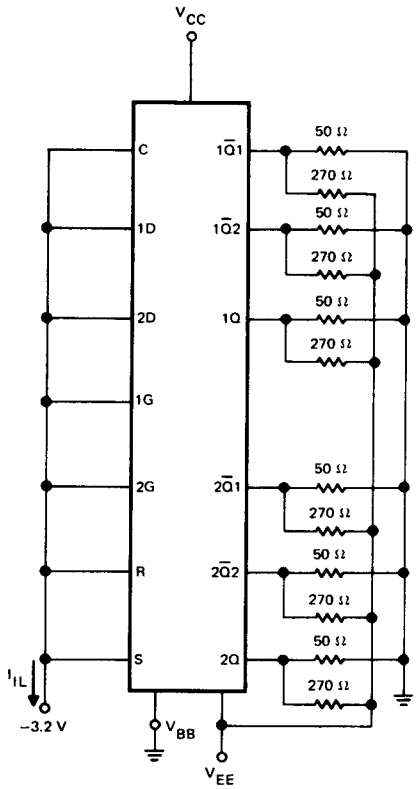


FIGURE 6–I_{IL}

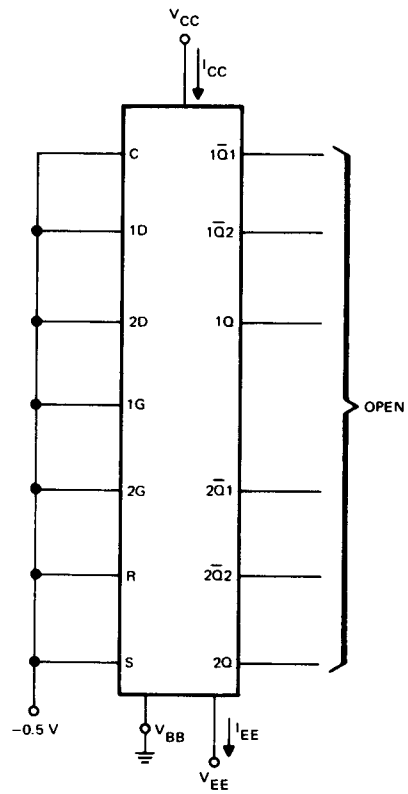


FIGURE 7–I_{CC} OR I_{EE}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

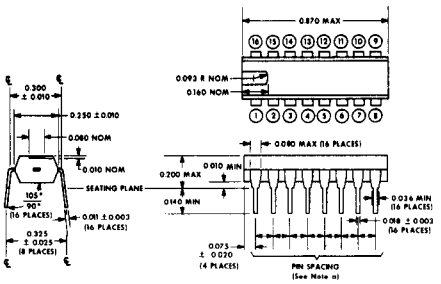
NOTE 13: ECL2540 and ECL2542 are tested in a manner similar to that shown for ECL2541.

mechanical data

The circuit bars are mounted on a 16-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

The plastic case is electrically nonconductive.

16-PIN PLASTIC DUAL-IN-LINE PACKAGE OUTLINE



NOTES: a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within 0.010 of its true longitudinal position relative to pins 1 and 16.

b. All dimensions are in inches unless otherwise noted.

terminal designations

Pin assignments are shown in the table below and correspond to the logic diagrams on pages 2 and 3. Outputs are denoted by 1Q, $1\overline{Q}$, 2Q, $2\overline{Q}$, 1Q1, $1\overline{Q}2$, $2\overline{Q}1$, and $2\overline{Q}2$. Inputs are denoted by C, C′, 1D, 2D, 1D1, 1D2, 2D1, 2D2, 1G, 2G, 1G1, 1G2, 2G1, 2G2, S and R. The number preceding the letter denotes whether the input (or output) is part of the first or second latch. The number (if any) following the letter distinguishes inputs (or outputs) of the same latch from each other.

Power is supplied via the V_{CC}, V_{EE}, and V_{BB} terminals.

V_{BB} is a reference voltage.

NC indicates no internal connection.

PIN ASSIGNMENTS

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ECL2540	$1\overline{Q}$	1Q	V_{CC}	NC	NC	V_{CC}	2Q	$2\overline{Q}$	NC	V_{EE}	C′	2D	C	1D	V_{BB}	NC
ECL2541	S	$1\overline{Q}1$	V_{CC}	$1\overline{Q}2$	$2\overline{Q}1$	$2\overline{Q}2$	2Q	1Q	C	V_{EE}	1D	1G	2D	2G	V_{BB}	R
ECL2542	1G1	$1\overline{Q}$	V_{CC}	R	S	$2\overline{Q}$	2G1	2D1	2G2	V_{EE}	2D2	C	1D2	1G2	V_{BB}	1D1

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