DUAL JK FLIP-FLOP WITH SET AND RESET; NEGATIVE-EDGE TRIGGER

FEATURES

- Asynchronous set and reset
- Output capability: standard
- I_{CC} category: flip-flops

GENERAL DESCRIPTION

The 74HC/HCT112 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT112 are dual negative-edge triggered JK-type flip-flops featuring individual nJ, nK, clock ($n\overline{CP}$), set ($n\overline{S}_D$) and reset ($n\overline{R}_D$) inputs. The set and reset inputs, when LOW, set or reset the outputs as shown in the function table regardless of the levels at the other inputs.

A HIGH level at the clock ($n\overline{CP}$) input enables the nJ and nK inputs and data will be accepted. The nJ and nK inputs control the state changes of the flip-flops as shown in the function table. The nJ and nK inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation. Output state changes are initiated by the HIGH-to-LOW transition of $n\overline{CP}$.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to nQ, $n\overline{Q}$	C_L = 15 pF; V_{CC} = 5 V	17	19	ns
	propagation delay $n\overline{S}_D$ to nQ, $n\overline{Q}$		15	15	ns
	propagation delay $n\overline{R}_D$ to nQ, $n\overline{Q}$		18	19	ns
f_{max}	maximum clock frequency		66	70	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	27	30	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 13	$1\overline{CP}$, $2\overline{CP}$	clock input (HIGH-to-LOW, edge triggered)
2, 12	1K, 2K	data inputs; flip-flops 1 and 2
3, 11	1J, 2J	data inputs; flip-flops 1 and 2
4, 10	$1\overline{S}_D$, $2\overline{S}_D$	set inputs (active LOW)
5, 9	1Q, 2Q	true flip-flop outputs
6, 7	$1\overline{Q}$, $2\overline{Q}$	complement flip-flop outputs
8	GND	ground (0 V)
15, 14	$1\overline{R}_D$, $2\overline{R}_D$	reset inputs (active LOW)
16	V_{CC}	positive supply voltage

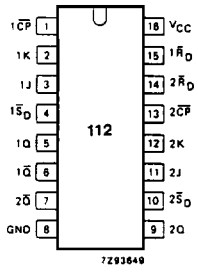

Fig. 1 Pin configuration.

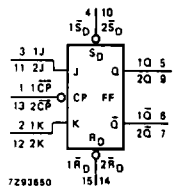

Fig. 2 Logic symbol.

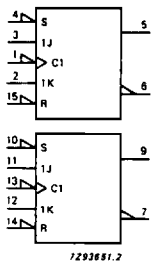

Fig. 3 IEC logic symbol.

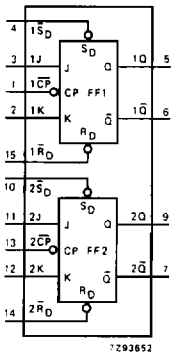

Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$n\bar{S}_D$	$n\bar{R}_D$	$n\bar{C}P$	nJ	nK	nQ	$n\bar{Q}$
asynchronous set	L	H	X	X	X	H	L
asynchronous reset	H	L	X	X	X	L	H
undetermined	L	L	X	X	X	H	L
toggle	H	H	↓	h	h	$\bar{q}$	q
load "0" (reset)	H	H	↓	l	h	L	H
load "1" (set)	H	H	↓	h	l	H	$\underline{L}$
hold "no change"	H	H	↓	l	l	q	$\underline{q}$

Note to function table

If $n\bar{S}_D$ and $n\bar{R}_D$ simultaneously go from LOW to HIGH, the output states will be unpredictable.

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW CP transition
X = don't care
↓ = HIGH-to-LOW CP transition

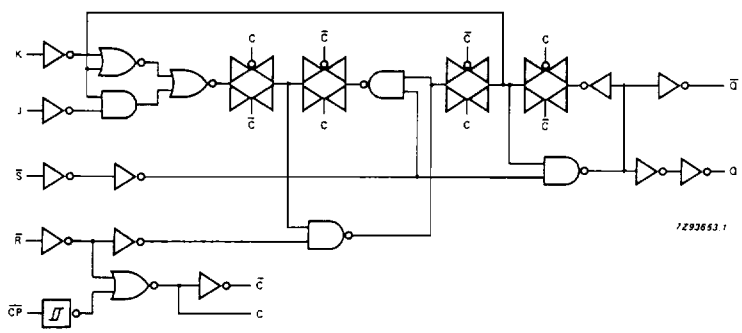

Fig. 5 Logic diagram (one flip-flop).

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: flip-flops

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to nQ		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to $n\overline{Q}$		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{R}_D$ to nQ, $n\overline{Q}$		58 21 17	180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $n\overline{S}_D$ to nQ, $n\overline{Q}$		50 18 14	155 31 26		295 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	set or reset pulse width LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time $n\overline{R}_D$ to $n\overline{CP}$	80 16 14	22 8 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time $n\overline{S}_D$ to $n\overline{CP}$	80 16 14	−19 −7 −6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time nJ, nK to $n\overline{CP}$	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_h	hold time nJ, nK to $n\overline{CP}$	0 0 0	−11 −4 −3		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 6
f_{max}	maximum clock pulse frequency	6 30 35	20 60 71		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: flip-flops

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$1\overline{S}_D$, $2\overline{S}_D$	0.5
1K, 2K	0.6
$1\overline{R}_D$, $2\overline{R}_D$	0.65
1J, 2J	1
$1\overline{CP}$, $2\overline{CP}$	1

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to nQ		21	35		44		53	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to $n\overline{Q}$		23	40		50		60	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay $n\overline{R}_D$ to nQ, $n\overline{Q}$		22	37		46		56	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $n\overline{S}_D$ to nQ, $n\overline{Q}$		18	32		40		48	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	16	8		20		24		ns	4.5	Fig. 6
t_W	set or reset pulse width LOW	18	10		23		27		ns	4.5	Fig. 7
t_{rem}	removal time $n\overline{R}_D$ to $n\overline{CP}$	20	11		25		30		ns	4.5	Fig. 7
t_{rem}	removal time $n\overline{S}_D$ to $n\overline{CP}$	20	−8		25		30		ns	4.5	Fig. 7
t_{su}	set-up time nJ, nK to $n\overline{CP}$	16	7		20		24		ns	4.5	Fig. 6
t_h	hold time nJ, nK to $n\overline{CP}$	0	−7		0		0		ns	4.5	Fig. 6
f_{max}	maximum clock pulse frequency	30	64		24		20		MHz	4.5	Fig. 6

AC WAVEFORMS

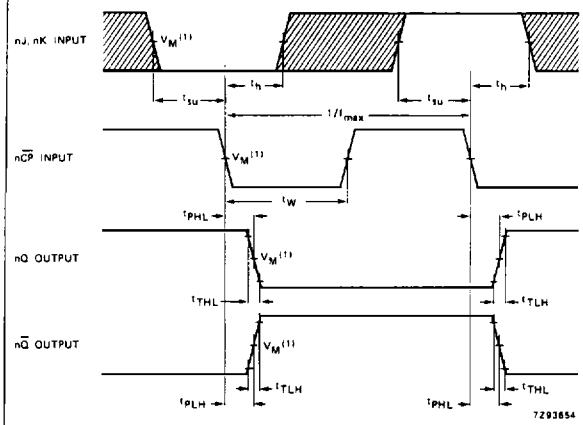

Fig. 6 Waveforms showing the clock ($n\overline{CP}$) to output (nQ, $n\overline{Q}$) propagation delays, the clock pulse width, the nJ, nK to $n\overline{CP}$ set-up times, the $n\overline{CP}$ to nJ, nK hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig. 6

The shaded areas indicate when the input is permitted to change for predictable output performance.

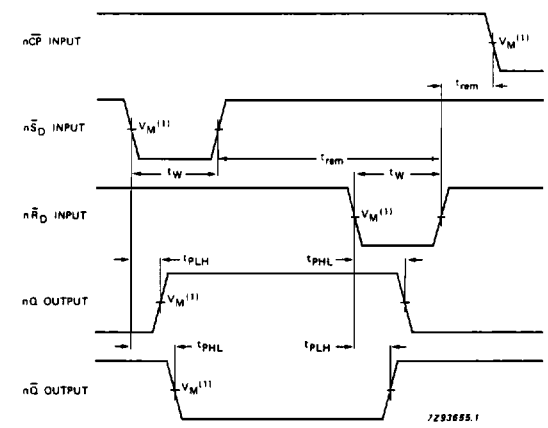

Fig. 7 Waveforms showing the set ($n\overline{S}_D$) and reset ($n\overline{R}_D$) input to output (nQ, $n\overline{Q}$) propagation delays, the set and reset pulse width and the $n\overline{R}_D$ and $n\overline{S}_D$ to $n\overline{CP}$ removal time.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.