

T-46-09-05 173

54/74173 54LS/74LS173

4-BIT D-TYPE REGISTER (With 3-State Outputs)

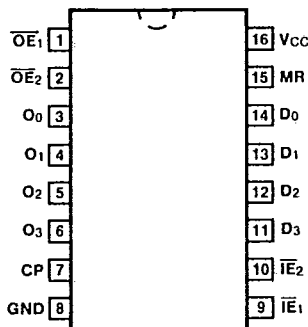
DESCRIPTION — The '173 is a high speed 4-bit register featuring 3-state outputs for use in bus-organized systems. The clock is fully edge-triggered allowing either a load from the D inputs or a hold (retain register contents) depending on the state of the Input Enable lines (\overline{IE}_1 , \overline{IE}_2). A HIGH on either Output Enable line (\overline{OE}_1 , \overline{OE}_2) brings the output to a high impedance state without affecting the actual register contents. A HIGH on the Master Reset (MR) input resets the register regardless of the state of the Clock (CP), the Output Enable (\overline{OE}_1 , \overline{OE}_2) or the Input Enable (\overline{IE}_1 , \overline{IE}_2) lines.

- FULLY EDGE-TRIGGERED
- 3-STATE OUTPUTS
- GATED INPUT AND OUTPUT ENABLES

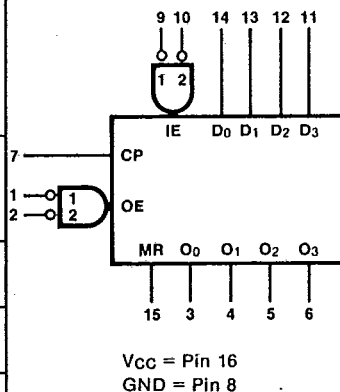
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V _{CC} = +5.0 V ±5%, T _A = 0°C to +70°C	V _{CC} = +5.0 V ±10%, T _A = -55°C to +125°C	
Plastic DIP (P)	A	74173PC, 74LS173PC		9B
Ceramic DIP (D)	A	74173DC, 74LS173DC	54173DM, 54LS173DM	7B
Flatpak (F)	A	74173FC, 74LS173FC	54173FM, 54LS173FM	4L

CONNECTION DIAGRAM PINOUT A



LOGIC SYMBOL



INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
D ₀ — D ₃	Data Inputs	1.0/1.0	0.5/0.25
\overline{IE}_1 , \overline{IE}_2	Input Enable Inputs (Active LOW)	1.0/1.0	0.5/0.25
\overline{OE}_1 , \overline{OE}_2	3-State Output Enable Inputs (Active LOW)	1.0/1.0	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	0.5/0.25
MR	Asynchronous Master Reset Input (Active HIGH)	1.0/1.0	0.5/0.25
O ₀ — O ₃	3-State Outputs	130/10 (50)	65/5.0 (25)/(2.5)

4

173

7-46-09-05

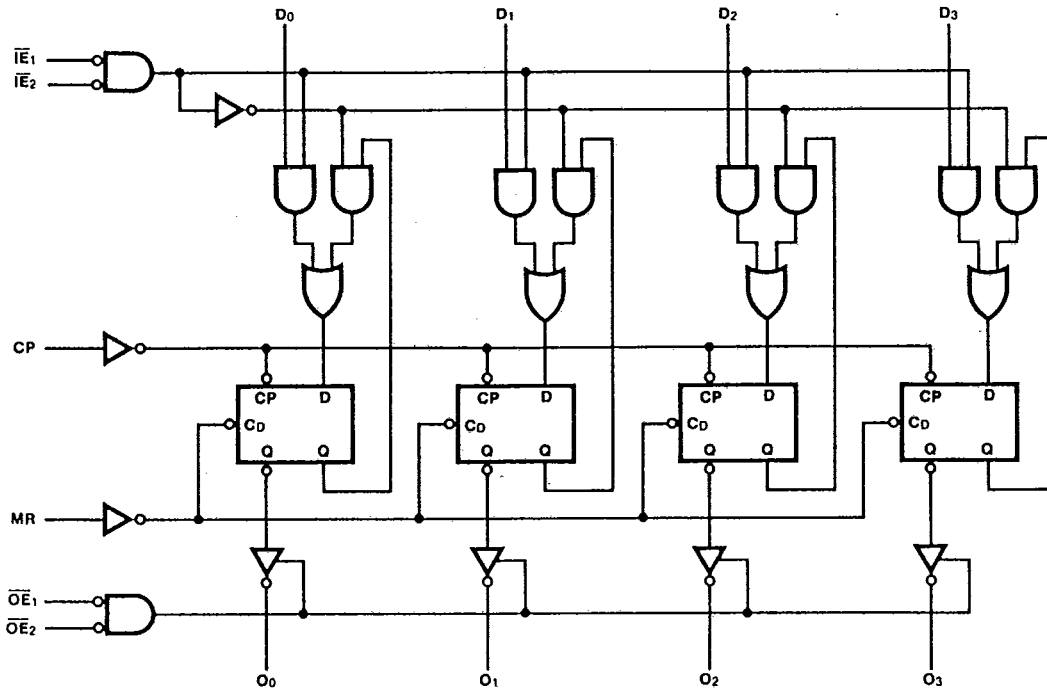
TRUTH TABLE

INPUTS					OUTPUT
MR	CP	\overline{OE}_1	\overline{OE}_2	D_n	Q_n
H	X	X	X	X	L
L	L	X	X	X	Q_n
L	\lceil	H	X	X	Q_n
L	\lceil	X	H	X	Q_n
L	\lceil	L	L	L	L
L	\lceil	L	L	H	H

When either \overline{OE}_1 or \overline{OE}_2 are HIGH, the output is in the OFF state (high impedance); however this does not affect the contents or sequential operating of the register.

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
I _{os}	Output Short Circuit Current	-30	-70	-20	-100	mA	V _{CC} = Max
I _{cc}	Power Supply Current		72		28	mA	V _{CC} = Max, MR = \overline{L} CP, $\overline{OE}_1 = 4.5\text{ V}$ $\overline{OE}_2, \overline{IE}_1, \overline{IE}_2, D_n = \text{Gnd}$

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		C _L = 50 pF R _L = 400 Ω		C _L = 15 pF			
		Min	Max	Min	Max		
f _{max}	Maximum Clock Frequency	25		30		MHz	Figs. 3-1, 3-8
t _{PLH} t _{PHL}	Propagation Delay CP to O _n		43 31		40 25	ns	
t _{PHL}	Propagation Delay, MR to O _n		27		25	ns	Figs. 3-1, 3-16
t _{PZH} t _{PZL}	Output Enable Time		30 30		20 20	ns	Figs. 3-3, 3-11, 3-12 R _L = 2 kΩ ('LS173)
t _{PHZ} t _{PLZ}	Output Disable Time		14 20		16 16	ns	Figs. 3-3, 3-11, 3-12 R _L = 2 kΩ ('LS173) C _L = 5 pF

4

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t _s (H) t _s (L)	Setup Time HIGH or LOW D _n to CP	10	10	10	10	ns	Fig. 3-6
t _h (H) t _h (L)	Hold Time HIGH or LOW D _n to CP	10	10	10	10	ns	
t _s (H) t _s (L)	Setup Time HIGH or LOW \overline{IE} to CP	17	17	17	17	ns	
t _h (H) t _h (L)	Hold Time HIGH or LOW \overline{IE} to CP	2.0	2.0	2.0	2.0	ns	
t _w (L)	CP Pulse Width LOW	20		17		ns	
t _w (H)	MR Pulse Width HIGH	20		17		ns	Fig. 3-16
t _{rec}	Recovery Time, MR to CP	10		15		ns	