MC74VHC1G125

Noninverting 3-State Buffer

The MC74VHC1G125 is an advanced high speed CMOS noninverting 3−state buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffered 3−state output which provides high noise immunity and stable output.

The MC74VHC1G125 input structure provides protection when voltages up to 7.0 V are applied, regardless of the supply voltage. This allows the MC74VHC1G125 to be used to interface 5.0 V circuits to 3.0 V circuits.

Features

- These are Pb−Free Devices
- High Speed: t_{PD} = 3.5 ns (Typ) at V_{CC} = 5.0 V
- Low Power Dissipation: I_{CC} = 1 μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: FETs = 58; Equivalent Gates = 15

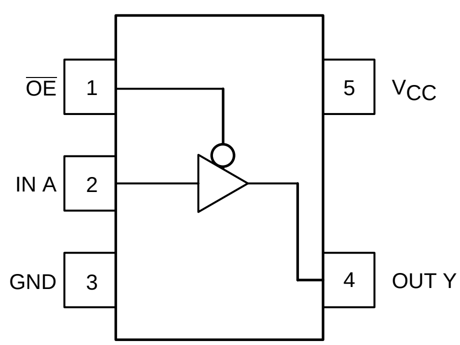


Figure 1. Pinout (Top View)

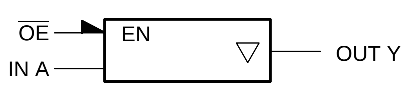
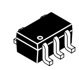


Figure 2. Logic Symbol

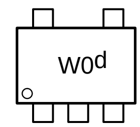
ON Semiconductor®

http://onsemi.com

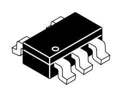
MARKING DIAGRAMS



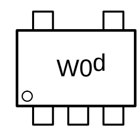
SC−88A/SOT−353/SC−70
DF SUFFIX
CASE 419A



Pin 1
d = Date Code



TSOP−5/SOT−23/SC−59
DT SUFFIX
CASE 483



Pin 1
d = Date Code

PIN ASSIGNMENT	
1	$\overline{OE}$
2	IN A
3	GND
4	OUT Y
5	V_{CC}

FUNCTION TABLE

A Input	$\overline{OE}$ Input	Y Output
L	L	L
H	L	H
X	H	Z

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 127 of this data sheet.

September, 2004 − Rev. 12

Publication Order Number:
MC74VHC1G125/D

MAXIMUM RATINGS

Symbol	Characteristics		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +7.0	V
V_{IN}	DC Input Voltage		−0.5 to +7.0	V
V_{OUT}	DC Output Voltage	V_{CC} = 0 High or Low State	−0.5 to 7.0 −0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current		−20	mA
I_{OK}	Output Diode Current	V_{OUT} < GND; V_{OUT} > V_{CC}	+20	mA
I_{OUT}	DC Output Current, per Pin		+25	mA
I_{CC}	DC Supply Current, V_{CC} and GND		+50	mA
P_D	Power Dissipation in Still Air	SC−88A, TSOP−5	200	mW
θ_{JA}	Thermal Resistance	SC−88A, TSOP−5	333	°C/W
T_L	Lead Temperature, 1 mm from Case for 10 s		260	°C
T_J	Junction Temperature Under Bias		+150	°C
T_{stg}	Storage Temperature		−65 to +150	°C
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 7) Machine Model (Note 8) Charged Device Model (Note 9)	> 2000 > 200 N/A	V
$I_{LatchUp}$	LatchUp Performance	Above V_{CC} and Below GND at 125°C (Note 10)	± 500	mA

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

7. Tested to EIA/JESD22−A114−A.
8. Tested to EIA/JESD22−A115−A.
9. Tested to JESD22−C101−A.
10. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{IN}	DC Input Voltage		0.0	5.5	V
V_{OUT}	DC Output Voltage		0.0	V_{CC}	V
T_A	Operating Temperature Range		−55	+125	°C
t_r , t_f	Input Rise and Fall Time	V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	0 0	100 20	ns/V

Device Junction Temperature versus Time to 0.1% Bond Failures

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

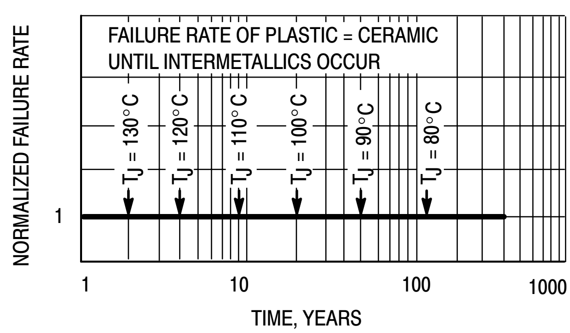


Figure 3. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	Typ	Max	$T_A \le$ 85°C Min	Max	−55 $\le T_A \le$ 125°C Min	Max	Unit
V_{IH}	Minimum High−Level Input Voltage		2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
V_{IL}	Maximum Low−Level Input Voltage		2.0 3.0 4.5 5.5			0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65	V
V_{OH}	Minimum High−Level Output Voltage V_{IN} = V_{IH} or V_{IL}	V_{IN} = V_{IH} or V_{IL} I_{OH} = −50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		V_{IN} = V_{IH} or V_{IL} I_{OH} = −4 mA I_{OH} = −8 mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V_{OL}	Maximum Low−Level Output Voltage V_{IN} = V_{IH} or V_{IL}	V_{IN} = V_{IH} or V_{IL} I_{OL} = 50 μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{IN} = V_{IH} or V_{IL} I_{OL} = 4 mA I_{OL} = 8 mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I_{OZ}	Maximum 3−State Leakage Current	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND	5.5			±0.25		± 2.5		± 2.5	μA
I_{IN}	Maximum Input Leakage Current	V_{IN} = 5.5 V or GND	0 to 5.5			±0.1		±1.0		± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5			1.0		20		40	μA

AC ELECTRICAL CHARACTERISTICS C_{load} = 50 pF, Input t_r = t_f = 3.0 ns

Symbol	Parameter	Test Conditions	T_A = 25°C Min	Typ	Max	$T_A \le$ 85°C Min	Max	−55 $\le T_A \le$ 125°C Min	Max	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Y (Figures 3 and 4)	V_{CC} = 3.3 ± 0.3 V C_L = 15 pF C_L = 50 pF		4.5 6.4	8.0 11.5		9.5 13.0		12.0 16.0	ns
		V_{CC} = 5.0 ± 0.5 V C_L = 15 pF C_L = 50 pF		3.5 4.5	5.5 7.5		6.5 8.5		8.5 10.5	
t_{PZL}, t_{PZH}	Maximum Output Enable Time, Input $\overline{OE}$ to Y (Figures 4 and 5)	V_{CC} = 3.3 ± 0.3 V C_L = 15 pF R_L = 1000 Ω C_L = 50 pF		4.5 6.4	8.0 11.5		9.5 13.0		11.5 15.0	ns
		V_{CC} = 5.0 ± 0.5 V C_L = 15 pF R_L = 1000 Ω C_L = 50 pF		3.5 4.5	5.1 7.1		6.0 8.0		8.5 10.5	
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time, Input $\overline{OE}$ to Y (Figures 4 and 5)	V_{CC} = 3.3 ± 0.3 V C_L = 15 pF R_L 1000 Ω C_L = 50 pF		6.5 8.0	9.7 13.2		11.5 15.0		14.5 18.0	ns
		V_{CC} = 5.0 ± 0.5 V C_L = 15 pF R_L = 1000 Ω C_L = 50 pF		4.8 7.0	6.8 8.8		8.0 10.0		10.0 12.0	
C_{IN}	Maximum Input Capacitance			4.0	10		10		10	pF
C_{OUT}	Maximum 3−State Output Capacitance (Output in High Impedance State)			6.0						pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 11)	8.0	pF

11. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

SWITCHING WAVEFORMS

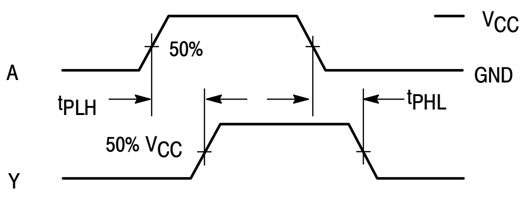


Figure 4. Switching Wave Forms

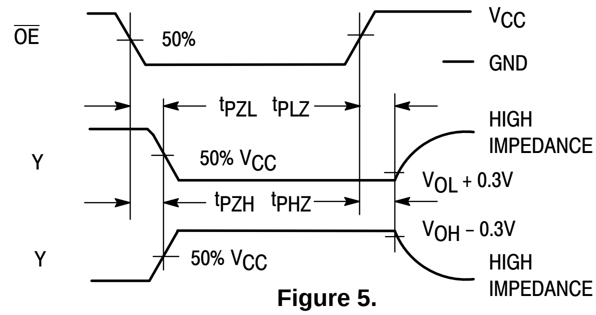
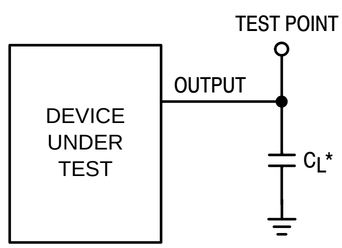
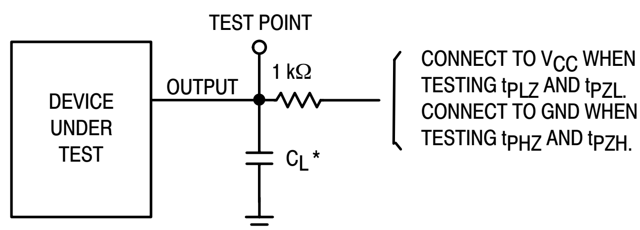


Figure 5.



*Includes all probe and jig capacitance

Figure 6. Test Circuit



*Includes all probe and jig capacitance

Figure 7. Test Circuit

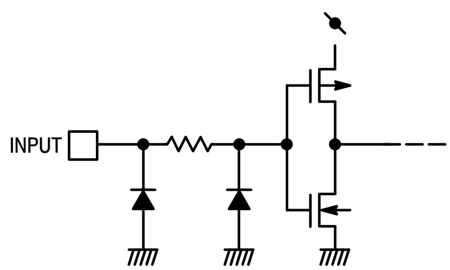


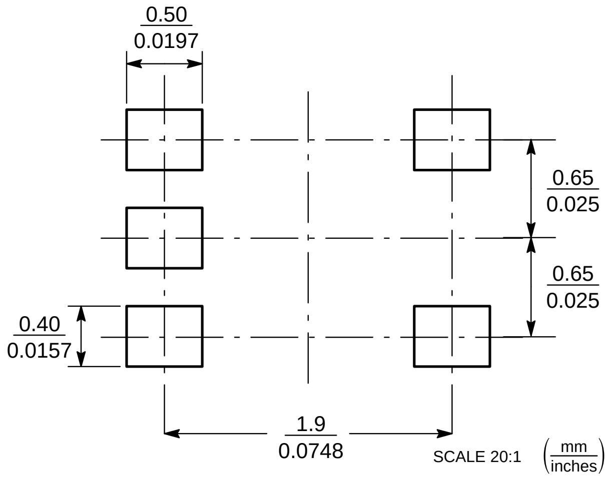
Figure 8. Input Equivalent Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature: Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix	Package Type (Name/SOT#/ Common Name)	Tape and Reel Size†
MC74VHC1G125DFT1	MC	74	VHC1G	125	DF	T1	SC−88A/SOT−353 /SC−70	178 mm (7”) 3000 Unit
MC74VHC1G125DFT1G	MC	74	VHC1G	125	DF	T1	SC−88A/SOT−353 /SC−70 (Pb−Free)	178 mm (7”) 3000 Unit
MC74VHC1G125DFT2	MC	74	VHC1G	125	DF	T2	SC−88A/SOT−353 /SC−70	178 mm (7”) 3000 Unit
MC74VHC1G125DFT2G	MC	74	VHC1G	125	DF	T2	TSC−88A/SOT−353 /SC−70 (Pb−Free)	178 mm (7”) 3000 Unit
MC74VHC1G125DTT1	MC	74	VHC1G	125	DT	T1	TSOP−5/SOT−23 /SC−59	178 mm (7”) 3000 Unit
MC74VHC1G125DTT1G	MC	74	VHC1G	125	DT	T1	TSOP−5/SOT−23 /SC−59 (Pb−Free)	178 mm (7”) 3000 Unit

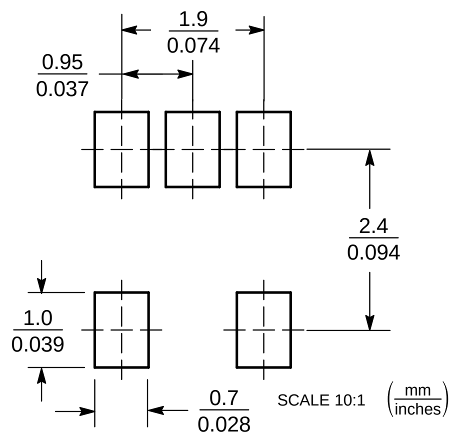
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.