FEATURES

- Positive edge-triggered common clock
- Asynchronous common reset
- Clock-to-output delays of 14 ns

DESCRIPTION

The LS174 is a six-bit register with single-rail outputs and the LS175 is a four-bit register with complementary outputs. Both consist of D-type flip-flops with a buffered common clock and an asynchronous, active-Low buffered clear.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

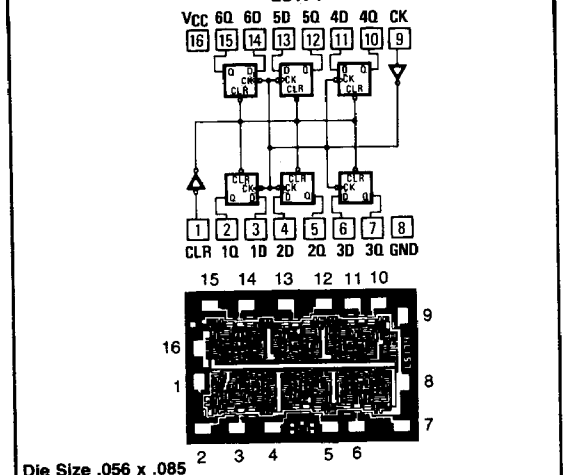
FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

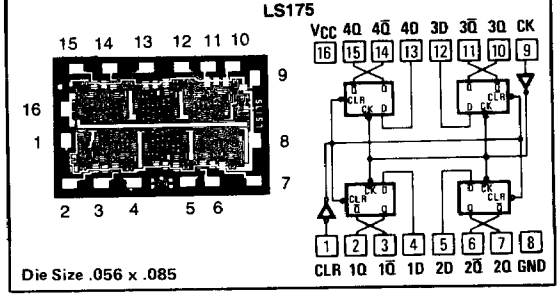
H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady state input conditions were established.
† = LS175 only

PIN-OUT DIAGRAMS

LS174

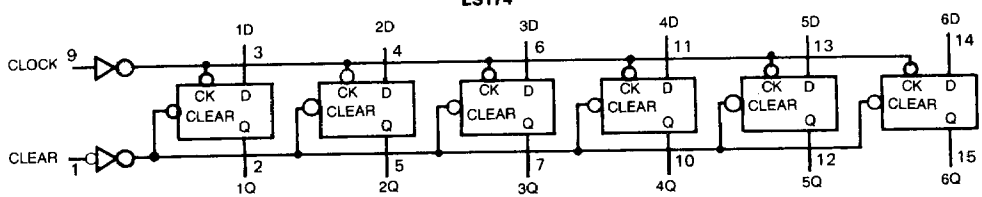


LS175

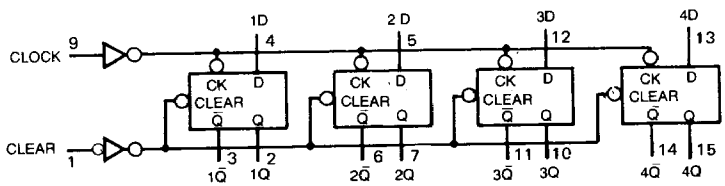


LOGIC DIAGRAMS

LS174



LS175



RAYTHEON

Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-400			-400	μA
Low-level output current, I_{OL}				4			8	mA
Clock frequency, f_{clock}		0		35	0		35	MHz
Width of clock pulse, t_w (Low)		15			15			ns
Width of clear pulse, t_w (Low)		20			20			ns
Setup time	Data input t_{setup}	10			10			ns
	Clear recovery, t_{rec}	12			12			ns
Data hold time, t_{hold}		5			5			ns
Operating free-air temperature, T_A		-55		125	0		70	°C

t_{setup} is the minimum time required for the correct logic level to be present at the data input prior to the rising edge of the clock in order to be recognized and transferred to the output.

t_{hold} is the minimum time required for the logic level to be maintained at the data input after the rising edge of the clock in order to insure recognition.

t_{rec} is the minimum time required between the end of the clear pulse and the rising edge of the clock in order to transfer High data to the Q output.

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=-400μA		2.5	3.5		2.7	3.5		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.4		0.25	0.40	V
		I_{OL}=8mA					0.35	0.5	
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				-0.4			-0.4	mA
I_{OS}†	V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CC}††	V_{CC}=MAX	LS174		16	26		16	26	mA
		LS175		11	18		11	18	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
††With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured, after a momentary ground, then 4.5V is applied to clock.

Switching Characteristics, V_{cc} = 5V Over Recommended Free-Air Temperature Range

Parameter	From (Input)	To (Output)	−55°C			+25°C			+125°C			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Figure A on page 2-174)												
f_{max}	maximum clock frequency					35	45					MHz
t_{PLH}	clear (LS175 only)	$\overline{Q}$		19	25		19	25		25	31	ns
t_{PHL}	clear (LS175 only)	Q		23	29		19	25		22	27	ns
t_{PLH}	clock	Q or $\overline{Q}$		14	20		13	17		14	19	ns
t_{PHL}	clock	Q or $\overline{Q}$		16	23		13	18		13	18	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Figure A on page 2-174)												
t_{PLH}	clear (LS175 only)	$\overline{Q}$		21	27		22	27		28	35	ns
t_{PHL}	clear (LS175 only)	Q		25	33		23	28		25	30	ns
t_{PLH}	clock	Q or $\overline{Q}$		16	22		15	19		17	21	ns
t_{PHL}	clock	Q or $\overline{Q}$		20	28		17	23		17	22	ns

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.