High Speed CMOS Transceivers With Parity

QS54/74FCT833T
QS54/74FCT853T

QS54/74FCT2833T
QS54/74FCT2853T
ADVANCE INFORMATION

FEATURES/BENEFITS

- Pin and function compatible to the Am29833/53
- Parity generation and detection
- CMOS power levels: <7.5 mW static
- Available in PDIP, ZIP, SOIC, QSOP, CERDIP
- Undershoot clamp diodes on all inputs
- TTL compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT 833T/53T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Iol = 48 mA Com., 32 mA Mil.

FCT 2833T/53T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Iol = 12 mA Com.

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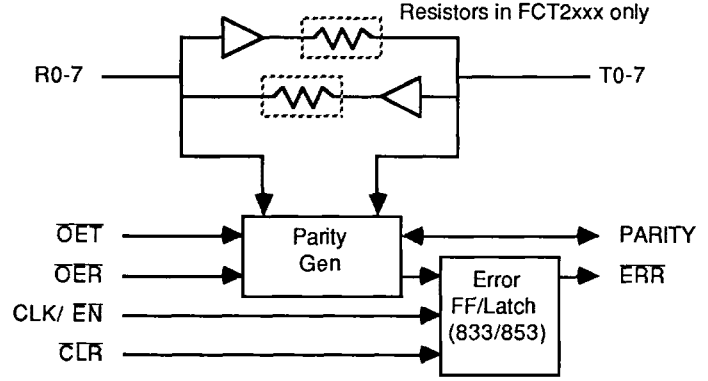
DESCRIPTION

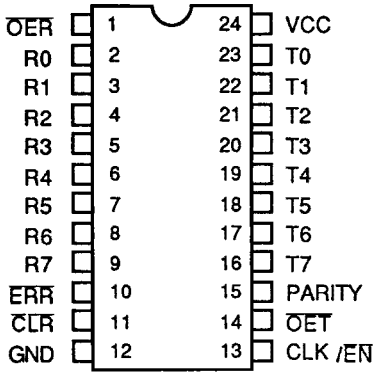
The QSFCT833T/853T and QSFCT2833T/2853T are 8-bit high-speed CMOS TTL compatible transceivers registers with three-state outputs and parity generate/detect logic that are ideal for driving high capacitance loads such as memory and address buses. These parts generate and check odd parity. All lows (zeros) in generates a one for parity. The 833 has a FF and the 853 has a latch to record a parity error defined as a difference between parity generated from the inputs and the parity bit supplied with the inputs. Once the FF/latch is set, it remains set until cleared by a pulse on $\overline{CLR}$. $\overline{ERR}$ is the output from this FF/latch and is open drain allowing multiple devices to be ORed. The 2833/53 devices are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. The 2833 series parts can replace the 833 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when Vcc is removed from the device.

FUNCTIONAL BLOCK DIAGRAM

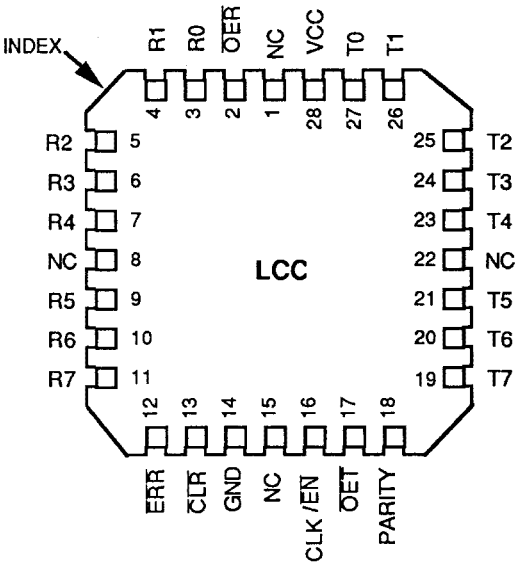


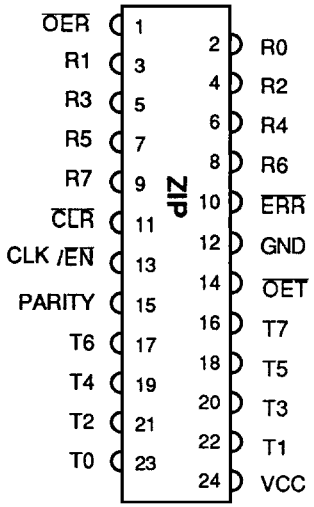
FCT833/853 PIN CONFIGURATIONS

PDIP, SOIC, QSOP



Note: Pin 13 (pin 16 of LCC) is CLK on 833 and EN on 853.





PIN DESCRIPTIONS

Name	I/O	Function
Ri	I/O	Data Bus, R side
Ti	I/O	Data Bus, T side
$\overline{OET}$	I	Enable R to T
$\overline{OER}$	I	Enable T to R
CLK	I	Parity FF Clock (833)
$\overline{EN}$	I	Parity Latch Enable (853)
$\overline{CLR}$	I	Parity FF/Latch Clear
PARITY	O	Parity
$\overline{ERR}$	O	Parity Error (Open Drain)

All packages are shown with the Top View

FCT833 FUNCTION TABLE

INPUTS						OUTPUTS				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	CLK	Ri (Σ of H's)	Ti Incl Parity (Σ of H's)	Ri	Ti	Parity	$\overline{ERR}$	Function
L	H	H	↑	H(Odd)	NA	NA	H	L	H	Transmit data from R port to T port with parity; receiveing path is disabled
L	H	H	↑	H(Even)	NA	NA	H	H	L	
L	H	H	↑	L(Odd)	NA	NA	L	L	H	
L	H	H	↑	L(even)	NA	NA	L	H	L	
H	L	H	↑	NA	H(odd)	H	NA	NA	H	Recievie data fromt T port to R port with parity test resulting in flag; transmitting path is disabled
H	L	H	↑	NA	H(even)	H	NA	NA	L	
H	L	H	↑	NA	L(odd)	L	NA	NA	H	
H	L	H	↑	NA	H(even)	L	NA	NA	L	
X	X	L	X	X	X	NA	NA	NA	H	Clear error flag register
H	H	H	H or L		X	Z	Z	Z	No chng	Tranmit and receive paths disabled. Parity in transmit mode
H	H	L	X		X	Z	Z	Z	H	
H	H	H	↑	H or L(Odd)	X	Z	Z	Z	H	
H	H	H	↑	H or L(even)	X	Z	Z	Z	L	
L	L	H	↑	H(Odd)	NA	NA	H	H	L	Error checking
L	L	H	↑	H(Even)	NA	NA	H	L	H	
L	L	H	↑	L(Odd)	NA	NA	L	H	L	
L	L	H	↑	L(even)	NA	NA	L	L	H	

NOTES :
1.. Output state assumes HIGH output before the state.
2. Odd = Odd number of logic one's
   Even = Even number of logic one's
   i = 0,1,2,3,4,5,6,7
   X = Don't care

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FCT853 FUNCTION TABLE

$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	$\overline{EN}$	Ri	Ri (Σ of H's)	Ti	Ti Incl Parity (Σ of H's)	Ri	Ti	Parity	$\overline{ERR}$	Function
L	H	X	X	H	ODD	NA	NA	NA	H	L	NA	Transmit data from R port to T port with parity; receiveing path is disabled
L	H	X	X	H	EVEN	NA	NA	NA	H	H	NA	
L	H	X	X	L	ODD	NA	NA	NA	L	L	NA	
L	H	X	X	L	EVEN	NA	NA	NA	L	H	NA	
H	L	X	L	NA	NA	H	ODD	H	NA	NA	H	Receive data fromt T port to R port with parity test resulting in flag; transmit path is disabled
H	L	X	L	NA	NA	H	EVEN	H	NA	NA	L	
H	L	X	L	NA	NA	L	ODD	L	NA	NA	H	
H	L	X	L	NA	NA	L	EVEN	L	NA	NA	L	
H	L	H	H	NA	NA	X	X	X	NA	NA	Store	Store the state of the error flag latch
X	X	L	H	X	X	X	X	X	NA	NA	H	Clear error flag latch
H	H	H	H	X	X	X	X	Z	Z	Z	Store	Transmit and receive paths are disabled. Prity logic in transmit mode
H	H	L	H	X	X	X	X	Z	Z	Z	H	
H	H	X	L	L	ODD	X	X	Z	Z	Z	H	
H	H	X	L	H	EVEN	X	X	Z	Z	Z	L	
L	L	X	X	H	ODD	NA	NA	NA	H	H	NA	Error checking
L	L	X	X	H	EVEN	NA	NA	NA	H	L	NA	
L	L	X	X	L	ODD	NA	NA	NA	L	H	NA	
L	L	X	X	L	EVEN	NA	NA	NA	L	L	NA	
L	L	H	X	H	H(Odd)		NA	NA	H	H	L	Error checking
L	L	H	X	H	H(Even)		NA	NA	H	L	H	
L	L	H	X	L	L(Odd)		NA	NA	L	H	L	
L	L	H	X	L	L(even)		NA	NA	L	L	H	

NOTES :
1.. Output state assumes HIGH output before the state.
2. Odd = Odd number of logic one's
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   i = 0,1,2,3,4,5,6,7
   X = Don't care

833 ERROR FLAG OUTPUT FUNCTION

Inputs		Internal to Device	Output Pre-state	Output	Function
$\overline{CLR}$	CLK	Point"P"	$\overline{ERR}$ n-1	$\overline{ERR}$	
H	↑	H	H	H	Sample
H	↑	—	L	L	(1's
H	↑	L	—	L	Capture)
L	—	—	—	H	Clear

Note: $\overline{OET}$ is HIGH and $\overline{OER}$ is LOW

853 ERROR FLAG OUTPUT

Input		Internal to	Output Pre-stat	Outpu	Function
$\overline{CLR}$	$\overline{EN}$	Point"P"	$\overline{ERR}$ n-1	$\overline{ERR}$	
L	L	L	X	L	Sample
L	L	H	X	H	Sample
L	H	L	X	L	Sample
L	L	X	L	L	Sample
L	H	H	H	H	Sample
H	L	X	X	H	Sample
H	H	X	L	L	Sample
H	H	X	H	H	Sample

Note: $\overline{OET}$ is HIGH and $\overline{OER}$ is LOW

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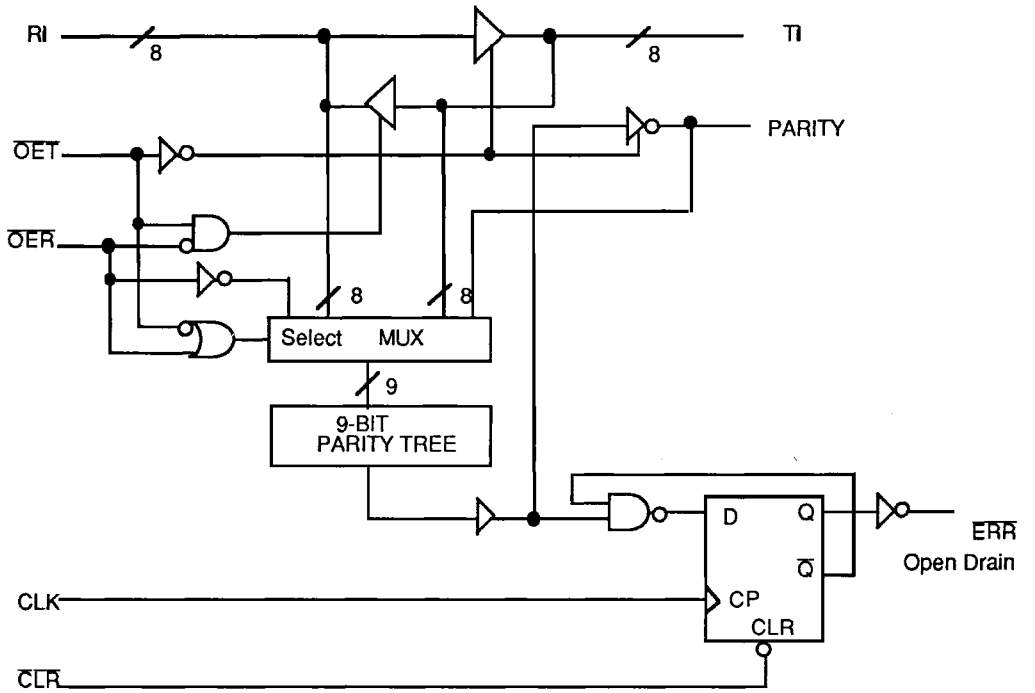
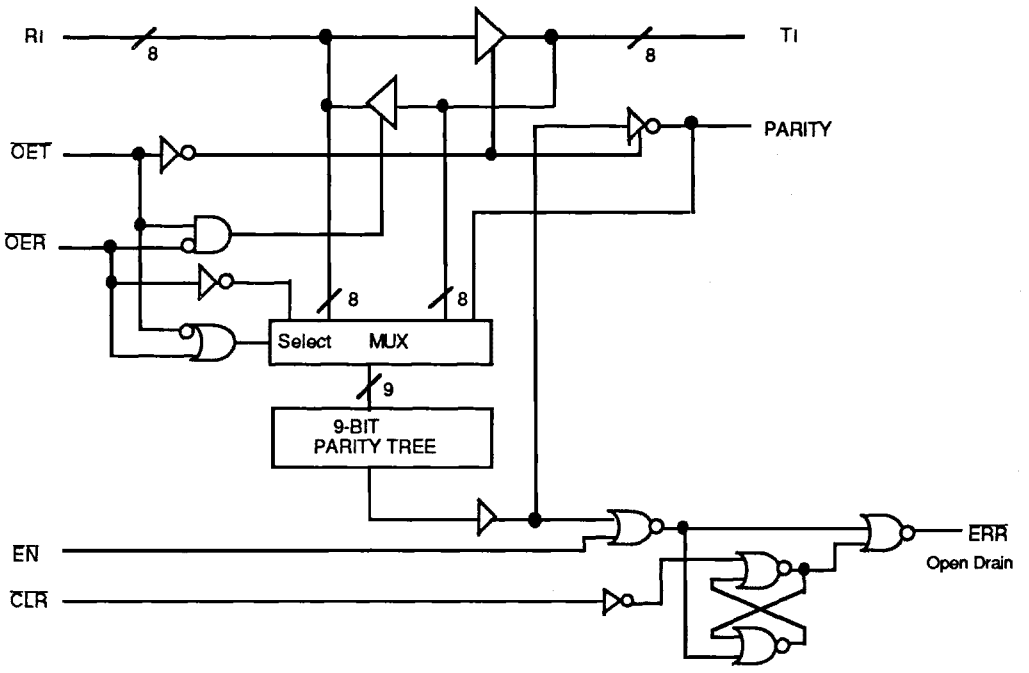
FCT833 LOGIC DIAGRAM



FCT853 LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground..... -0.5V to +7.0V
DC Output Voltage V_O ..... -0.5V to 7.0V
DC Input Voltage V_I ..... -0.5V to 7.0V
AC Input Voltage (for a pulse width ≤20 ns)..... -3.0V
DC Input Diode Current with V_I<0..... -20 mA
DC Output Diode Current with V_O <0..... -50 mA
DC Output Current Max. sink current/pin..... 120 mA
N=Number of Outputs, M=Number of inputs
Maximum Power Dissipation.....0.5 watts
T_{STG}Storage Temperature..... -65° to +165°C

CAPACITANCE

TA = 25 °C, f = 1 MHz, Vin = 0V, Vout = 0 V

Pins	SOIC	QSOP	PDIP,LCC	ZIP	Unit
ALL I/OS	8	8	9	10	pF

Note: Capacitance is characterized but not tested

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A=0°C to 70°C, V_{CC}=5.0V±5% Military T_A=-55°C to 125°C, V_{CC}=5.0V±10%

Symbol	Parameter	Test Conditions		Min	Typ (1)	Max	Unit
Vih	Input High Voltage	Logic HIGH for All Inputs		2.0	-	-	Volts
Vil	Input LOW Voltage	Logic LOW for All Inputs		-	-	0.8	
ΔVt	Input Hysterisis	Vtlh - Vthl for All Inputs		-	0.2	-	
| Iih | | Iil |	Input Current Input HIGH or LOW	Vcc = MAX	0 ≤ Vin < Vcc	-	-	5	µA
| Ioz |	Off State Output Current (Hi-Z)	Vcc = MAX, 0 ≤ Vin ≤ Vcc		-	-	5	
Ios	Short Circuit Current FCTXXX	Vcc = MAX, Vo = GND (2,3)		-60	-	-225	mA
Ior	Current Drive FCT2XXX	Vcc = Min, Vo =2.0V (3)		50	-	-	mA
Vic	Input Clamp Voltage	Vcc = MIN, Iin = 18 mA (3)		-	-0.7	-1.2	Volts
Voh	Output HIGH Voltage FCTXXX & FCT2XXX	Vcc = MIN	Ioh = 12 mA (MIL)	2.4	-	-	Volts
			Ioh = 15 mA (COM)	2.4	-	-	
Vol	Output LOW Voltage FCTXXX	Vcc = MIN	Iol = 32 mA (MIL)	-	-	0.50	
			Iol = 48 mA (COM)	-	-	0.50	
	Output LOW Voltage FCT2XXX (25Ω)	Vcc = MIN	Iol = 12 mA (MIL)	-	-	0.50	
			Iol = 12 mA (COM)	-	-	0.50	
Rout	Output Resistance FCT2XXX (25Ω)	Vcc = MIN	Iol = 12 mA (MIL)	-	25	-	Ω
			Iol = 12 mA (COM)	20	28	40	

Notes:
1. Typical values indicate V_{CC}=5.0V and T_A=25°C.
2. Not more than one output should be shorted and the duration is ≤1 second.
3. These parameters are guaranteed by design but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
Icc	Quiescent Power Supply Current	Vcc = MAX, freq = 0 0V≤Vin≤0.2V or Vcc-0.2V≤Vin≤Vcc	-	1.5	mA
ΔIcc	Supply Current per Input @ TTL HIGH	Vcc = MAX, Vin =3.4 V, freq = 0 (2)	-	2.0	
Qccd	Supply Current per input per mHz	Vcc = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or Vcc (3,4)	-	0.25	mA/ MHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input (Vi=3.4V)
3. For flipflops Qccd is measured by switching one of the data in pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. Ic can be computed using the above parameters as explained in the Technical Overview section.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A=0°C to 70°C, V_{CC}=5.0V±5% Military T_A=-55°C to 125°C, V_{CC}=5.0V±10%
Cload = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description	Notes	833AT,853AT, 2833AT, 2853AT				833AT,853AT, 2833AT, 2853AT				2/833CT, 2/853CT		Unit
			Com		Mil		Com		Mil		Com		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t PHL t PLH	Propagation Delay Ti to/fm Ri		-	10	-	14	-	7	-	10	-	5.5	ns
		3	-	17.5	-	21.5	-	14.5	-	17.5	-	11.5	
	Propagation Delay Ri to PARITY		-	15	-	20	-	10.5	-	14	-	9	
		3	-	22.5	-	27.5	-	21.5	-	27.5	-	19.5	
	Propagation Delay CLK to $\overline{ERR}$		-	12	-	16	-	8.5	-	11	-	7	
	Propagation Delay CLR to $\overline{ERR}$		-	16	-	20	-	15	-	18	-	13	
	Propagation Delay $\overline{OER}$ to PARITY		-	15	-	20	-	10.5	-	14	-	9	
		3	-	22.5	-	27.5	-	18	-	21.5	-	15	
t PZH t PZL	Output Enable Time $\overline{OER}$, $\overline{OET}$ to Ri, Ti		-	12	-	16	-	8.5	-	11	-	8.5	
		3	-	19.5	-	23.5	-	16	-	18.5	-	16	
tPHZ tPLZ	Output Disable Time $\overline{OER}$, $\overline{OET}$ to Ri, Ti		-	10.7	-	14.7	-	7.2	-	9.8	-	7.2	
		3	-	12	-	16	-	8.5	-	11	-	8.5	
tSU	Ti PARITY to CLK setup		12	-	16	-	8.5	-	11	-	8	-	
tH	Ti PARITY to CLK Hold		0	-	0	-	0	-	0	-	0	-	
tREM	$\overline{CLR}$ to CLK recovery		15	-	20	-	10.5	-	14	-	9	-	
tW	Clock pulse width	2	7	-	9.5	-	5.5	-	7	-	5	-	
tW	$\overline{CLR}$ pulse width	2	7	-	9.5	-	5.5	-	7	-	5	-	

Notes:
1) See Test Circuit and Waveforms.
2) This parameter is guaranteed by design but not tested.
3) Cload = 300pF