



# CY54/74FCT2646T CY54/74FCT2648T

## 8-Bit Registered Transceivers

### Features

- Function and pinout compatible with FCT and F logic
- FCT-C speed at 5.4 ns max. (Com'l)  
FCT-A speed at 6.3 ns max. (Com'l)
- Reduced  $V_{OH}$  (typically = 3.3V) versions of equivalent FCT functions
- 25Ω output series resistors to reduce transmission line reflection noise
- Reduced  $V_{OH}$  (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Matched rise and fall times
- ESD > 2000V

- Fully compatible with TTL Input and output logic levels
- Sink current 12 mA (Com'l), 12 mA (Mil)
- Source current 15 mA (Com'l), 12 mA (Mil)
- Independent register for A and B buses
- Three-state output

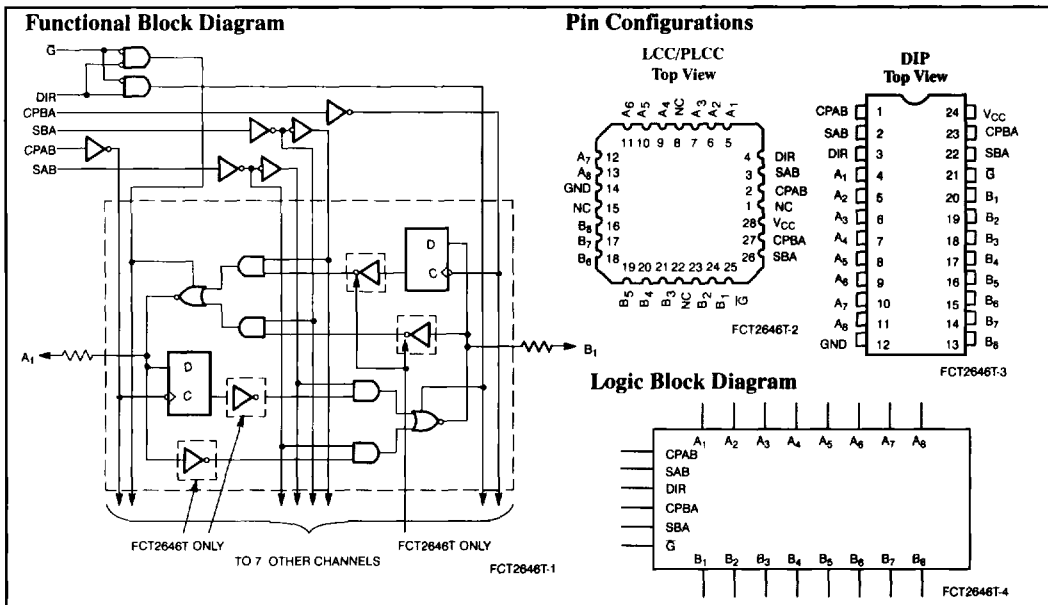
### Functional Description

The FCT2646T and FCT2648T consist of a bus transceiver circuit with three-state, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a HIGH logic level. Enable Control  $\bar{G}$  and direction pins are provided to control the

transceiver function. On-chip termination resistors have been added to the outputs to reduce system noise caused by reflections so that the FCT2646T and the FCT2648T can be used to replace the FCT646T and the FCT648T, respectively, in an existing design.

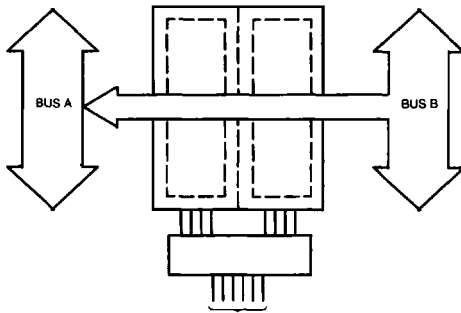
In the transceiver mode, data present at the high impedance port may be stored in either the A or B register, or in both. Select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control  $\bar{G}$  is Active LOW. In the isolation mode (enable control  $\bar{G}$  HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

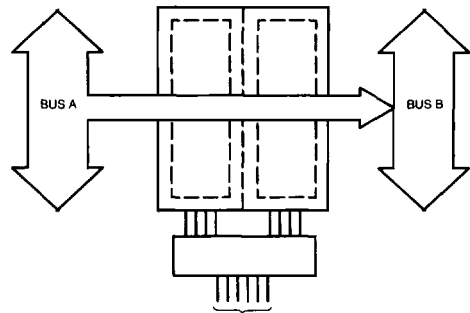


### Pin Description

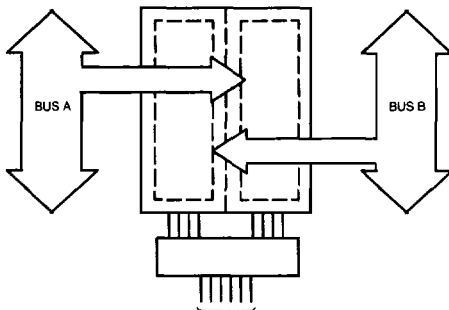
Name	Description
A	Data Register A Inputs, Data Register B Outputs
B	Data Register B Inputs, Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR, $\bar{G}$	Output Enable Inputs



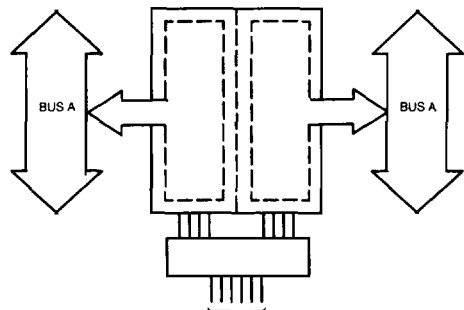
DIR L     $\bar{G}$  L    CPAB X    CPBA X    SAB X    SBA X  
Real-Time Transfer  
Bus B to Bus A



DIR H     $\bar{G}$  L    CPAB X    CPBA X    SAB L    SBA X  
Real-Time Transfer  
Bus A to Bus B



DIR H     $\bar{G}$  L    CPAB  $\downarrow$     CPBA X    SAB X    SBA X  
L    L     $\downarrow$      $\downarrow$     X    X  
X    H     $\downarrow$      $\downarrow$     X    X  
Storage from  
A and/or B



DIR<sup>(1)</sup> L     $\bar{G}$  L    CPAB X    CPBA H or L    SAB X    SBA H  
H    L    H or L    X    H    X  
Transfer Stored Data  
to A and/or B

Function Table<sup>[2]</sup>

Inputs						Data I/O <sup>[3]</sup>		Operation or Function	
$\bar{G}$	DIR	CPAB	CPBA	SAB	SBA	A <sub>1</sub> thru A <sub>8</sub>	B <sub>1</sub> thru B <sub>8</sub>	FCT2646T	FCT2648T
H	X	H or L	H or L	X	X	Input	Input	Isolation Store A and B Data	Isolation Store A and B Data
H	X	$\downarrow$	$\downarrow$	X	X				
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus	Real Time A Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored A Data to B Bus

Notes:

1. Cannot transfer data to A bus and B bus simultaneously.
2. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.
3. The data output functions may be enabled or disabled by various signals at the G or DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.



**Maximum Ratings**<sup>[4, 5]</sup>

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied ..... -65°C to +135°C  
 Supply Voltage to Ground Potential ..... -0.5V to +7.0V  
 DC Input Voltage ..... -0.5V to +7.0V  
 DC Output Voltage ..... -0.5V to +7.0V  
 DC Output Current (Maximum Sink Current/Pin) .... 120 mA  
 Power Dissipation ..... 0.5W

Static Discharge Voltage ..... >2001V  
 (per MIL-STD-883, Method 3015)

**Operating Range**

Range	Range	Ambient Temperature	V <sub>CC</sub>
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	T. AT	-40°C to +85°C	5V ± 5%
Military <sup>[6]</sup>	All	-55°C to +125°C	5V ± 10%

**Electrical Characteristics Over the Operating Range**

Parameter	Description	Test Conditions	Min.	Typ. <sup>[7]</sup>	Max.	Unit	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min., I <sub>OH</sub> =-15 mA	Com'l	2.4	3.3		V
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-12 mA	Mil	2.4	3.3		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min., I <sub>OL</sub> =12 mA	Com'l		0.3	0.55	V
		V <sub>CC</sub> =Min., I <sub>OL</sub> =12 mA	Mil		0.3	0.55	V
R <sub>OUT</sub>	Output Resistance	V <sub>CC</sub> =Min., I <sub>OL</sub> =12 mA	Com'l	20	25	40	Ω
		V <sub>CC</sub> =Min., I <sub>OL</sub> =12 mA	Mil		25		Ω
V <sub>IH</sub>	Input HIGH Voltage		2.0			V	
V <sub>IL</sub>	Input LOW Voltage				0.8	V	
V <sub>H</sub>	Hysteresis <sup>[8]</sup>	All inputs		0.2		V	
V <sub>IK</sub>	Input Clamp Diode Voltage	V <sub>CC</sub> =Min., I <sub>IN</sub> =-18 mA		-0.7	-1.2	V	
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> =Max., V <sub>IN</sub> =V <sub>CC</sub>			5	μA	
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> =Max., V <sub>IN</sub> =2.7V			±1	μA	
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> =Max., V <sub>IN</sub> =0.5V			±1	μA	
I <sub>OS</sub>	Output Short Circuit Current <sup>[9]</sup>	V <sub>CC</sub> =Max., V <sub>OUT</sub> =0.0V	-60	-120	-225	mA	
I <sub>OFF</sub>	Power-Off Disable	V <sub>CC</sub> =0V, V <sub>OUT</sub> =4.5V			±1	μA	

**Capacitance**<sup>[8]</sup>

Parameter	Description	Typ. <sup>[7]</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	6	10	pF
C <sub>OUT</sub>	Output Capacitance	8	12	pF

**Notes:**

- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V<sub>CC</sub> or ground.
- T<sub>A</sub> is the "instant on" case temperature.
- Typical values are at V<sub>CC</sub>=5.0V, T<sub>A</sub>=+25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

**Power Supply Characteristics**

Parameter	Description	Test Conditions	Typ. <sup>[7]</sup>	Max.	Unit
I <sub>CC</sub>	Quiescent Power Supply Current	V <sub>CC</sub> =Max., V <sub>IN</sub> ≤0.2V, V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	0.1	0.2	mA
ΔI <sub>CC</sub>	Quiescent Power Supply Current (TTL inputs HIGH)	V <sub>CC</sub> =Max., V <sub>IN</sub> =3.4V <sup>[10]</sup> f <sub>1</sub> =0, Outputs Open	0.5	2.0	mA
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>[11]</sup>	V <sub>CC</sub> =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, G=DIR=GND, GAB=GBA=GND, V <sub>IN</sub> ≤0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	0.06	0.12	mA/ MHz
I <sub>C</sub>	Total Power Supply Current <sup>[12]</sup>	V <sub>CC</sub> =Max., f <sub>0</sub> =10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f <sub>1</sub> =5 MHz, G=DIR=GND, GAB=GBA=GND, V <sub>IN</sub> ≤0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	0.7	1.4	mA
		V <sub>CC</sub> =Max., f <sub>0</sub> =10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f <sub>1</sub> =5 MHz, G=DIR=GND, GAB=GBA=GND, V <sub>IN</sub> =3.4V or V <sub>IN</sub> =GND	1.2	3.4	mA
		V <sub>CC</sub> =Max., f <sub>0</sub> =10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f <sub>1</sub> =5 MHz, G=DIR=GND, GAB=GBA=GND, V <sub>IN</sub> ≤0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	2.8	5.6 <sup>[13]</sup>	mA
		V <sub>CC</sub> =Max., f <sub>0</sub> =10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f <sub>1</sub> =5 MHz, G=DIR=GND, GAB=GBA=GND, V <sub>IN</sub> =3.4V or V <sub>IN</sub> =GND	5.1	14.6 <sup>[13]</sup>	mA

**Notes:**

10. Per TTL driven input (V<sub>IN</sub>=3.4V); all other inputs at V<sub>CC</sub> or GND.

11. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

12. I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>  
 I<sub>C</sub> = I<sub>CC</sub> + ΔI<sub>CC</sub>D<sub>H</sub>N<sub>T</sub> + I<sub>CCD</sub>(f<sub>0</sub>/2 + f<sub>1</sub>N<sub>I</sub>)  
 I<sub>CC</sub> = Quiescent Current with CMOS input levels  
 ΔI<sub>CC</sub> = Power Supply Current for a TTL HIGH input (V<sub>IN</sub>=3.4V)  
 D<sub>H</sub> = Duty Cycle for TTL inputs HIGH

N<sub>T</sub> = Number of TTL inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic Current caused by an input transition pair (HLH or LHL)

f<sub>0</sub> = Clock frequency for registered devices, otherwise zero

f<sub>1</sub> = Input signal frequency

N<sub>I</sub> = Number of inputs changing at f<sub>1</sub>

All currents are in milliamps and all frequencies are in megahertz.

13. Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.



Switching Characteristics Over the Operating Range

Parameter	Description	FCT2646T/FCT2648T				FCT2646AT/FCT2648AT				Unit	Fig. No. <sup>[15]</sup>
		Military		Commercial		Military		Commercial			
		Min. <sup>[14]</sup>	Max.	Min. <sup>[14]</sup>	Max.	Min. <sup>[14]</sup>	Max.	Min. <sup>[14]</sup>	Max.		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Bus to Bus	1.5	11.0	1.5	9.0	1.5	7.7	1.5	6.3	ns	1, 3
$t_{PZH}$ $t_{PZL}$	Output Enable Time Enable to Bus and DIR to A <sub>n</sub> or B <sub>n</sub>	1.5	15.0	1.5	14.5	1.5	10.5	1.5	9.8	ns	1, 7, 8
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time G to Bus and DIR to Bus	1.5	11.0	1.5	9.0	1.5	7.7	1.5	6.3	ns	1, 7, 8
$t_{PLH}$ $t_{PHL}$	Propagation Delay Clock to Bus	1.5	10.0	1.5	9.0	1.5	7.0	1.5	6.3	ns	1, 5
$t_{PLH}$ $t_{PHL}$	Propagation Delay SBA or SAB to A or B	1.5	12.0	1.5	11.0	1.5	8.4	1.5	7.7	ns	1, 5
$t_s$	Set-Up Time HIGH or LOW, Bus to Clock	4.5		4.0		2.0		2.0		ns	4
$t_H$	Hold Time HIGH or LOW, Bus to Clock	2.0		2.0		1.5		1.5		ns	4
$t_w$	Pulse Width, <sup>[6]</sup> HIGH or LOW	6.0		6.0		5.0		5.0		ns	5

Parameter	Description	FCT2646CT/FCT2648CT				Unit	Fig. No. <sup>[15]</sup>
		Military		Commercial			
		Min. <sup>[14]</sup>	Max.	Min. <sup>[14]</sup>	Max.		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Bus to Bus	1.5	6.0	1.5	5.4	ns	1, 3
$t_{PZH}$ $t_{PZL}$	Output Enable Time Enable to Bus and DIR to A <sub>n</sub> or B <sub>n</sub>	1.5	8.9	1.5	7.8	ns	1, 7, 8
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time G to Bus and DIR to Bus	1.5	7.7	1.5	6.3	ns	1, 7, 8
$t_{PLH}$ $t_{PHL}$	Propagation Delay Clock to Bus	1.5	6.3	1.5	5.7	ns	1, 5
$t_{PLH}$ $t_{PHL}$	Propagation Delay SBA or SAB to A or B	1.5	7.0	1.5	6.2	ns	1, 5
$t_s$	Set-Up Time HIGH or LOW, Bus to Clock	2.0		2.0		ns	4
$t_H$	Hold Time HIGH or LOW, Bus to Clock	1.5		1.5		ns	4
$t_w$	Pulse Width, <sup>[6]</sup> HIGH or LOW	5.0		5.0		ns	5

Notes:

14. Minimum limits are guaranteed but not tested on Propagation Delays.
15. See "Parameter Measurement Information" in the General Information Section.



**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	CY74FCT2646CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2646CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT2646CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
6.0	CY54FCT2646CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT2646CTLMB	L64	28-Square Leadless Chip Carrier	
6.3	CY74FCT2646ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2646ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT2646ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.7	CY54FCT2646ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT2646ATLMB	L64	28-Square Leadless Chip Carrier	
9.0	CY74FCT2646TPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2646TQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT2646TSOC	S13	24-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT2646TDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT2646TLMB	L64	28-Square Leadless Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	CY74FCT2648CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2648CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT2648CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
6.0	CY54FCT2648CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT2648CTLMB	L64	28-Square Leadless Chip Carrier	
6.3	CY74FCT2648ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2648ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT2648ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.7	CY54FCT2648ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT2648ATLMB	L64	28-Square Leadless Chip Carrier	
9.0	CY74FCT2648TPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2648TQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT2648TSOC	S13	24-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT2648TDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT2648TLMB	L64	28-Square Leadless Chip Carrier	

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