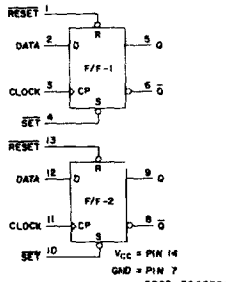


CD54/74HC74 CD54/74HCT74

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Dual D Flip-Flop with Set and Reset Positive-Edge Trigger

Type Features:

- Hysteresis on clock inputs for improved noise immunity and increased input Rise and Fall times.
- Asynchronous Set and Reset
- Complementary Outputs
- Buffered Inputs
- Typical $I_{max} = 50 \text{ MHz} @ V_{CC} = 5 \text{ V}, C_L = 15 \text{ pF}, T_A = 25^\circ \text{ C}$

The RCA-CD54/74HC74 and CD54/74HCT74 utilize silicon-gate CMOS technology to achieve operating speeds equivalent to LSTTL parts. They exhibit the low power consumption of standard CMOS integrated circuits, together with the ability to drive 10 LSTTL Loads.

This flip-flop has independent DATA, SET, RESET and CLOCK inputs and Q and Q-bar outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. SET and RESET are independent of the clock and are accomplished by a low level at the appropriate input.

The 54HCT/74HCT logic family is functionally as well as pin compatible with the standard 54LS/74LS logic family.

The CD54HC74 and CD54HCT74 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC74 and CD74HCT74 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- Fanout (Over Temperature Range):
Standard Outputs - 10 LSTTL Loads
Bus Driver Outputs - 15 LSTTL Loads
- Wide Operating Temperature Range:
CD74HC/HCT: -40 to +85°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips/Signetics
- CD54HC/CD74HC Types:
2 to 6 V Operation
High Noise Immunity:
 $N_{IL} = 30\%, N_{IH} = 30\% \text{ of } V_{CC} @ V_{CC} = 5 \text{ V}$
- CD54HCT/CD74HCT Types:
4.5 to 5.5 V Operation
Direct LSTTL Input Logic Compatibility
 $V_{IL} = 0.8 \text{ V Max.}, V_{IH} = 2 \text{ V Min.}$
CMOS Input Compatibility
 $I_L \leq 1 \mu\text{A} @ V_{OL}, V_{OH}$

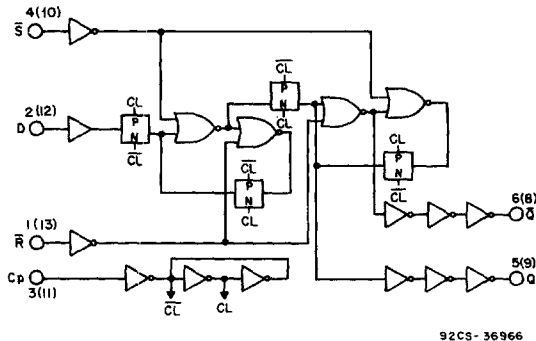


Fig. 1 — Logic Diagram

TRUTH TABLE

INPUTS				OUTPUTS	
SET	RESET	CP	D	Q	Q-bar
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	—	H	H	L
H	H	—	L	L	H
H	H	L	X	Q0	Q0-bar

H = High Level (Steady State)
L = Low Level (Steady State)
X = Don't Care
— = Transition from Low to High level

NOTES: Q0 = the level of Q before the indicated input conditions were established.

*This configuration is nonstable, that is, it will not persist when set and reset inputs return to their inactive (high) level.

CD54/74HC74 CD54/74HCT74

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V _{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I _{IK} (FOR V _i < -0.5 V OR V _i > V _{CC} + 0.5V)	±20mA
DC OUTPUT DIODE CURRENT, I _{OK} (FOR V _o < -0.5 V OR V _o > V _{CC} + 0.5V)	±20mA
DC DRAIN CURRENT, PER OUTPUT (I _O) (FOR -0.5 V < V _o < V _{CC} + 0.5V)	±25mA
DC V _{CC} OR GROUND CURRENT (I _{CC})	±50mA
POWER DISSIPATION PER PACKAGE (P ₀):	
For T _A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T _A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T _A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T _A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T _A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T _A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T _A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T _{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

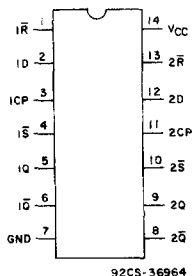
RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T _A = Full Package Temperature Range) V _{CC} * CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V _{in} , V _{out}	0	V _{CC}	V
Operating Temperature T _A : CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times t _r , t _f • at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

•Applicable for all inputs except clock.



TERMINAL ASSIGNMENT

CD54/74HC74
CD54/74HCT74

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC74/CD54HC74										CD74HCT74/CD54HCT74								UNITS			
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES			TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES			54HCT TYPES		
	V _I V	I _D mA	V _{CC} V	+25° C			-40/ +85° C		-55/ +125° C			V _I V	V _{CC} V	+25° C			-40/ +85° C			-55/ +125° C		
				Min	Typ	Max	Min	Max	Min	Max	Min			Typ	Max	Min	Max	Min		Max		
High-Level Input Voltage V _{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5	to	2	—	—	2	—	2	—	V	
			4.5	3.15	—	—	3.15	—	3.15	—	—	5.5										
			6	4.2	—	—	4.2	—	4.2	—	—											
Low-Level Input Voltage V _{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5	to	—	—	0.8	—	0.8	—	0.8	V	
			4.5	—	—	1.35	—	1.35	—	1.35	—	5.5										
			6	—	—	1.8	—	1.8	—	1.8	—											
High-Level Output Voltage V _{OH}	V _{IL}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V _I	4.5	4.4	—	—	4.4	—	4.4	—	4.4	V	
or			4.5	4.4	—	—	4.4	—	4.4	—	or	5.5										
CMOS Loads	V _{IH}		6	5.9	—	—	5.9	—	5.9	—	V _{IH}											
TTL Loads	V _{IL}										V _{IL}	4.5	3.98	—	—	3.84	—	3.7	—	—	V	
or		-4	4.5	3.98	—	—	3.84	—	3.7	—	or	5.5										
	V _{IH}	-5.2	6	5.48	—	—	5.34	—	5.2	—	V _{IH}											
Low-Level Output Voltage V _{OL}	V _{IL}	0.02	2	—	—	0.1	—	0.1	—	0.1	V _I	4.5	—	—	0.1	—	0.1	—	0.1	—	V	
or			4.5	—	—	0.1	—	0.1	—	0.1	—	5.5										
CMOS Loads	V _{IH}		6	—	—	0.1	—	0.1	—	0.1	—	V _{IH}										
TTL Loads	V _{IL}										V _{IL}	4.5	—	—	0.26	—	0.33	—	0.4	—	V	
or		4	4.5	—	—	0.26	—	0.33	—	0.4	or	5.5										
	V _{IH}	5.2	6	—	—	0.26	—	0.33	—	0.4	V _{IH}											
Input Leakage Current I _I	V _{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V _{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	—	μA	
Quiescent Device Current I _{CC}	V _{CC} or Gnd	0	6	—	—	4	—	40	—	80	V _{CC} or Gnd	5.5	—	—	4	—	40	—	80	—	μA	
Additional Quiescent Device Current per input pin: 1 unit load ΔI _{CC} *											V _{CC} -2.1 to 5.5	4.5 to	—	100	360	—	450	—	490	—	μA	

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
D	0.5
\bar{R}	0.5
CP	0.7
\bar{S}	0.75

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart.
e.g., 360 μA max. @ 25° C.

CD54/74HC74 CD54/74HCT74

SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 6\text{ ns}$)

CHARACTERISTIC	SYMBOL	C _L (pF)	TYPICAL		UNITS
			HC	HCT	
Propagation Delay CP to Q, \bar{Q} (Fig. 2) \bar{R} to Q, \bar{Q} (Fig. 3) \bar{S} to Q, \bar{Q} (Fig. 3)	t _{PLH} t _{PHL}	15	14	14	ns
			17	17	
			17	17	
CP Frequency	f _{MAX}	15	50	50	MHz
Power Dissipation Capacitance*	C _{PD}	—	25	30	pF

*C_{PD} is used to determine the dynamic power consumption, per flip-flop

PD = C_{PD} V_{CC}² f_i + Σ (C_L V_{CC}² f_o) where: f_i = input frequency

f_o = output frequency

C_L = output load capacitance

V_{CC} = supply voltage

PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	TEST CONDITIONS V _{CC} (V)	LIMITS										UNITS		
		25°C				-40°C to +85°C				-55°C to +125°C				
		HC		HCT		74HC		74HCT		54HC			54HCT	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Data to CP Set-up Time (Fig. 4)	t _{SU}	2	60	—	—	—	75	—	—	—	90	—	—	—
		4.5	12	—	12	—	15	—	15	—	18	—	18	—
		6	10	—	—	—	13	—	—	—	15	—	—	—
Hold Time (Fig. 4)	t _H	2	3	—	—	—	3	—	—	—	3	—	—	—
		4.5	3	—	3	—	3	—	3	—	3	—	3	—
		6	3	—	—	—	3	—	—	—	3	—	—	—
Removal Time \bar{R} , \bar{S} to CP (Fig. 3)	t _{REM}	2	30	—	—	—	40	—	—	—	45	—	—	—
		4.5	6	—	6	—	8	—	8	—	9	—	9	—
		6	5	—	—	—	7	—	—	—	8	—	—	—
Pulse Width \bar{R} , \bar{S} (Figs. 2, 3)	t _w	2	80	—	—	—	100	—	—	—	120	—	—	—
		4.5	16	—	16	—	20	—	20	—	24	—	24	—
		6	14	—	—	—	17	—	—	—	20	—	—	—
Pulse Width CP (Figs. 2, 3)	t _w	2	80	—	—	—	100	—	—	—	120	—	—	—
		4.5	16	—	18	—	20	—	23	—	24	—	27	—
		6	14	—	—	—	17	—	—	—	20	—	—	—
CP Frequency	f _{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—
		4.5	30	—	25	—	25	—	20	—	20	—	16	—
		6	35	—	—	—	29	—	—	—	23	—	—	—

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	V _{CC} (V)	LIMITS										UNITS		
		25°C				-40°C to +85°C				-55°C to +125°C				
		HC		HCT		74HC		74HCT		54HC			54HCT	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, CP to Q, \bar{Q} (Fig. 2)	t _{PLH}	2	—	175	—	—	—	220	—	—	—	265	—	—
	t _{PHL}	4.5	—	35	—	35	—	44	—	44	—	53	—	53
		6	—	30	—	—	—	37	—	—	—	45	—	—
\bar{R} , \bar{S} to Q, \bar{Q} (Fig. 3)	t _{PHL}	2	—	200	—	—	—	250	—	—	—	300	—	—
	t _{PLH}	4.5	—	40	—	40	—	50	—	50	—	60	—	60
		6	—	34	—	—	—	43	—	—	—	51	—	—
Transition Times (Fig. 5)	t _{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—
	t _{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22
		6	—	13	—	—	—	16	—	—	—	19	—	—
Input Capacitance	C _i	—	—	10	—	10	—	10	—	10	—	10	—	10

CD54/74HC74 CD54/74HCT74

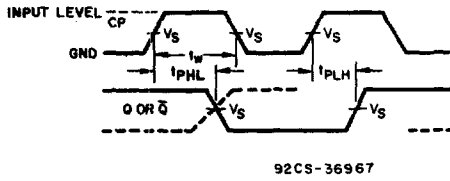


Fig. 2 — Clock pre-requisite and propagation delays.

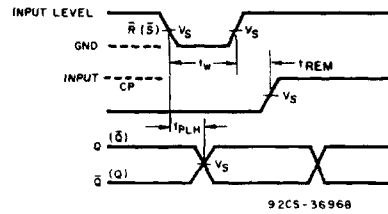


Fig. 3 — $\overline{\text{Reset}}$ or $\overline{\text{Set}}$ pre-requisite and propagation delays

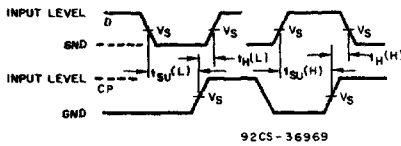


Fig. 4 — Data pre-requisite times.

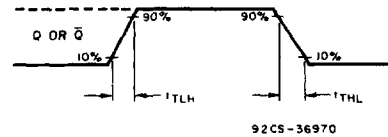


Fig. 5 — Output transition times.

	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3V
V_S	50% V_{CC}	1.3V