Order number: MC100ES7014
Rev 1, 05/2004

Product Preview

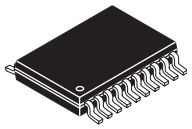
Low Voltage 1:5 Differential LVDS Clock Fanout Buffer

MC100ES7014

1:5 DIFFERENTIAL LVDS CLOCK FANOUT DRIVER

The MC100ES7014 is a LVDS differential clock fanout buffer. Designed for the most demanding clock distribution systems, the MC100ES7014 supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver are in high performance clock distribution in computing, networking and telecommunication systems.

The MC100ES7014 is designed for low skew clock distribution systems and supports clock frequencies up to 1000MHz. The device accepts two clock sources. The CLK0 input accepts LVDS or HSTL compatible signals and CLK1 accepts PECL compatible signals. The selected input signal is distributed to 5 identical, differential LVDS compatible outputs.



DT SUFFIX
20-LEAD TSSOP PACKAGE
CASE 948E-02

Features

- 1:5 differential clock fanout buffer
- 50 ps maximum device skew
- SiGe Technology
- Supports DC to 1000 MHz operation
- LVDS compatible differential clock outputs
- PECL and HSTL/LVDS compatible differential clock inputs
- 3.3V power supply
- Supports industrial temperature range
- Standard 20 lead TSSOP package

ORDERING INFORMATION

Device	Package
MC100ES7014DT	TSSOP-20
MC100ES7014DTR2	TSSOP-20

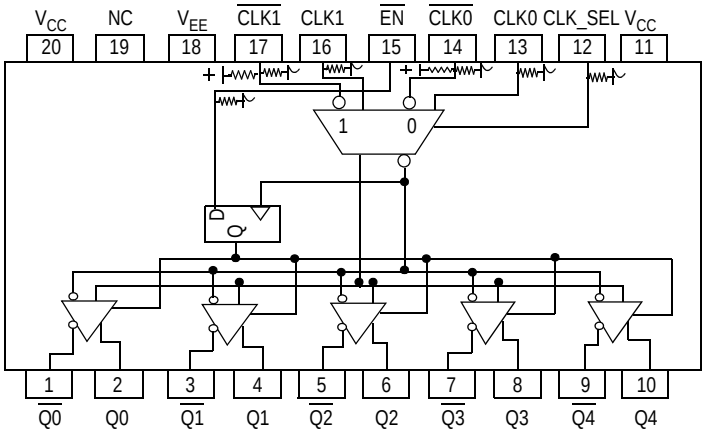


Figure 1. 20-Lead Pinout (Top View) **and Logic Diagram**

This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

Table 1. Pin Description

Pin	Function
CLK0, $\overline{\text{CLK0}}$	HSTL/LVDS Data Inputs
CLK1, $\overline{\text{CLK1}}$	PECL Data Inputs
Q[0:4], $\overline{\text{Q[0:4]}}$	LVDS Data Outputs
CLK_SEL	LVCMOS Active Clock Select Input
$\overline{\text{EN}}$	LVCMOS Sync Enable
V_{CC}	Positive Supply
V_{EE}	Negative Supply
nc	no connect

Table 2. Function Table

Control	Default	0	1
CLK_SEL	0	CLK0, $\overline{\text{CLK0}}$ (HSTL/LVDS) is the active differential clock input	CLK1, $\overline{\text{CLK1}}$ (PECL) is the active differential clock input
$\overline{\text{EN}}$	0	Q[0:4], $\overline{\text{Q[0:4]}}$ are active. Deassertion of $\overline{\text{EN}}$ can be asynchronous to the reference clock without generation of output runt pulses.	Q[0:4] = L, $\overline{\text{Q[0:4]}}$ = H (outputs disabled). Assertion of $\overline{\text{EN}}$ can be asynchronous to the reference clock without generation of output runt pulses.

Table 3. General Specifications

Characteristics		Value
Internal Input Pulldown Resistor		TBD
Internal Input Pullup Resistor		TBD
ESD Protection	Human Body Model Machine Model	TBD
θ_{JA} Thermal Resistance (Junction to Ambient)	0 LFPM, 8 SOIC 500 LFPM, 8 SOIC	TBD

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

Table 4. Absolute Maximum Ratings[1]

Symbol	Parameter	Conditions	Rating	Unit
V_{SUPPLY}	Power Supply Voltage	Difference between V_{CC} & V_{EE}	3.9	V
V_{IN}	Input Voltage	$V_{CC} - V_{EE} \leq 3.6V$	V_{CC} + 0.3 V_{EE} – 0.3	V V
I_{OUT}	Output Current	Continuous Surge	50 100	mA mA
T_A	Operating Temperature Range		–40 to +85	°C
T_{STG}	Storage Temperature Range		–65 to +150	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. DC Characteristics (V_{CC} = 3.3V±5%; T_J = 0°C to 110°C)[1]

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
HSTL/LVDS differential input signals (CLK0, $\overline{CLK0}$)						
V_{DIF}	Differential Input Voltage[2]	0.2			V	
$V_{X, IN}$	Differential Cross Point Voltage[3]	0.25	0.68 – 0.9	V_{CC} – 1.3	V	
V_{IH}	Input High Voltage	V_X + 0.1			V	
V_{IL}	Input Low Voltage			V_X – 0.1	V	
I_{IN}	Input Current			±150	mA	V_{IN} = V_X ± 0.1V
PECL differential input signals (CLK1, $\overline{CLK1}$)						
V_{PP}	Differential input Voltage[4]	0.15		1.0	V	Differential Operation
V_{CMR}	Differential Cross Point Voltage[5]	1.0		V_{CC} – 0.6	V	Differential Operation
V_{IH}	Input High Voltage	V_{CC} – 1.165		V_{CC} – 0.880	V	
V_{IL}	Input Low Voltage	V_{CC} – 1.810		V_{CC} – 1.475	V	
I_{IN}	Input Current			±150	mA	V_{IN} = V_{IH} or V_{IN}
LVCMOS control inputs $\overline{EN}$, CLK_SEL						
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
I_{IN}	Input Current			±150	mA	V_{IN} = V_{IH} or V_{IN}
LVDS clock outputs (Q[0:4], $\overline{Q[0:4]}$)						
V_{PP}	Output Differential Voltage (peak-to-peak)	250			mV	LVDS
V_{OS}	Output Offset Voltage	1125		1275	mV	LVDS
Supply Current						
I_{CC}	Maximum Quiescent Supply Current without output termination current		TBD	TBD	mA	V_{CC} pin (core)

1. DC characteristics are design targets and pending characterization.
2. V_{DIF} (DC) is the minimum differential HSTL/LVDS input voltage swing required for device functionality.
3. V_X (DC) is the crosspoint of the differential HSTL/LVDS input signal. Functional operation is obtained when the crosspoint is within the V_X (DC) range and the input swing lies within the V_{PP} (DC) specification.
4. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
5. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 6. AC Characteristics (V_{CC} = 3.3V±5%; T_J = 0°C to 110°C)[1 2]

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
HSTL/LVDS differential input signals (CLK0, $\overline{CLK0}$)						
V_{DIF}	Differential Input Voltage (peak-to-peak)[3]	0.4			V	
$V_{X, IN}$	Differential Cross Point Voltage[4]	0.68		1.275	V	
f_{CLK}	Input Frequency		1000	TBD	MHz	Differential
t_{PD}	Propagation Delay			TBD	ps	Differential
PECL differential input signals (CLK1, $\overline{CLK1}$)						
V_{PP}	Differential Input Voltage (peak-to-peak)[5]	0.2		1.0	V	
V_{CMR}	Differential Cross Point Voltage[6]	1		V_{CC} – 0.6	V	
f_{CLK}	Input Frequency		1000		MHz	Differential
t_{PD}	Propagation Delay			TBD	ps	Differential
LVDS clock outputs (Q[0:4], $\overline{Q[0:4]}$)						
$t_{SK(O)}$	Output-to-Output Skew			50	ps	Differential
$t_{SK(PP)}$	Output-to-Output Skew (part-to-part)			TBD	ps	Differential
$t_{JIT(CC)}$	Output Cycle-to-Cycle Jitter			TBD		
DC_O	Output Duty Cycle	TBD	50	TBD	%	DC_{fref} = 50%
t_r / t_f	Output Rise/Fall Times	0.05		TBD	ns	20% to 80%
t_{PDL}	Output Disable Time[7]	2.5*T +t_{PD}		3.5*T +t_{PD}	ns	T = CLK period
t_{PLD}	Output Enable Time[8]	3*T +t_{PD}		4*T +t_{PD}	ns	T = CLK period

1. AC characteristics are design targets and pending characterization.
2. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
3. V_{DIF} (AC) is the minimum differential HSTL/LVDS input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
4. V_X (AC) is the crosspoint of the differential HSTL/LVDS input signal. Functional operation is obtained when the crosspoint is within the V_X (AC) range and the input swing lies within the V_{DIF} (AC) specification. Violation of V_X (AC) or V_{DIF}(AC) impacts the device propagation delay, device and part-to-part skew.
5. V_{PP} (AC) is the minimum differential PECL input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
6. V_{CMR} (AC) is the crosspoint of the differential PECL input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP}(AC) impacts the device propagation delay, device and part-to-part skew.
7. Propagation delay $\overline{EN}$ deassertion to differential output disabled (differential low: true output low, complementary output high).
8. Propagation delay $\overline{EN}$ assertion to output enabled (active).

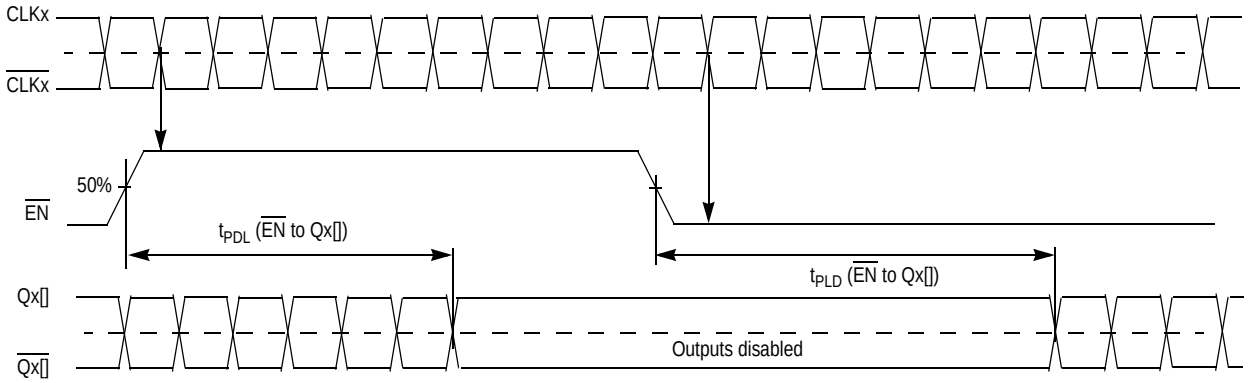


Figure 2. MC100ES7014 AC Test Reference

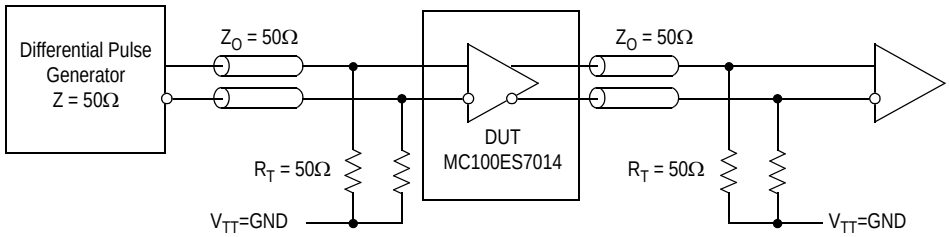


Figure 3. MC100ES7014 AC Test Reference

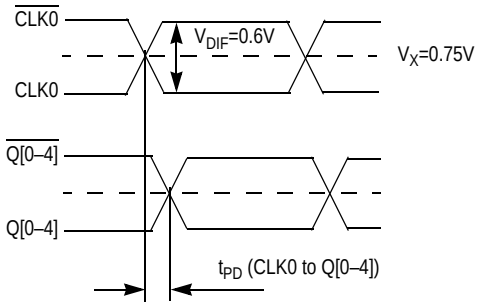


Figure 4. MC100ES7014 AC Reference Measurement Waveform (HSTL Input)

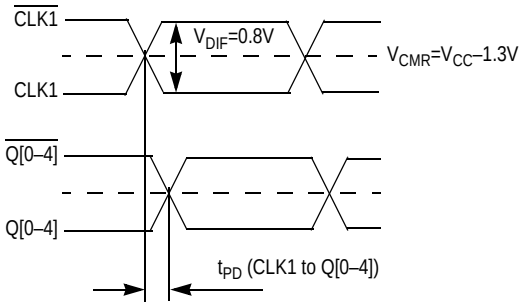


Figure 5. MC100ES7014 AC Reference Measurement Waveform (PECL Input)

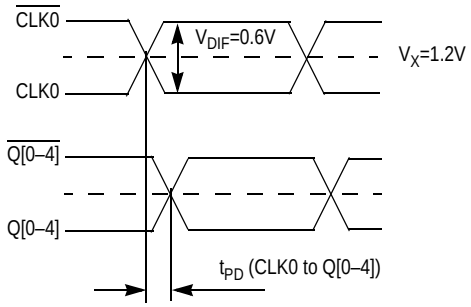


Figure 6. MC100ES7014 AC Reference Measurement Waveform (LVDS Input)