HARRIS

HI-574A

Fast, Complete 12-Bit A/D Converter with Microprocessor Interface

Features

- Complete 12-Bit A/D Converter with Reference and Clock
- Full 8-, 12- or 16-Bit Microprocessor Bus Interface
- 150ns Bus Access Time
- No Missing Codes Over Temperature
- Minimal Set-up Time for Control Signals
- 25μs Maximum Conversion Time
- Low Noise, via Current-Mode Signal Transmission Between Chips
- Byte Enable/Short Cycle (A_0 Input)
  - Guaranteed Break-Before-Make Action, Eliminating Bus Contention During Read Operation. Latched by the Start Convert Input (To Set the Conversion Length)
- Improved Second Source for AD574A and HS574
- $\pm$12V to $\pm$15V Operation

Applications

- Military and Industrial Data Acquisition Systems
- Electronic Test and Scientific Instrumentation
- Process Control Systems

Description

The HI-574A is a complete 12-bit Analog-to-Digital Converter, including a +10V reference, clock, three-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice housed in a 28 pin package. The bipolar analog die features the Harris Dielectric Isolation process, which provides enhanced AC performance and freedom from latch-up.

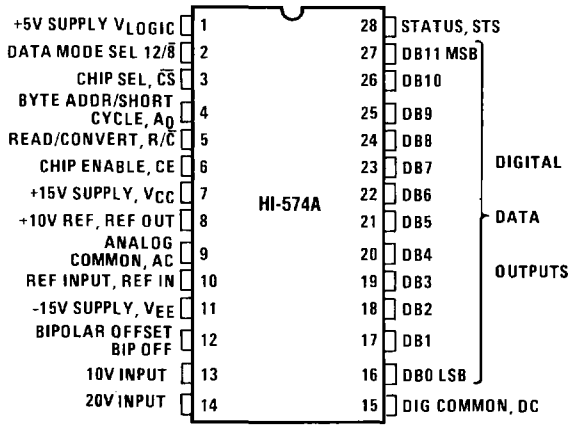
Custom design of each IC (bipolar analog and CMOS digital) has yielded improved performance over existing versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1 LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital IC's. Also, the clock oscillator is current-controlled for excellent stability over temperature. The oscillator is trimmed for a nominal conversion time of 20 $\pm$ 1μs.

The HI-574A offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity, gain and offset accuracy. The buried zener reference circuit is trimmed for minimum temperature coefficient.

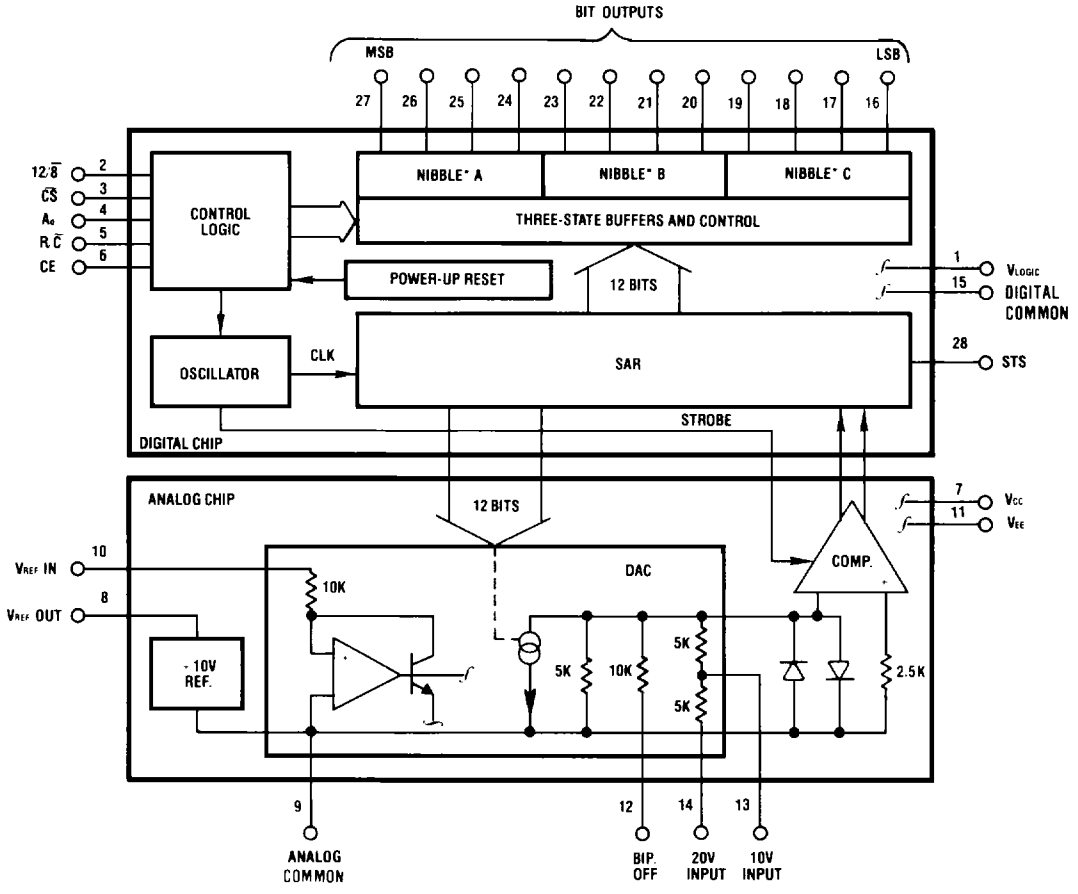
Power requirements are +5V and $\pm$12V to $\pm$15V, with typical dissipation of 385mW at $\pm$12V. All models are available in a 28 pin Sidebrazed DIP. For additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix. For MIL-STD-883 compliant parts, request the HI-574A/883 data sheet.

Pinouts

SIDEBRAZE DIP
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.



("NIBBLE" IS A 4 BIT DIGITAL WORD)

(Typical @ +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise specified)

DC and Transfer Accuracy Specifications

MODEL	HI-574AJ	HI-574AK	HI-574AL	UNITS
Temperature Range		-5		
Resolution (max)	12	12	12	Bits
Linearity Error				
25°C (max)	±1	±1/2	±1/2	LSB
0°C to +75°C (max)	±1	±1/2	±1/2	LSB
Differential Linearity Error				
(Maximum resolution for which no missing codes is guaranteed)				
25°C	11	12	12	Bits
T_{min} to T_{max}	11	12	12	Bits
Unipolar Offset (max)				
(Adjustable to zero)	±2	±2	±2	LSB
Bipolar Offset (max)				
(Adjustable to zero)	±10	±4	±4	LSB
Full Scale Calibration Error				
25°C (max), with fixed 50 Ω resistor from				
REF OUT to REF IN (Adjustable to zero)	0.3	0.3	0.3	% of F.S.
T_{min} to T_{max}				
(No adjustment at +25°C)	0.5	0.4	0.35	% of F.S.
(With adjustment to zero at +25°C)	0.22	0.12	0.05	% of F.S.
Temperature Coefficients				
Guaranteed max change, T_{min} to T_{max} (Using internal reference)				
Unipolar Offset	±2	±1	±1	LSB
	(10)	(5)	(5)	(ppm/°C)
Bipolar Offset	±2	±1	±1	LSB
	(10)	(5)	(5)	(ppm/°C)
Full Scale Calibration	±9	±5	±2	LSB
	(45)	(25)	(10)	(ppm/°C)
Power Supply Rejection				
Max change in Full Scale Calibration				
+13.5V<V_{CC}<+16.5V or +11.4V<V_{CC}<+12.6V	±2	±1	±1	LSB
+4.5V<V_{LOGIC}<+5.5V	±1/2	±1/2	±1/2	LSB
−16.5V<V_{EE}<−13.5V or −12.6V<V_{EE}<−11.4V	±2	±1	±1	LSB
Analog Inputs				
Input Ranges				
Bipolar		−5 to +5		Volts
		−10 to +10		Volts
Unipolar		0 to +10		Volts
		0 to +20		Volts
Input Impedance				
10 Volt Span		5K, ± 25%		Ohms
20 Volt Span		10K, ± 25%		Ohms
Power Supplies				
Operating Voltage Range				
V_{LOGIC}		+4.5 to +5.5		Volts
V_{CC}		+11.4 to +16.5		Volts
V_{EE}		−11.4 to −16.5		Volts
Operating Current				
I_{LOGIC}		7 TYP, 15 MAX		mA
I_{CC} +15V Supply		11 TYP, 15 MAX		mA
I_{EE} -15V Supply		21 TYP, 28 MAX		mA
Power Dissipation				
±15V, +5V		515 TYP, 720 MAX		mW
±12V, +5V		385 TYP		mW
Internal Reference Voltage, T_{min} to T_{max}		+10.00 ± 0.5 MAX		Volts
Output current,[1]		2.0 MAX		mA
available for external loads (External load				
should not change during conversion).				

[1] *When supplying an external load (not including the ADC) and operating on ±12V supplies, a buffer amplifier must be provided for the Reference Output.*

(Typical @ +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise specified)

DC and Transfer Accuracy Specifications

MODEL	HI-574AS	HI-574AT	UNITS
Temperature Range	-2, -8		
Resolution (max)	12	12	Bits
Linearity Error			
25°C (max)	±1	±1/2	LSB
−55°C to +125°C (max)	±1	±1	LSB
Differential Linearity Error			
(Maximum resolution for which no missing codes is guaranteed)			
25°C	11	12	Bits
T_{min} to T_{max}	11	12	Bits
Unipolar Offset (max)			
(Adjustable to zero)	±2	±2	LSB
Bipolar Offset (max)			
(Adjustable to zero)	±10	±4	LSB
Full Scale Calibration Error			
25°C (max), with fixed 50 Ω resistor from			
REF OUT to REF IN (Adjustable to zero)	0.3	0.3	% of F.S.
T_{min} to T_{max}			
(No adjustment at +25°C)	0.8	0.6	% of F.S.
(With adjustment to zero at +25°C)	0.5	0.25	% of F.S.
Temperature Coefficients			
Guaranteed max change, T_{min} to T_{max} (Using internal reference)			
Unipolar Offset	±2	±1	LSB
	(5)	(2.5)	(ppm/°C)
Bipolar Offset	±4	±2	LSB
	(10)	(5)	(ppm/°C)
Full Scale Calibration	±20	±10	LSB
	(50)	(25)	(ppm/°C)
Power Supply Rejection			
Max change in Full Scale Calibration			
+13.5V<V_{CC}<+16.5V or +11.4V<V_{CC}<+12.6V	±2	±1	LSB
+4.5V<V_{LOGIC}<+5.5V	±1/2	±1/2	LSB
−16.5V<V_{EE}<−13.5V or −12.6V<V_{EE}<−11.4V	±2	±1	LSB
Analog Inputs			
Input Ranges			
Bipolar	−5 to +5		Volts
	−10 to +10		Volts
Unipolar	0 to +10		Volts
	0 to +20		Volts
Input Impedance			
10 Volt Span	5K Ω, ± 25%		Ohms
20 Volt Span	10K Ω, ± 25%		Ohms
Power Supplies			
Operating Voltage Range			
V_{LOGIC}	+4.5 to +5.5		Volts
V_{CC}	+11.4 to +16.5		Volts
V_{EE}	−11.4 to −16.5		Volts
Operating Current			
I_{LOGIC}	7 TYP, 15 MAX		mA
I_{CC} +15V Supply	11 TYP, 15 MAX		mA
I_{EE} -15V Supply	21 TYP, 28 MAX		mA
Power Dissipation			
±15V, +5V	515 TYP, 720 MAX		mW
±12V, +5V	385 TYP		mW
Internal Reference Voltage, T_{min} to T_{max}	+10.00 ±.05 MAX		Volts
Output current,[1]	2.0 MAX		mA
available for external loads (External load should not change during conversion).			

1 When supplying an external load (not including the ADC) and operating on ±12V supplies a buffer amplifier must be provided for the Reference Output

DIGITAL CHARACTERISTICS[1]
(ALL MODELS, OVER FULL TEMP. RANGE)

	MIN	TYP	MAX
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, A0, 12/$\overline{8}$)[2]			
Logic "1"	+2.4V		+5.5V
Logic "0"	−0.5V		+0.8V
Current	−5μA	±0.1μA	+5μA
Capacitance		5pF	
Logic Outputs (DB11-DB0, STS)			
Logic "0" (I_{SINK} — 1.6mA)			+0.4V
Logic "1" (I_{SOURCE} — 500μA)	+2.4V		
Leakage (High - Z State, DB11-DB0 ONLY)	−5μA	±0.1μA	+5μA
Capacitance		5pF	

[1] *See "HI-574A Timing Specifications" for a detailed listing of digital timing parameters.*

[2] *Although this guaranteed threshold is higher than standard TTL (+2.0V), bus loading is much less, i.e., typical input current is only 0.25% of a TTL load.*

Absolute Maximum Ratings

(Specifications apply to all grades, except where noted)

V_{CC} to Digital Common ..... 0 to +16.5V
V_{EE} to Digital Common ..... 0 to −16.5V
V_{LOGIC} to Digital Common ..... 0 to +7V
Analog Common to Digital Common ..... ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to
Digital Common ..... −0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, 10V_{IN}) to
Analog Common ..... ±16.5V
20V_{IN} to Analog Common ..... ±24V
REF OUT ..... Indefinite short to common
Momentary short to V_{CC}
Junction Temperature ..... 175°C
Lead Temperature, Soldering ..... 300°C, 10 sec.
Storage Temperature ..... −65°C to +150°C

*Derate 20.8mW/°C above 75°C

HI-574A Ordering Guide

MODEL	TEMP. RANGE	LINEARITY ERROR MAX (T_{MIN} to T_{MAX})	RESOLUTION (NO MISSING CODES, T_{MIN} to T_{MAX})	FULL SCALE TC (PPM/°C MAX)
HI1-574AJD-5	0 to 75°C	±1 LSB	11 Bits	45.0
HI1-574AKD-5	0 to 75°C	±1/2 LSB	12 Bits	25.0
HI1-574ALD-5	0 to 75°C	±1/2 LSB	12 Bits	10.0
HI1-574ASD-2	−55 to +125°C	±1 LSB	11 Bits	50.0
HI1-574ASD-8*	−55 to +125°C	±1 LSB	11 Bits	50.0
HI1-574ATD-2	−55 to +125°C	±1 LSB	12 Bits	25.0
HI1-574ATD-8*	−55 to +125°C	±1 LSB	12 Bits	25.0

* *The MIL-STD-883 data sheet is available on request.*

Definitions of Specifications

LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs ½LSB (1.22mV for 10 volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1½LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HI-574AK, AL, AT, and AU grades are guaranteed for maximum nonlinearity of ±½LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HI-574AJ and AS grades are guaranteed to ±1LSB max error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR
(NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HI-574AK, AL, AT, and AU grades, which

Definitions of Specifications (Continued)

guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HI-574AJ and AS grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

UNIPOLAR OFFSET

The first transition should occur at a level ½LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

BIPOLAR OFFSET

Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value ½LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

FULL SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1½LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 2 and 3. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 volt reference.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{min} or T_{max}.

POWER SUPPLY REJECTION

The standard specifications for the HI-574A assume use of +5.00 and ±15.00 or ±12.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

CODE WIDTH

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10 volts for a 12-bit ADC.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±½LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

LEFT-JUSTIFIED DATA

The data format used in the HI-574A is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

Applying the HI-574A

For each application of this converter, the ground connections, power supply bypassing, analog signal source, digital timing and signal routing on the circuit board must be optimized to assure maximum performance. These areas are reviewed in the following sections, along with basic operating modes and calibration requirements.

PHYSICAL MOUNTING AND LAYOUT CONSIDERATIONS

Layout –

Unwanted, parasitic circuit components, (L, R, and C) can make 12 bit accuracy impossible, even with a perfect A/D converter. The best policy is to eliminate or minimize these parasitics through proper circuit layout, rather than try to quantify their effects.

The recommended construction is a double-sided printed circuit board with a ground plane on the component side. Other techniques, such as wire-wrapping or point-to-point wiring on vectorboard, will have an unpredictable effect on accuracy.

In general, sensitive analog signals should be routed between ground traces and kept well away from digital lines. If analog and digital lines must cross, they should do so at right angles.

Power Supplies

Supply voltages to the HI-574A (+15V, −15V and +5V) must be "quiet" and well regulated. Voltage spikes on these lines can affect the converter's accuracy, causing several LSB's to flicker when a constant input is applied. Digital noise and spikes from a switching power supply are especially troublesome. If switching supplies must be used, outputs should be carefully filtered to assure "quiet" DC voltage at the converter terminals.

Further, a bypass capacitor pair on each supply voltage terminal is necessary to counter the effect of variations in supply current. Connect one pair from pin 1 to 15 (V_{LOGIC} supply), one from pin 7 to 9 (V_{CC} to Analog Common) and one from pin 11 to 9 (V_{EE} to Analog Common). For each capacitor pair, a 10μF tantalum type in parallel with a 0.1μF ceramic type is recommended.

Ground Connections

The typical HI-574A ground currents are 5.5mADC into pin 9 (Analog Common)and 7mADC out of pin 15 (Digital Common). These pins should be tied together at the package to guarantee specified performance for the converter. In addition, a wide PC trace should run directly from pin 9 to (usually) 15V common, and from pin 15 to (usually) the +5V Logic Common. If the converter is located some distance from the system's "single point" ground, make only these connections to pins 9 and 15: Tie them together at the package, and back to the system ground with a single path. This path should have low resistance since it will carry about 1.5mA of DC current. (Code dependent currents flow in the V_{CC}, V_{EE} and V_{LOGIC} terminals, but not through the HI-574A's Analog Common or Digital Common).

ANALOG SIGNAL SOURCE

The device chosen to drive the HI-574A analog input will see a nominal load of 5KΩ (10V range) or 10KΩ (20V range). However, the other end of these input resistors may change ±400mV with each bit decision, creating abrupt changes in current at the analog input. Thus, the signal source must maintain its output voltage while furnishing these step changes in load current, which occur at 1.6μS intervals. This requires low output impedance and fast settling by the signal source.

The output impedance of an op amp, for example, has an open loop value which, in a closed loop, is divided by the loop gain available at a frequency of interest. The amplifier should have acceptable loop gain at 600KHz for use with the HI-574A. To check whether the output properties of a signal source are suitable, monitor the 574A's input (pin 13 or 14) with an oscilloscope while a conversion is in progress. Each of the twelve disturbances should subside in one microsecond or less. (The comparator decision is made about 1.5μS after each code change from the SAR).

If the application calls for a Sample/Hold to precede the converter, it should be noted that not all Sample/Holds are compatible with the HI-574A in the manner described above. These will require an additional wideband buffer amplifier to lower their output impedance. A simpler solution is to use the Harris HA-5320 Sample/Hold, which was designed for use with the HI-574A.

RANGE CONNECTIONS AND CALIBRATION PROCEDURES

The HI-574A is a "complete" A/D converter, meaning it is fully operational with addition of the power supply voltages, a Start Convert signal, and a few external components as shown in Figures 2 and 3. Nothing more is required for most applications.

Whether controlled by a processor or operating in the stand-alone mode, the HI-574A offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V and ±10V. The maximum errors for gain and offset are listed under Specifications. If required, however, these errors may be adjusted to zero as explained below. Power supply and ground connections have been discussed in an earlier section.

Unipolar Connections and Calibration –

Refer to Fig. 2. The resistors shown* are for calibration of offset and gain. If this is not required, replace R2 with a 50Ω, 1% metal film resistor and remove the network on pin 12. Connect pin 12 to pin 9. Then, connect the analog signal to pin 13 for the 0V to 10V range, or to pin 14 for the 0V to 20V range. Inputs to +20V (5V over the power supply) are no problem – the converter operates normally.

Calibration consists of adjusting the converter's most negative output to its ideal value (offset adjustment), then, adjusting the most positive output to its ideal value (gain adjustment). To understand the procedure, note that in principle, one is setting the output with respect to the midpoint of an increment of analog input, as denoted by two adjacent code changes. Nominal value of an increment is one

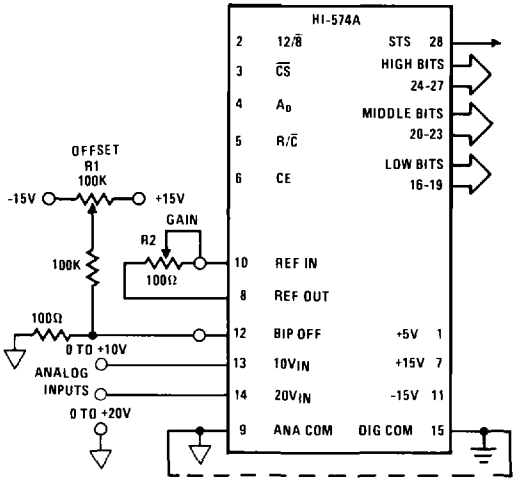


FIGURE 2. UNIPOLAR CONNECTIONS

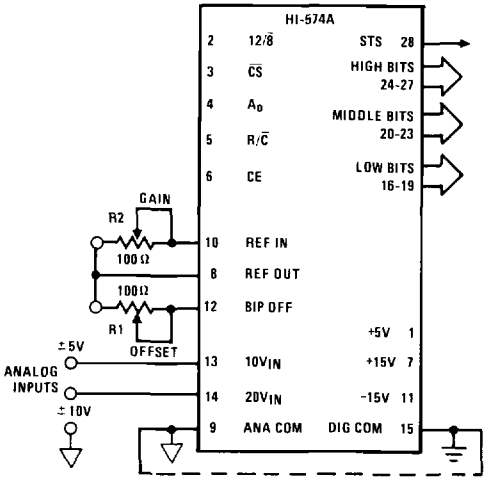


FIGURE 3 BIPOLAR INPUT CONNECTIONS

LSB. However, this approach is impractical because nothing "happens" at a midpoint to indicate that an adjustment is complete. Therefore, calibration is performed in terms of the observable code changes instead of the midpoint between code changes.

For example, midpoint of the first LSB increment should be positioned at the origin, with an output code of all 0's. To do this, apply an input of +1/2 LSB (+1.22mV for the 10V range; +2.44mV for the 20V range). Adjust the Offset potentiometer R1 until the first code transition flickers between 0000 0000 0000 and 0000 0000 0001.

Next, perform a Gain Adjust at positive full scale. Again, the ideal input corresponding to the last code change is applied. This is 1-1/2 LSB's below the nominal full scale (+9.9963V for 10V range; +19.9927V for 20V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

Bipolar Connections and Calibration –

Refer to Figure 3. The gain and offset errors listed under Specifications may be adjusted to zero using potentiometers R1 and R2*. If this isn't required, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

Connect the Analog signal to pin 13 for a ±5V range, or to pin 14 for a ±10V range. Calibration of offset and gain is similar to that for the unipolar ranges as discussed above. First apply a DC input voltage 1/2 LSB above negative full scale (i.e., −4.9988V for the ±5V range, or −9.9976V for the ±10V range). Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1-1/2 LSB's below positive full scale (+4.9963V for ±5V range; +9.9927V for ±10V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

* The 100Ω potentiometer R2 provides Gain Adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (LSB equals 2.5mV) or 20.48V (LSB equals 5.0mV) is more convenient. For these, replace R2 by a 50Ω, 1% metal film resistor. Then, to provide Gain Adjust for the 10.24V range, add a 200Ω potentiometer in series with pin 13. For the 20.48V range, add a 500Ω potentiometer in series with pin 14.

CONTROLLING THE HI-574A

The HI-574A includes logic for direct interface to most microprocessor systems. The processor may take full control of each conversion, or the converter may operate in the "stand-alone" mode, controlled only by the R/C̄ input. Full control consists of selecting an 8 or 12 bit conversion cycle, initiating the conversion, and reading the output data when ready – choosing either 12 bits at once or 8 followed by 4, in a left-justified format. The five control inputs are all TTL/CMOS-compatible: (12/8̄, CS̄, A0, R/C̄ and CE). Table 1 illustrates the use of these inputs in controlling the converter's operations. Also, a simplified schematic of the internal control logic is shown in Figure 4.

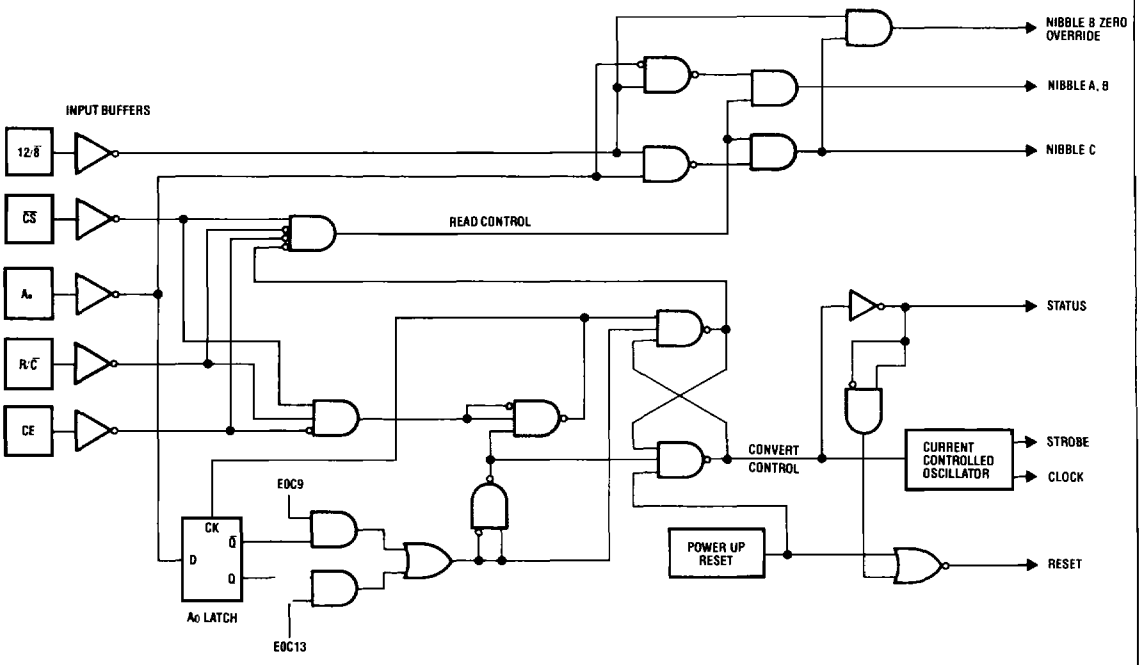


FIGURE 4. HI-574A CONTROL LOGIC

"Stand-Alone Operation"

The simplest control interface calls for a single control line connected to R/$\overline{C}$. Also, CE and 12/$\overline{8}$ are wired high, $\overline{CS}$ and A_0 are wired low, and the output data appears in words of 12 bits each.

The R/$\overline{C}$ signal may have any duty cycle within (and including) the extremes shown in Figures 5 and 6. In general, data may be read when R/$\overline{C}$ is high unless STS is also high, indicating a conversion is in progress. Timing parameters particular to this mode of operation are listed below under "Stand-Alone Mode Timing."

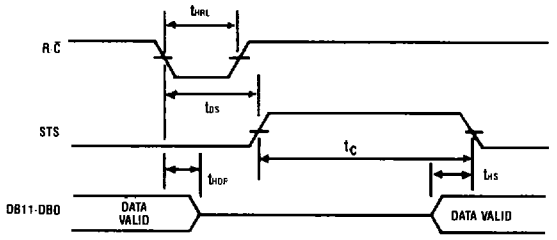


FIGURE 5. LOW PULSE FOR R/$\overline{C}$ – OUTPUTS ENABLED AFTER CONVERSION

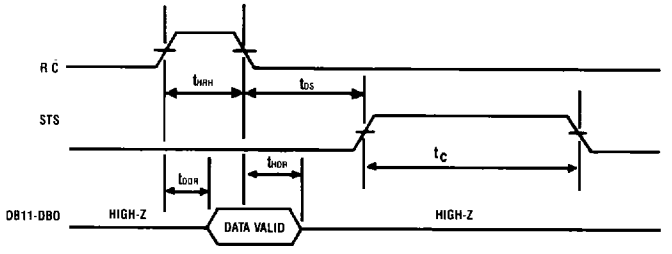


FIGURE 6. HIGH PULSE FOR R/$\overline{C}$–OUTPUTS ENABLED WHILE R/C HIGH, OTHERWISE HIGH-Z

STAND-ALONE MODE TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
tHRL	Low R/C Pulse Width	50	–	–	ns
tDS	STS Delay From R/C	–	–	200	ns
tHDR	Data Valid After R/C Low	25	–	–	ns
tHS	STS Delay After Data Valid	300	–	1200	ns
tHRH	High R/C Pulse Width	150	–	–	ns
tDDR	Data Access Time	–	–	150	ns

Time is measured from 50% level of digital transitions. Tested with a 50pF and 3kΩ load.

Conversion Length

A Convert Start transition (see Table 1) latches the state of A_0, which determines whether the conversion continues for 12 bits (A_0 low) or stops with 8 bits (A_0 high). If all 12 bits are read following an 8 bit conversion, the three LSB's will read zero and DB3 will read ONE. A_0 is latched because it is also involved in enabling the output buffers (see "Reading the Output Data"). No other control inputs are latched.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

TABLE 1

Truth Table for HI-574A Control Inputs.

Conversion Start

A conversion may be initiated as shown in Table 1 by a logic transition on any of three inputs: CE, $\overline{CS}$ or R/$\overline{C}$. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same, and if necessary, all three may change state simultaneously. To assure that a particular input controls the start of conversion, the other two should be set up at least 50nS earlier, however. See the HI-574A Timing Specifications, Convert mode.

This variety of HI-574A control modes allows a simple interface in most system applications. The Convert Start timing relationships are illustrated in Figure 7.

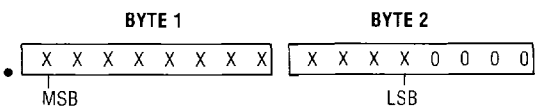
The output signal STS indicates status of the converter by going high only while a conversion is in progress. While STS is high, the output buffers remain in a high impedance state and data cannot be read. Also, an additional Start Convert will not reset the converter or reinitiate a conversion while STS is high. (However, if A_0 changes state after a conversion begins, an additional Start Convert signal will latch the new state of A_0, possibly causing a wrong cycle length (8 vs 12 bits) for that conversion).

Reading the Output Data

The output data buffers remain in a high impedance state until four conditions are met: R $\overline{C}$ high, STS low, CE high and $\overline{CS}$ low. At that time, data lines become active according to the state of inputs 12 $\overline{8}$ and A_0. Timing constraints are illustrated in Figure 8.

The 12/$\overline{8}$ input will be tied high or low in most applications, though it is fully TTL/CMOS-compatible. With 12/$\overline{8}$ high, all 12 output lines become active simultaneously, for interface to a 12 or 16 bit data bus. The A_0 input is ignored.

With 12/$\overline{8}$ low, the output is organized in two 8 bit bytes, selected one at a time by A_0. This allows an 8 bit data bus to be connected as shown in Figure 9. A_0 is usually tied to the least significant bit of the address bus, for storing the HI-574A output in two consecutive memory locations. (With A_0 low, the 8 MSB's only are enabled. With A_0 high, 4 MSB's are disabled, bits 4 through 7 are forced to zero, and the 4 LSB's are enabled). This two byte format is considered "left justified data", for which a decimal (or binary!) point is assumed to the left of byte 1:



Further, A_0 may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in Figure 9 will never be enabled at the same time.

A read operation usually begins after the conversion is complete and STS is low. For earliest access to the data however, the read should begin no later than (t_{DD} + t_{HS}) before STS goes low. See Figure 8.

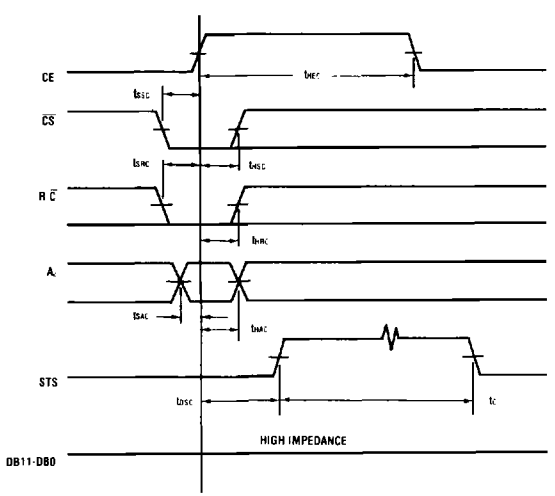


FIGURE 7. CONVERT START TIMING

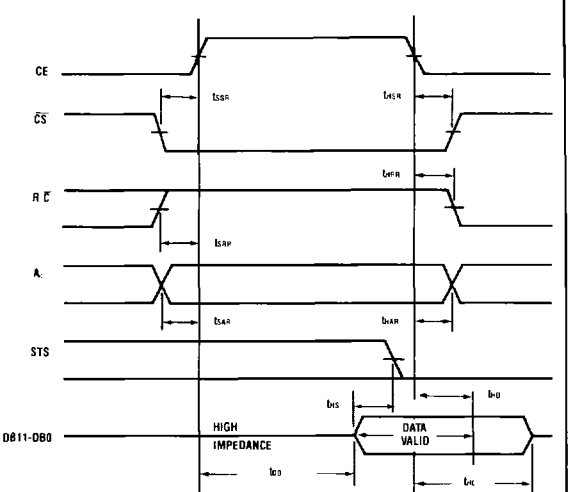


FIGURE 8. READ CYCLE TIMING

Timing Specifications +25°C Unless Otherwise Specified

Symbol	Parameter	Min	Typ	Max	Units
Convert Mode					
t_{DSC}	STS Delay from CE			200	nS
t_{HEC}	CE Pulse width	50			nS
t_{SSC}	$\overline{CS}$ to CE Setup	50			nS
t_{HSC}	$\overline{CS}$ Low during CE High	50			nS
t_{SRC}	R/$\overline{C}$ to CE Setup	50			nS
t_{HRC}	R/$\overline{C}$ Low during CE high	50			nS
t_{SAC}	A_0 to CE Setup	0			nS
t_{HAC}	A_0 Valid during CE high	50			nS
t_c	Conversion time. 12 bit cycle T min to T max	15	20	25	μS
	8 bit cycle T min to T max	10	13	17	μS
Read Mode					
t_{DD}	Access time from CE		75	150	nS
t_{HD}	Data Valid after CE low	25			nS
t_{HL}	Output float delay		100	150	nS
t_{SSR}	$\overline{CS}$ to CE setup	50			nS
t_{SRR}	R/$\overline{C}$ to CE setup	0			nS
t_{SAR}	A_0 to CE setup	50			nS
t_{HSR}	$\overline{CS}$ valid after CE low	0			nS
t_{HRR}	R/$\overline{C}$ high after CE low	0			nS
t_{HAR}	A_0 valid after CE low	50			nS
t_{HS}	STS delay after data valid	300		1200	nS

NOTE: Time is measured from 50% level of digital transitions. Tested with a 50pF and 3kΩ load.

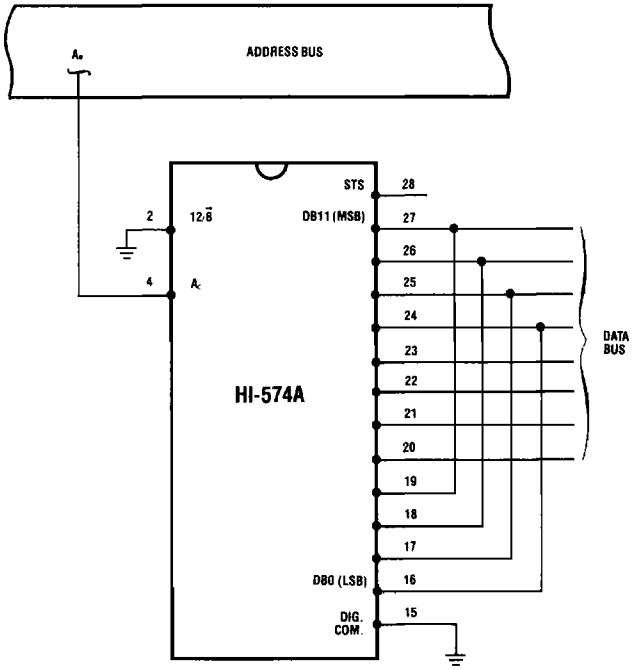


FIGURE 9 INTERFACE TO AN 8 BIT DATA BUS

DIE CHARACTERISTICS

Transistor Count		1117	Thermal Constants;	θja	48°C/W
Die Size:	Analog	204 x 104 mils		θjc	15°C/W
	Digital	158 x 84 mils	Process:		Bipolar – DI and CMOS – JI