

ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H174 Dual 4-to-1 Multiplexer

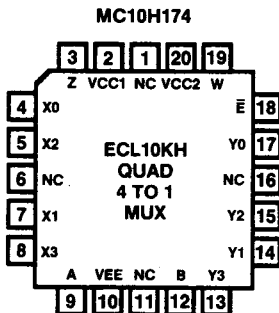
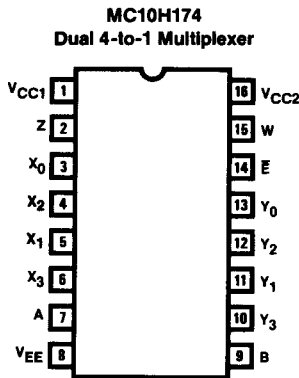
Features/Benefits

- Propagation delay 1.5 ns typical
- Power dissipation, 305 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Description

The MC10H174 is a Dual 4-to-1 Multiplexer. This device is a member of Monolithic Memories' new ECL family. This device is a functional/pinout duplication of the standard ECL 10K part with 100% improvement in propagation delay, and no increase in power-supply current.

Pin Configuration

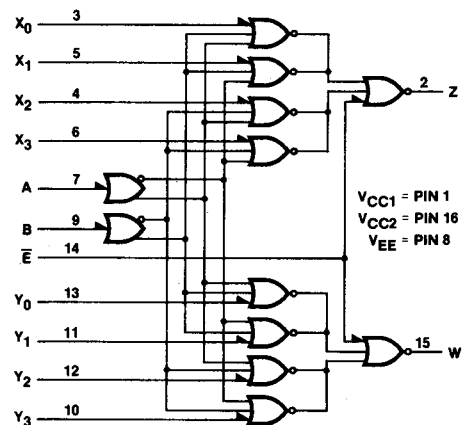


Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H174	J,N,NL(20)	Com

Logic Diagram

MC10H174



Function Table

ENABLE	ADDRESS	INPUTS	OUTPUTS	
E-bar	B	A	Z	W
H	X	X	L	L
L	L	L	X ₀	Y ₀
L	L	H	X ₁	Y ₁
L	H	L	X ₂	Y ₂
L	H	H	X ₃	Y ₃

X = Don't care.

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Absolute Maximum Ratings

Supply voltage V_{EE} ($V_{CC} = 0$)	-8.0 V to 0 Vdc
Input voltage V_I ($V_{CC} = 0$)	0 Vdc to V_{EE}
Output Current:	
Continuous	50 mA
Surge	100 mA

Operating Conditions

SYMBOL	PARAMETER	COMMERCIAL			UNIT
		MIN	TYP	MAX	
V_{EE}	Supply voltage	-5.46	-5.2	-4.94	V
T_A	Operating temperature range	0		75	°C
T_{STG}	Storage temperature range	Plastic		150	°C
		Ceramic		165	

Electrical Characteristics $V_{EE} = -5.2 V \pm 5%$ (See Note)

SYMBOL	PARAMETER	0°		25°		75°		UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX		
I_E	Power supply current	—	80	—	73	—	80	mA	
I_{inH}	Input current HIGH	Pins 3 - 7 and 9 - 13	—	475	—	300	—	300	μA
		Pin 14	—	670	—	420	—	420	
I_{inL}	Input current LOW	0.5	—	0.5	—	0.3	—	μA	
V_{OH}	HIGH output voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc	
V_{OL}	LOW output voltage	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc	
V_{IH}	HIGH input voltage	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc	
V_{IL}	LOW input voltage	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc	

Switching Characteristics $V_{EE} = -5.2 V, \pm 5%$ (See Note)

SYMBOL	PARAMETER	0°		25°		75°		UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{pd}	Propagation delay	Data (All others)	0.7	2.4	0.8	2.3	0.9	2.6	ns
		Select (A,B) Pin 7, 9	1.0	2.8	1.1	2.9	1.2	3.2	
		Enable Pin 14	0.4	1.45	0.4	1.50	0.5	1.70	
t_r, t^+	Rise time	0.5	1.5	0.5	1.6	0.5	1.70	ns	
t_f, t^-	Fall time	0.5	1.5	0.5	1.6	0.5	1.70	ns	

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.