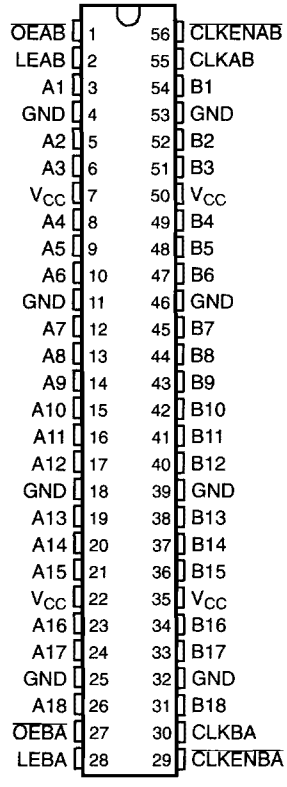
- **Member of the Texas Instruments *Widebus*™ Family**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident Wave Switching for Line Impedances of 50 Ω or Greater**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages**

DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

This 18-bit universal bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16601 combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. Output enable $\overline{OEAB}$ is active low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CLKENBA}$.

The SN74ALVC16601 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16601 is characterized for operation from −40°C to 85°C.

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FUNCTION TABLE†

INPUTS					OUTPUT
$\overline{CLKENAB}$	$\overline{OEAB}$	LEAB	CLKAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B_0‡
H	L	L	X	X	B_0‡
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B_0‡
L	L	L	H	X	B_0§

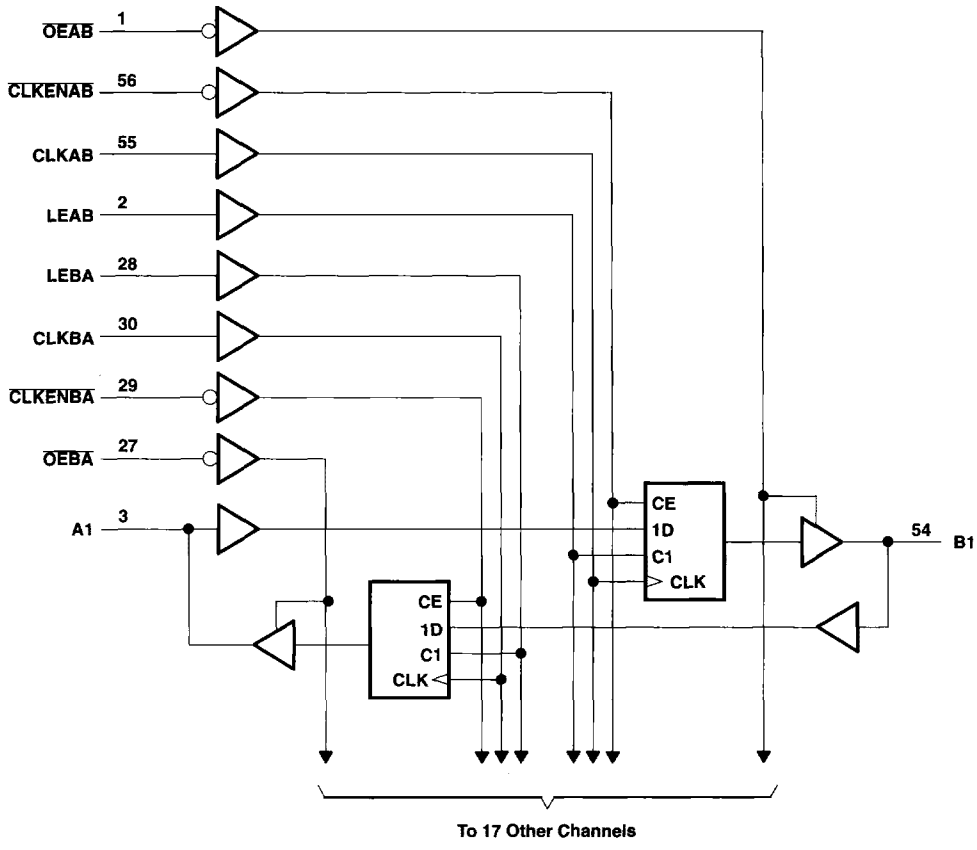
† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CLKENBA}$.

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

PRODUCT PREVIEW

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... −50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 0.7 W
DL package ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24†	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24†	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.
† Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}‡	MIN	TYP	MAX	UNIT
V_{IK}		I_I = −18 mA		2.7 V			−1.2	V
V_{OH}		I_{OH} = −100 µA		MIN to MAX	V_{CC}−0.2			V
		I_{OH} = −12 mA		2.7 V	2.2			
				3 V	2.4			
		I_{OH} = −24 mA		3 V	2			
V_{OL}		I_{OL} = 100 µA		MIN to MAX			0.2	V
		I_{OL} = 12 mA		2.7 V			0.4	
		I_{OL} = 24 mA		3 V			0.55	
I_I		V_I = V_{CC} or GND		3.6 V			±5	µA
I_{OZ}§		V_O = V_{CC} or GND		3.6 V			±10	µA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V			20	µA
ΔI_{CC}		V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				500	µA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		TBD		pF
C_{io}	A or B ports	V_O = V_{CC} or GND		3.3 V		TBD		pF

‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

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