Standard Products

# UT9Q512 512K x 8 SRAM

Advanced Data Sheet

March 12, 2001

## FEATURES

- 25ns maximum (5 volt supply) address access time
- Asynchronous operation for compatibility with industry-standard 512K x 8 SRAMs
- TTL compatible inputs and output levels, three-state bidirectional data bus
- Typical radiation performance
  - Total dose
    - Solution #1: Up to 30krads
    - Solution #2: Up to 300krads
  - SEL Immune >100 MeV-cm$^2$/mg
  - $LET_{TH}$(0.25) = 40 MeV-cm$^2$/mg
  - Saturated Cross Section (cm$^2$) per bit, 1.0E-9
    - 3.8E-11 errors/bit-day, Adams to 90% geosynchronous heavy ion
  - Inherent Neutron Hardness: 1.0E14n/cm$^2$
  - Nominal Dose Rate
    - Upset 1.0E9 rad(Si)/sec
    - Latchup >1.0E11 rad(Si)/sec
- Packaging options:
  - 36-lead ceramic flatpack
  - 36-lead flatpack shielded
- Standard Microcircuit Drawing 5962-00536
  - QML T and Q compliant part

## INTRODUCTION

The UT9Q512 is a high-performance CMOS static RAM organized as 524,288 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{E}$), an active LOW Output Enable ($\overline{G}$), and three-state drivers. This device has a power-down feature that reduces power consumption by more than 90% when deselected.

Writing to the device is accomplished by taking Chip Enable one ($\overline{E}$) input LOW and Write Enable ($\overline{W}$) inputs LOW. Data on the eight I/O pins ($DQ_0$ through $DQ_7$) is then written into the location specified on the address pins ($A_0$ through $A_{18}$). Reading from the device is accomplished by taking Chip Enable one ($\overline{E}$) and Output Enable ($\overline{G}$) LOW while forcing Write Enable ($\overline{W}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins ($DQ_0$ through $DQ_7$) are placed in a high impedance state when the device is deselected ($\overline{E}$ HIGH), the outputs are disabled ($\overline{G}$ HIGH), or during a write operation ($\overline{E}$ LOWand $\overline{W}$ LOW).

Aeroflex UTMC offers this device for operation in systems requiring the full Mil-TEMP range, as well as an extended industrial temperature range (-40$^o$C to +125$^o$C).

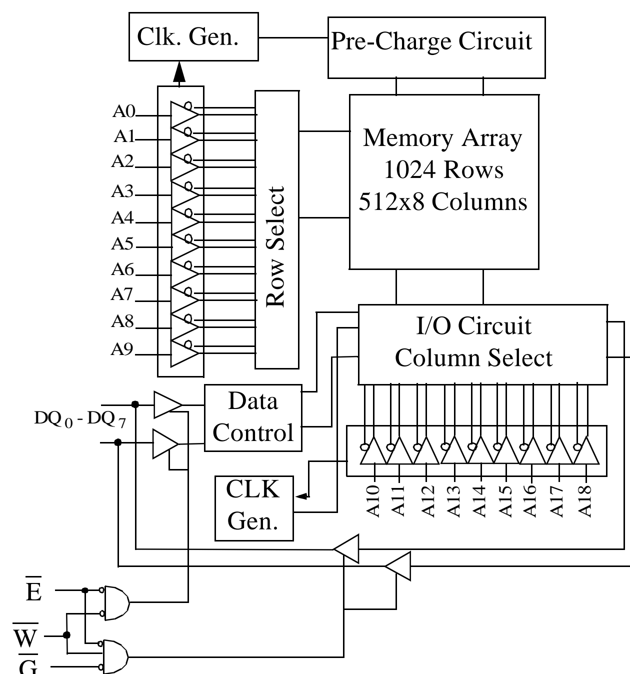



Figure 1. UT9Q512 SRAM Block Diagram

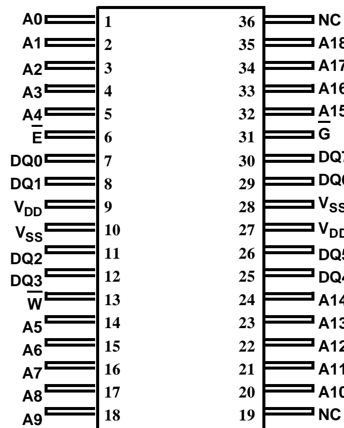



**Figure 2. UT9Q512 25ns SRAM Pinout (36)**
**(For both shielded and unshielded packages)**

**PIN NAMES**

| | |
|---|---|
| A(18:0) | Address |
| DQ(7:0) | Data Input/Output |
| $\overline{E}$ | Enable |
| $\overline{W}$ | Write Enable |
| $\overline{G}$ | Output Enable |
| $V_{DD}$ | Power |
| $V_{SS}$ | Ground |

## DEVICE OPERATION

The UT9Q512 has three control inputs called Enable 1 ($\overline{E}$), Write Enable ($\overline{W}$), and Output Enable ($\overline{G}$); 19 address inputs, A(18:0); and eight bidirectional data lines, DQ(7:0). $\overline{E}$ Device Enable controls device selection, active, and standby modes. Asserting $\overline{E}$ enables the device, causes $I_{DD}$ to rise to its active value, and decodes the 19 address inputs to select one of 524,288 words in the memory. $\overline{W}$ controls read and write operations. During a read cycle, $\overline{G}$ must be asserted to enable the outputs.

**Table 1. Device Operation Truth Table**

| $\overline{G}$ | $\overline{W}$ | $\overline{E}$ | I/O Mode | Mode |
|---|---|---|---|---|
| X[1] | X | 1 | 3-state | Standby |
| X | 0 | 0 | Data in | Write |
| 1 | 1 | 0 | 3-state | Read[2] |
| 0 | 1 | 0 | Data out | Read |

**Notes:**
1. "X" is defined as a "don't care" condition.
2. Device active; outputs disabled.

## READ CYCLE

A combination of $\overline{W}$ greater than $V_{IH}$ (min) and $\overline{E}$ less than $V_{IL}$ (max) defines a read cycle. Read access time is measured from the latter of Device Enable, Output Enable, or valid address to valid data output.

SRAM Read Cycle 1, the Address Access in figure 3a, is initiated by a change in address inputs while the chip is enabled with $\overline{G}$ asserted and $\overline{W}$ deasserted. Valid data appears on data outputs DQ(7:0) after the specified $t_{AVQV}$ is satisfied. Outputs remain active throughout the entire cycle. As long as Device Enable and Output Enable are active, the address inputs may change at a rate equal to the minimum read cycle time ($t_{AVAV}$).

SRAM read Cycle 2, the Chip Enable - Controlled Access in figure 3b, is initiated by $\overline{E}$ going active while $\overline{G}$ remains asserted, $\overline{W}$ remains deasserted, and the addresses remain stable for the entire cycle. After the specified $t_{ETQV}$ is satisfied, the eight-bit word addressed by A(18:0) is accessed and appears at the data outputs DQ(7:0).

SRAM read Cycle 3, the Output Enable - Controlled Access in figure 3c, is initiated by $\overline{G}$ going active while $\overline{E}$ is asserted, $\overline{W}$ is deasserted, and the addresses are stable. Read access time is $t_{GLQV}$ unless $t_{AVQV}$ or $t_{ETQV}$ have not been satisfied.

## WRITE CYCLE

A combination of $\overline{W}$ less than $V_{IL}$(max) and $\overline{E}$ less than $V_{IL}$(max) defines a write cycle. The state of $\overline{G}$ is a "don't care" for a write cycle. The outputs are placed in the high-impedance state when either $\overline{G}$ is greater than $V_{IH}$(min), or when $\overline{W}$ is less than $V_{IL}$(max).

Write Cycle 1, the Write Enable - Controlled Access in figure 4a, is defined by a write terminated by $\overline{W}$ going high, with $\overline{E}$ still active. The write pulse width is defined by $t_{WLWH}$ when the write is initiated by $\overline{W}$, and by $t_{ETWH}$ when the write is initiated by $\overline{E}$. Unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait $t_{WLQZ}$ before applying data to the nine bidirectional pins DQ(7:0) to avoid bus contention.

Write Cycle 2, the Chip Enable - Controlled Access in figure 4b, is defined by a write terminated by $\overline{E}$ going inactive. The write pulse width is defined by $t_{WLEF}$ when the write is initiated by $\overline{W}$, and by $t_{ETEF}$ when the write is initiated by the $\overline{E}$ going active. For the $\overline{W}$ initiated write, unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait $t_{WLQZ}$ before applying data to the eight bidirectional pins DQ(7:0) to avoid bus contention.

## TYPICAL RADIATION HARDNESS

**Table 2. Radiation Hardness Design Specifications[1]**

| | | |
|---|---|---|
| **Total Dose** | 30 | krad(Si) |
| **Heavy Ion Error Rate[2]** | 3.8E-11 | Errors/Bit-Day |

**Notes:**
1. The SRAM will not latchup during radiation exposure under recommended operating conditions.
2. 10% worst case particle environment, Geosynchronous orbit, 0.025 mils of Aluminum.

## ABSOLUTE MAXIMUM RATINGS[1]

(Referenced to $V_{SS}$)

| SYMBOL | PARAMETER | LIMITS |
| --- | --- | --- |
| $V_{DD}$ | DC supply voltage | -0.5 to 7.0V |
| $V_{I/O}$ | Voltage on any pin | -0.5 to 7.0V |
| $T_{STG}$ | Storage temperature | -65 to +150°C |
| $P_D$ | Maximum power dissipation | 1.0W |
| $T_J$ | Maximum junction temperature[2] | +150°C |
| $\Theta_{JC}$ | Thermal resistance, junction-to-case[3] | 10°C/W |
| $I_I$ | DC input current | ±10 mA |

**Notes:**
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Maximum junction temperature may be increased to +175°C during burn-in and steady-static life.
3. Test per MIL-STD-883, Method 1012.

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS |
| --- | --- | --- |
| $V_{DD}$ | Positive supply voltage | 4.5 to 5.5V |
| $T_C$ | Case temperature range | (C) screening: -55° to +125°C<br>(E) screening: -40° to +125°C |
| $V_{IN}$ | DC input voltage | 0V to $V_{DD}$ |

**DC ELECTRICAL CHARACTERISTICS (Pre/Post-Radiation)***

(-55°C to +125°C for (C) screening and -40°C to +125°C for (E) screening) ($V_{DD}$ = 5.0V ± 10%)

| SYMBOL | PARAMETER | CONDITION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 2.0 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $V_{OL1}$ | Low-level output voltage | $I_{OL}$ = 8mA, $V_{DD}$ =4.5V | | 0.4 | V |
| $V_{OL2}$ | Low-level output voltage | $I_{OL}$ = 200µA,$V_{DD}$ =4.5V | | 0.05 | V |
| $V_{OH1}$ | High-level output voltage | $I_{OH}$ = -4mA,$V_{DD}$ =4.5V | 2.4 | | V |
| $V_{OH2}$ | High-level output voltage | $I_{OH}$ = -200µA,$V_{DD}$ =4.5V | 3.2 | | V |
| $C_{IN}$[1] | Input capacitance | *f* = 1MHz @ 0V | | 10 | pF |
| $C_{IO}$[1] | Bidirectional I/O capacitance | *f* = 1MHz @ 0V | | 12 | pF |
| $I_{IN}$ | Input leakage current | $V_{IN}$ = $V_{DD}$ and $V_{SS}$, $V_{DD}$ = $V_{DD}$ (max) | -2 | 2 | µA |
| $I_{OZ}$ | Three-state output leakage current | $V_O$ = $V_{DD}$ and $V_{SS}$<br>$V_{DD}$ = $V_{DD}$ (max)<br>$\overline{G}$ = $V_{DD}$ (max) | -2 | 2 | µA |
| $I_{OS}$[2, 3] | Short-circuit output current | $V_{DD}$ = $V_{DD}$ (max), $V_O$ = $V_{DD}$<br>$V_{DD}$ = $V_{DD}$ (max), $V_O$ = 0V | -90 | 90 | mA |
| $I_{DD}$(OP) | Supply current operating @ 1MHz | Inputs: $V_{IL}$ = 0.8V,<br>$V_{IH}$ = 2.0V<br>$I_{OUT}$ = 0mA<br>$V_{DD}$ = $V_{DD}$ (max) | | 125 | mA |
| $I_{DD1}$(OP) | Supply current operating @40MHz | Inputs: $V_{IL}$ = 0.8V,<br>$V_{IH}$ = 2.0V<br>$I_{OUT}$ = 0mA<br>$V_{DD}$ = $V_{DD}$ (max) | | 180 | mA |
| $I_{DD2}$(SB) | Supply current standby @0MHz | Inputs: $V_{IL}$ = $V_{SS}$<br>$I_{OUT}$ = 0mA<br>$\overline{E}$ = $V_{DD}$ - 0.5<br>$V_{DD}$ = $V_{DD}$ (max)<br>$V_{IH}$ = $V_{DD}$ - 0.5V<br>-55°C and 25°C<br>-40°C and 25°C | | 6<br>6 | mA<br>mA |
| | | 125°C | | 12 | mA |

**Notes:**

* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.

1. Measured only for initial qualification and after process or design changes that could affect input/output capacitance.
2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.

**AC CHARACTERISTICS READ CYCLE (Pre/Post-Radiation)***

(-55°C to +125°C for (C) screening and -40°C to +125°C for (E) screening) ($V_{DD}$ = 5.0V ± 10%)

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{AVAV}$ [1] | Read cycle time | 25 | | ns |
| $t_{AVQV}$ | Read access time | | 25 | ns |
| $t_{AXQX}$ | Output hold time | 3 | | ns |
| $t_{GLQX}$ | $\overline{G}$-controlled Output Enable time | 0 | | ns |
| $t_{GLQV}$ | $\overline{G}$-controlled Output Enable time (Read Cycle 3) | | 10 | ns |
| $t_{GHQZ}$ [2] | $\overline{G}$-controlled output three-state time | | 10 | ns |
| $t_{ETQX}$ [3] | $\overline{E}$-controlled Output Enable time | 3 | | ns |
| $t_{ETQV}$ [3] | $\overline{E}$-controlled access time | | 25 | ns |
| $t_{EFQZ}$ [1,2,4] | $\overline{E}$-controlled output three-state time | | 10 | ns |

**Notes:** * Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.
1. Functional test.
2. Three-state is defined as a 500mV change from steady-state output voltage (see Figure 3).
3. The ET (enable true) notation refers to the falling edge of E. SEU immunity does not affect the read parameters.
4. The EF (enable false) notation refers to the rising edge of E. SEU immunity does not affect the read parameters.

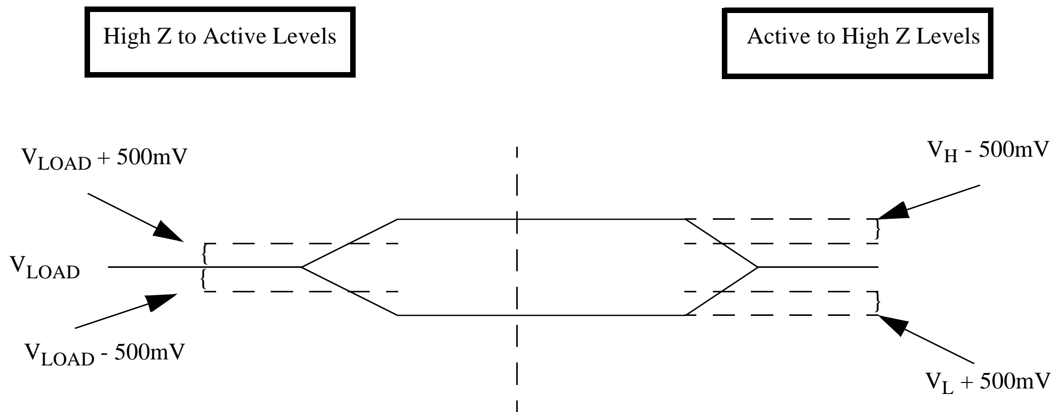
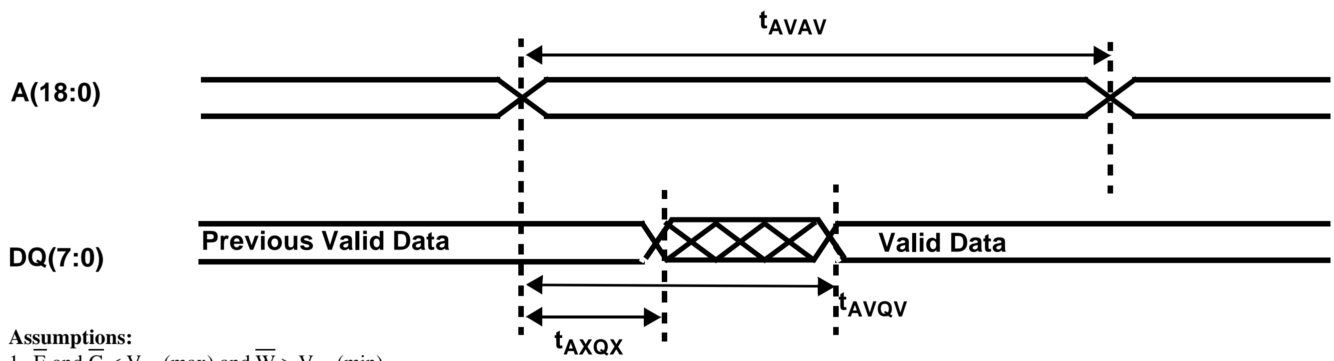
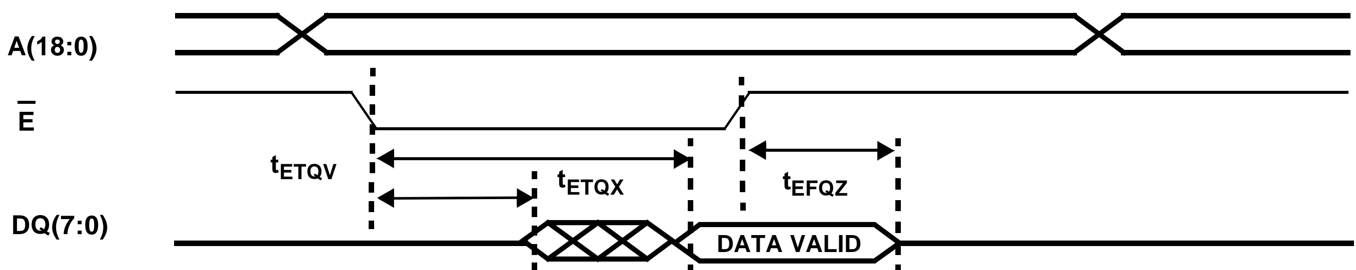



**Figure 3. 5-Volt SRAM Loading**



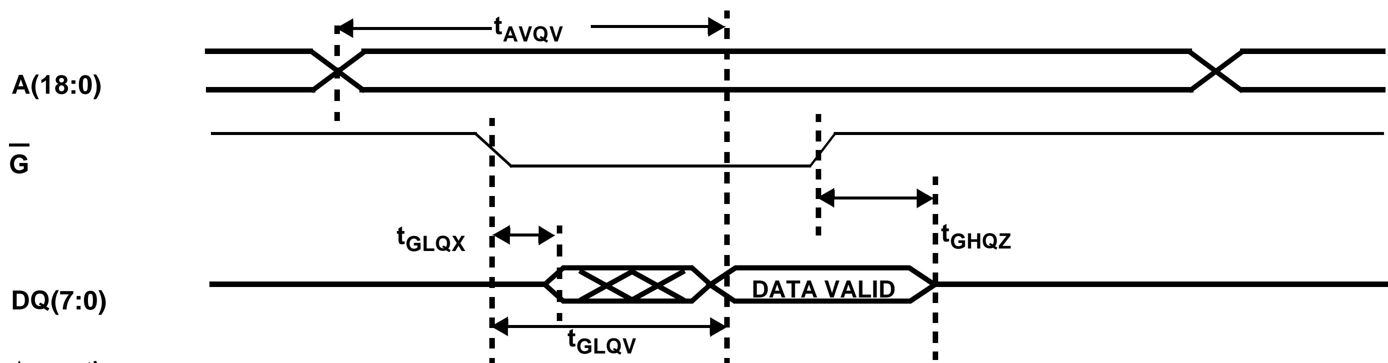

**Assumptions:**
1. $\overline{E}$ and $\overline{G} \leq V_{IL}$ (max) and $\overline{W} \geq V_{IH}$ (min)

**Figure 4a. SRAM Read Cycle 1: Address Access**




**Assumptions:**
1. $\overline{G} \leq V_{IL}$ (max) and $\overline{W} \geq V_{IH}$ (min)

**Figure 4b. SRAM Read Cycle 2: Chip Enable-Controlled Access**




**Assumptions:**
1. $\overline{E} \leq V_{IL}$ (max) and $\overline{W} \geq V_{IH}$ (min)

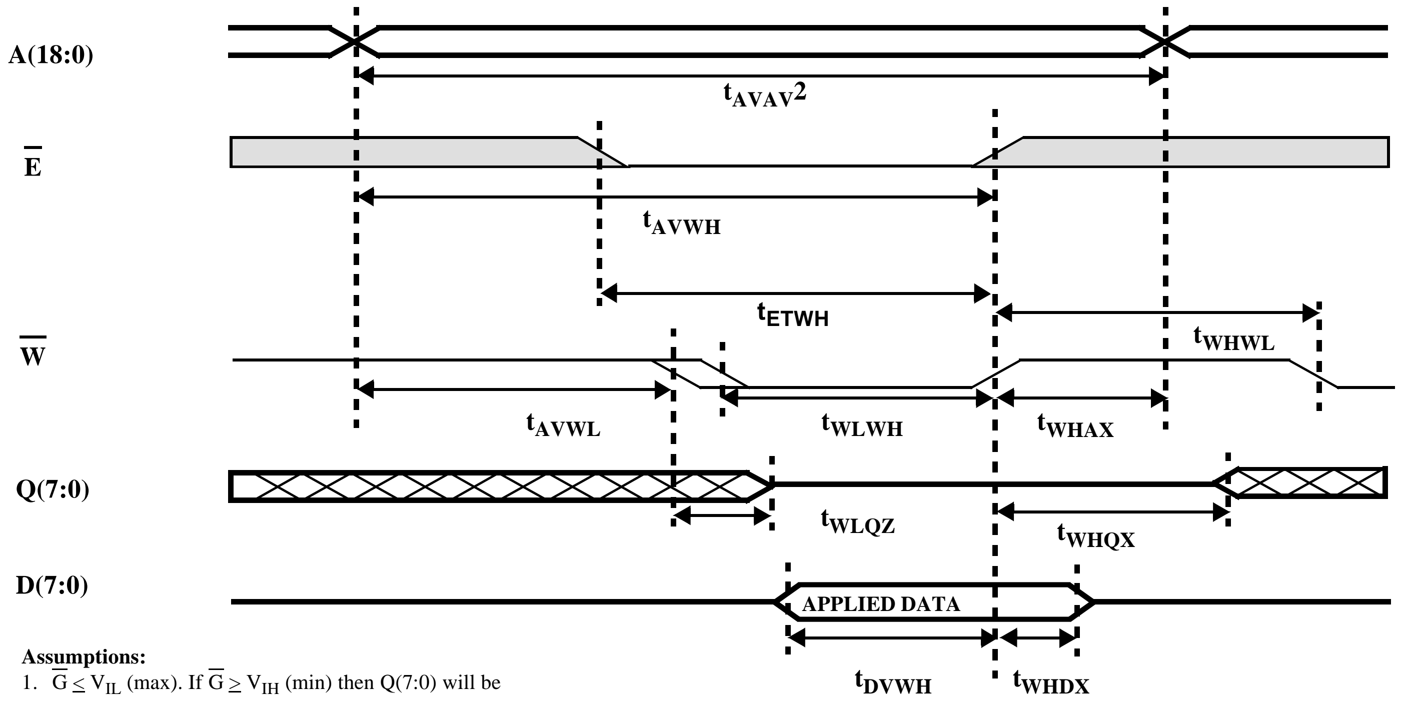
**Figure 4c. SRAM Read Cycle 3: Output Enable-Controlled Access**

**AC CHARACTERISTICS WRITE CYCLE (Pre/Post-Radiation)***

(-55°C to +125°C for (C) screening and -40°C to +125°C for (E) screening) ($V_{DD}$ = 5.0V ± 10%)

| SYMBOL | PARAMETER | 9Q512-25 5.0V MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{AVAV}$[1] | Write cycle time | 25 | | ns |
| $t_{ETWH}$ | Device Enable to end of write | 20 | | ns |
| $t_{AVET}$ | Address setup time for write ($\overline{E}$ - controlled) | 0 | | ns |
| $t_{AVWL}$ | Address setup time for write ($\overline{W}$ - controlled) | 0 | | ns |
| $t_{WLWH}$ | Write pulse width | 20 | | ns |
| $t_{WHAX}$ | Address hold time for write ($\overline{W}$ - controlled) | 0 | | ns |
| $t_{EFAX}$ | Address hold time for Device Enable ($\overline{E}$ - controlled) | 0 | | ns |
| $t_{WLQZ}$[2] | $\overline{W}$ - controlled three-state time | | 10 | ns |
| $t_{WHQX}$ | $\overline{W}$ - controlled Output Enable time | 5 | | ns |
| $t_{ETEF}$ | Device Enable pulse width ($\overline{E}$ - controlled) | 20 | | ns |
| $t_{DVWH}$ | Data setup time | 15 | | ns |
| $t_{WHDX}$ | Data hold time | 2 | | ns |
| $t_{WLEF}$ | Device Enable controlled write pulse width | 20 | | ns |
| $t_{DVEF}$ | Data setup time | 15 | | ns |
| $t_{EFDX}$ | Data hold time | 2 | | ns |
| $t_{AVWH}$ | Address valid to end of write | 20 | | ns |
| $t_{WHWL}$[1] | Write disable time | 5 | | ns |

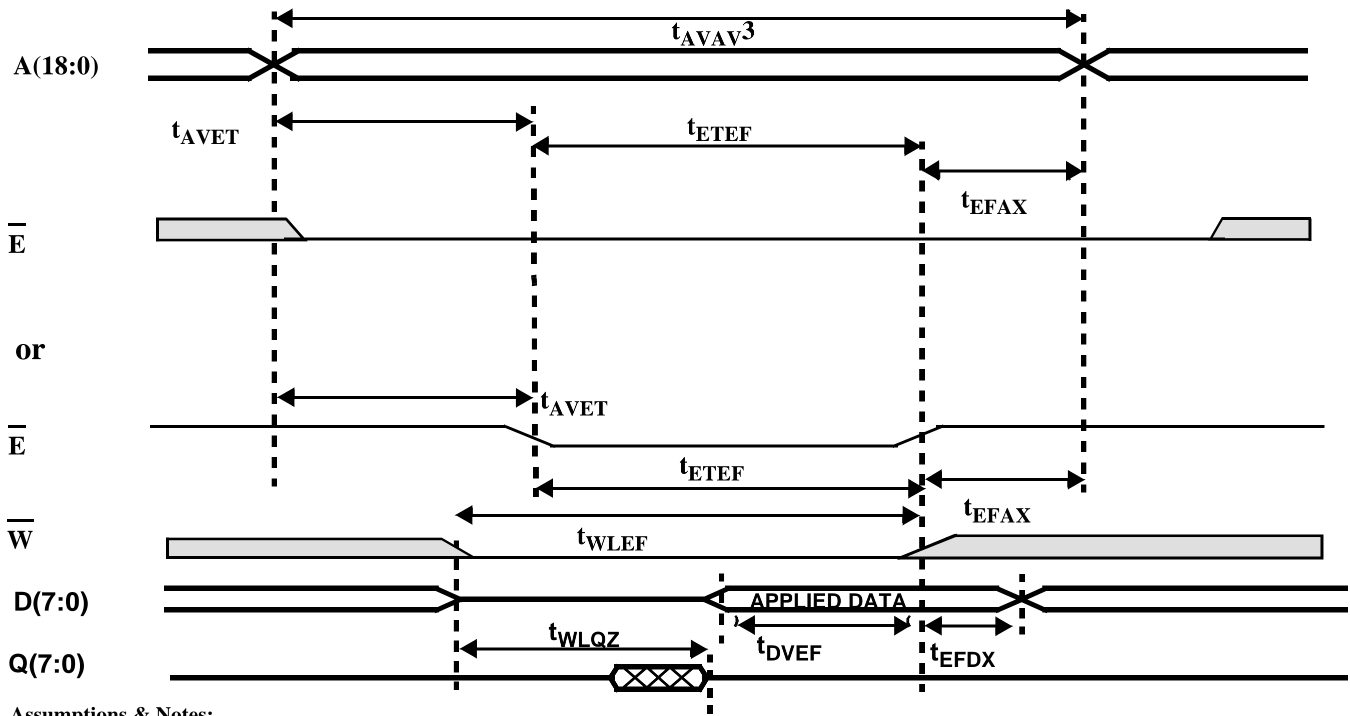
**Notes**:
* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.
1. Functional test performed with outputs disabled ($\overline{G}$ high).
2. Three-state is defined as 500mV change from steady-state output voltage (see Figure 3).




**Assumptions:**

1. $\overline{G} \leq V_{IL}$ (max). If $\overline{G} \geq V_{IH}$ (min) then Q(7:0) will be in three-state for the entire cycle.
2. $\overline{G}$ high for $t_{AVAV}$ cycle.

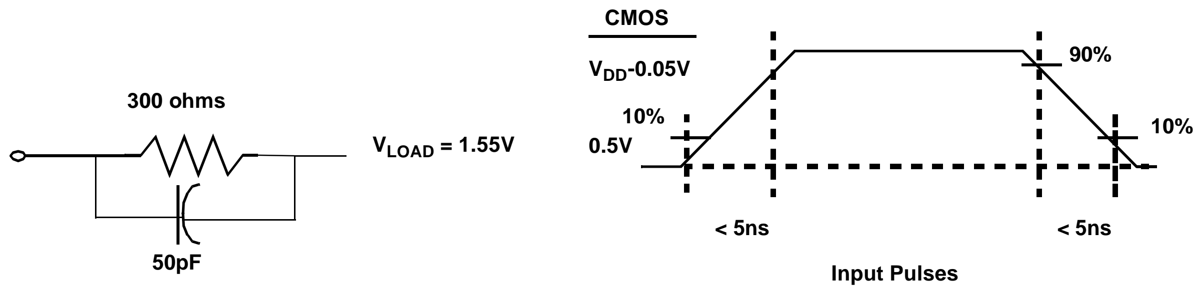
**Figure 5a. SRAM Write Cycle 1: Write Enable - Controlled Access**




**Assumptions & Notes:**

1. $\overline{G} \leq V_{IL}$ (max). If $\overline{G} \geq$ VIH (min) then Q(7:0) will be in three-state for the entire cycle.
2. Either $\overline{E}$ scenario above can occur.
3. $\overline{G}$ high for $t_{AVAV}$ cycle.

**Figure 5b. SRAM Write Cycle 2: Chip Enable - Controlled Access**




**Notes:**

1. 50pF including scope probe and test socket capacitance.
2. Measurement of data output occurs at the low to high or high to low transition mid-point (i.e., CMOS input = $V_{DD}/2$).

**Figure 6. AC Test Loads and Input Waveforms**

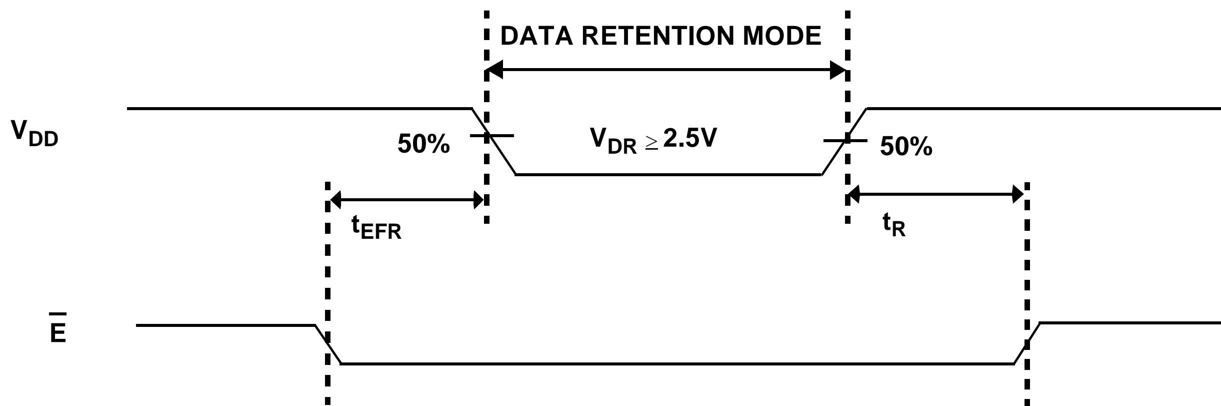



**Figure 7. Low $V_{DD}$ Data Retention Waveform**

**DATA RETENTION CHARACTERISTICS (Pre/Post-Irradiation)**
(1 Second Data Retention Test)

| SYMBOL | PARAMETER | MINIMUM | MAXIMUM | UNIT |
|---|---|---|---|---|
| $V_{DR}$ | $V_{DD}$ for data retention | 2.5 | -- | V |
| $I_{DDR}$ [1,2] | Data retention current | -- | 5.0 | mA |
| $t_{EFR}$ [1,3] | Chip select to data retention time | 0 | | ns |
| $t_R$ [1,3] | Operation recovery time | $t_{AVAV}$ | | ns |

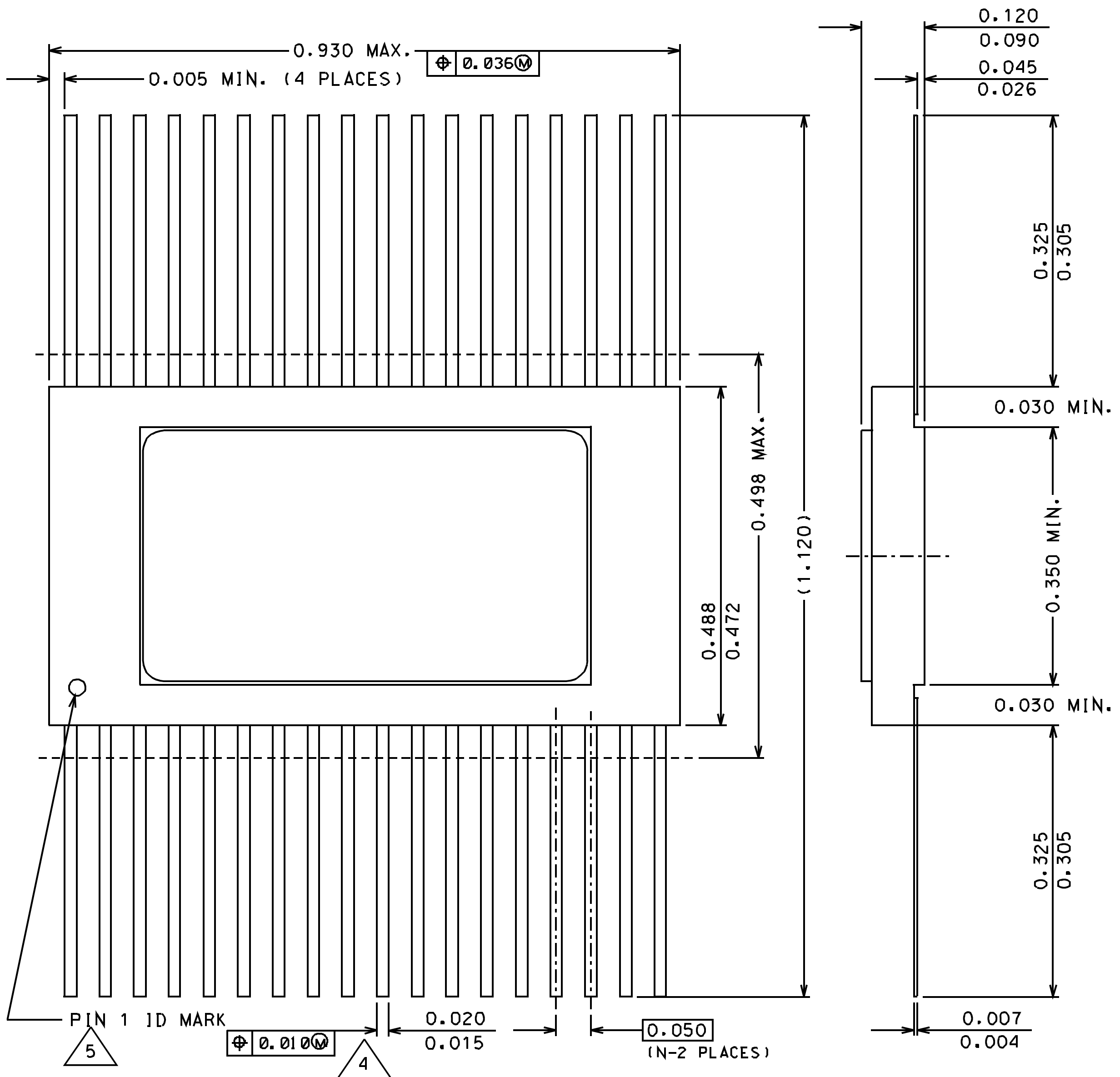
**Notes:**
1. $\overline{E} = V_{DD}$ - .2V, all other inputs = $V_{DR}$ or $V_{SS}$.
2. Data retention current ($I_{DDR}$) Tc = 25°C.
3. Not guaranteed or tested.

**DATA RETENTION CHARACTERISTICS (Pre/Post-Irradiation)**
(10 Second Data Retention Test, Tc= -55°C to 125°Cf or (C) screening and -40°C to +125°C for (E) screening)

| SYMBOL | PARAMETER | MINIMUM | MAXIMUM | UNIT |
|---|---|---|---|---|
| $V_{DD}$ [1] | $V_{DD}$ for data retention | 4.5 | 5.5 | V |
| $t_{EFR}$ [2, 3] | Chip select to data retention time | 0 | | ns |
| $t_R$ [2, 3] | Operation recovery time | $t_{AVAV}$ | | ns |

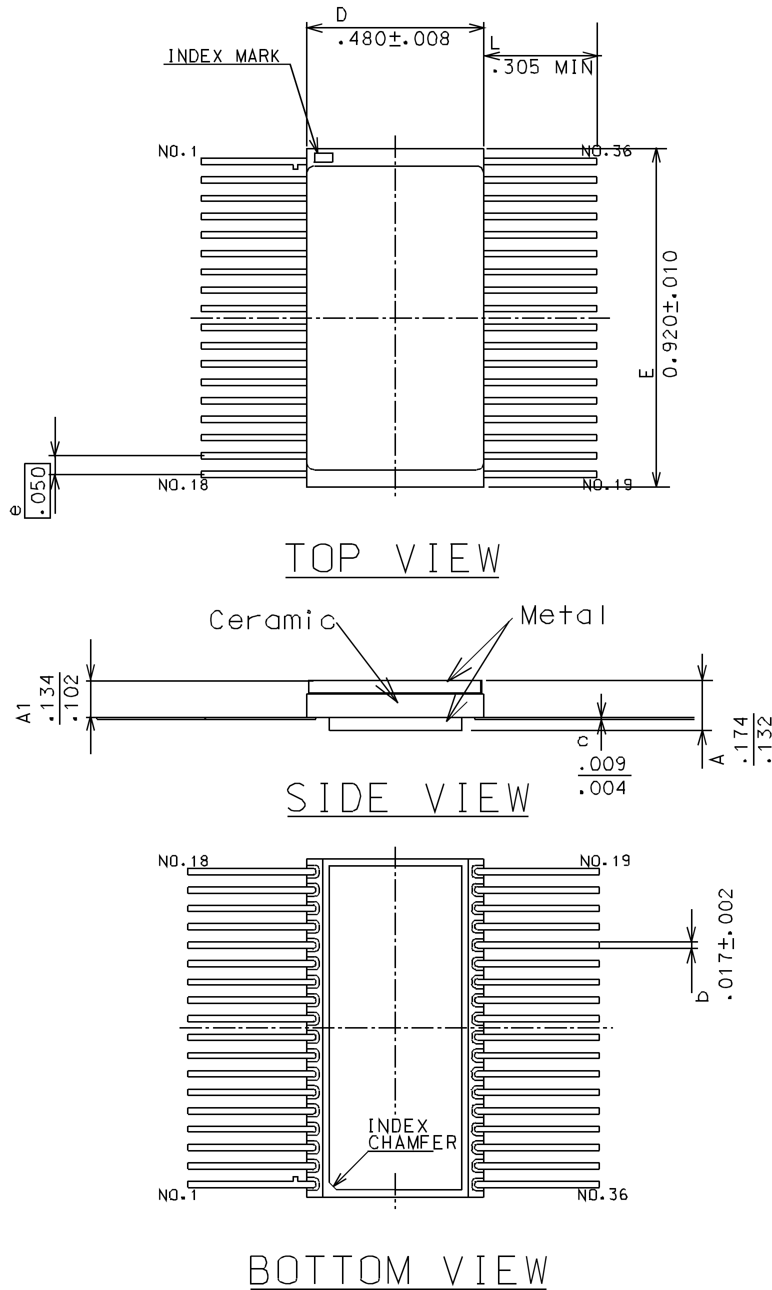
**Notes:**
1. Performed at $V_{DD}$ (min) and $V_{DD}$ (max).
2. $\overline{E} = V_{SS}$, all other inputs = $V_{DR}$ or $V_{SS}$.
3. Not guaranteed or tested.

## PACKAGING




1. All exposed metalized areas are gold plated over electroplated nickel per MIL-PRF-38535.
2. The lid is electrically connected to $V_{SS}$.
3. Lead finishes are in accordance to MIL-PRF-38535.
4. Lead position and coplanarity are not measured.
5. ID mark is vendor option.

**Figure 8. 36-pin Ceramic FLATPACK**




1. All package finishes are per MIL-PRF-38535.
2. Letter designations are for cross-reference to MIL-STD-1835.
3. All leads increase max. limit by 0.003 measured at the center of the flat, when lead finish A (solder) is applied.
4. Total weight is approx. 10.5 g.

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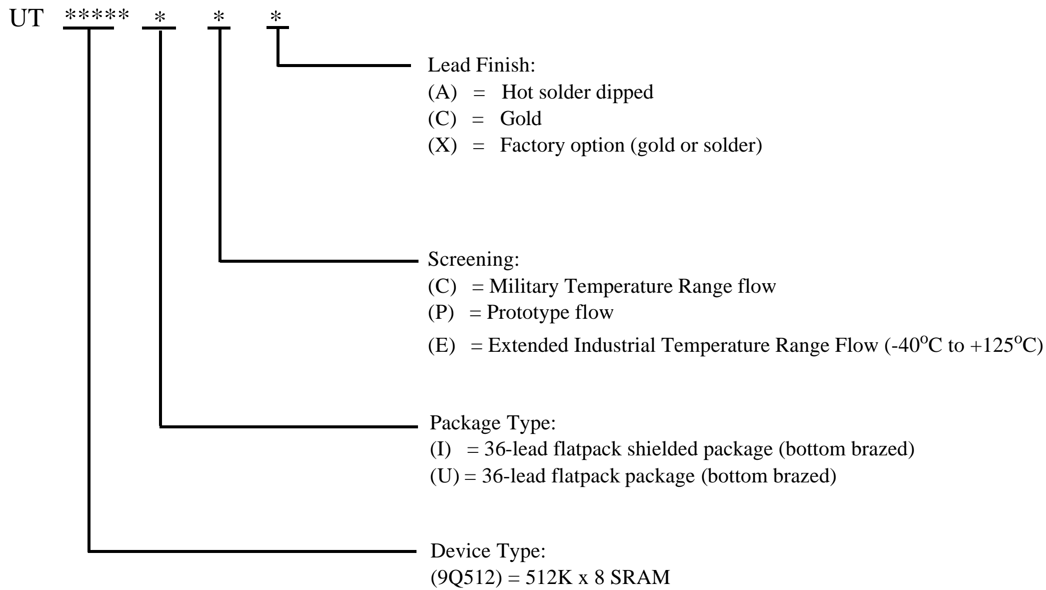
**Figure 9. 36-lead flatpack shielded package**

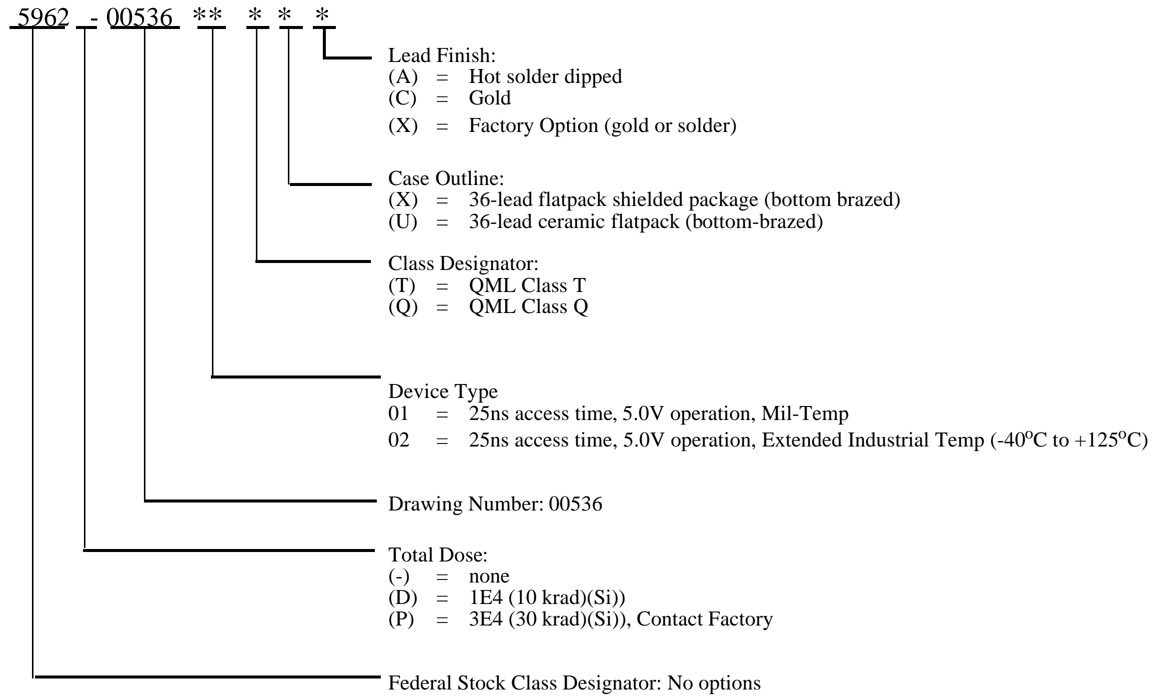
## ORDERING INFORMATION

### 512K x 8 SRAM:




**Notes:**
1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Prototype flow per UTMC Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY. Radiation neither tested nor guaranteed.
4. Military Temperature Range flow per UTMC Manufacturing Flows Document. Devices are tested at -55°C, room temp, and 125°C. Radiation neither tested nor guaranteed.
5. 36-lead flatpack shielded package bottom brazed for reduced high rel orders only.

## 512K x 8 SRAM: SMD




**Notes:**

1.Lead finish (A,C, or X) must be specified.

2.If an “X” is specified when ordering, part marking will match the lead finish and will be either “A” (solder) or “C” (gold).

3.Total dose radiation must be specified when ordering. QML Q and QML T not available without radiation hardening.