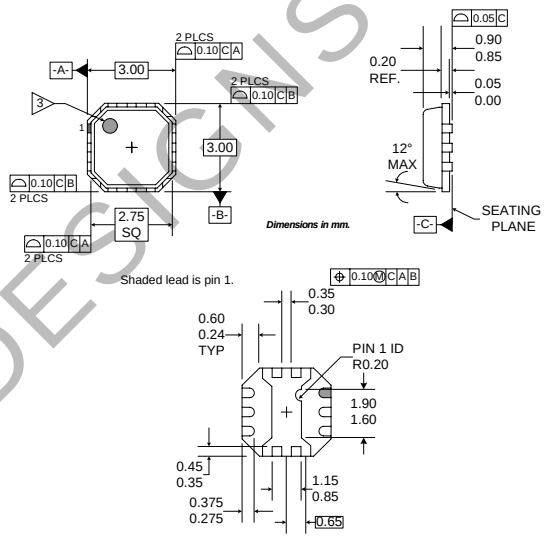
BROADBAND HIGH LINEARITY AMPLIFIER

Typical Applications

- Basestation Applications
- Cellular and PCS Systems
- WLL, W-CDMA Systems
- Final PA for Low-Power Applications

Product Description

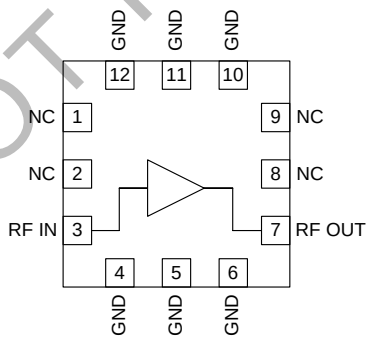
The RF3305 is a high-efficiency GaAs Heterojunction Bipolar Transistor (HBT) amplifier packaged in a low-cost surface-mount package. This amplifier is ideal for use in applications requiring high-linearity and low noise figure over the 300MHz to 3GHz frequency range. The RF3305 operates from a single 5V power supply. The 3mmx3mm footprint is compatible with standard SOT89 packages.



Package Style: QFN, 12-Pin, 3x3

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS
- ☐ InGaP/HBT
- ☐ GaN HEMT
- ☐ SiGe Bi-CMOS



Functional Block Diagram

Features

- 300MHz to 3GHz
- +40dBm Output IP3
- 12.5dB Gain at 2.0GHz
- +23dBm P1dB
- 3.0dB Typical Noise Figure at 2.0GHz
- Single 5V Power Supply

Ordering Information

RF3305	Broadband High Linearity Amplifier
RF3305 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7628 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

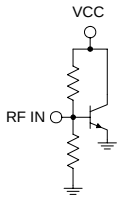
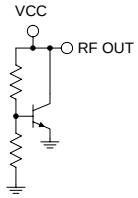
Absolute Maximum Ratings

Parameter	Rating	Unit
RF Input Power	+20	dBm
Device Voltage	-0.5 to +6.0	V
Device Current	250	mA
Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C
Junction Temperature	+225	°C

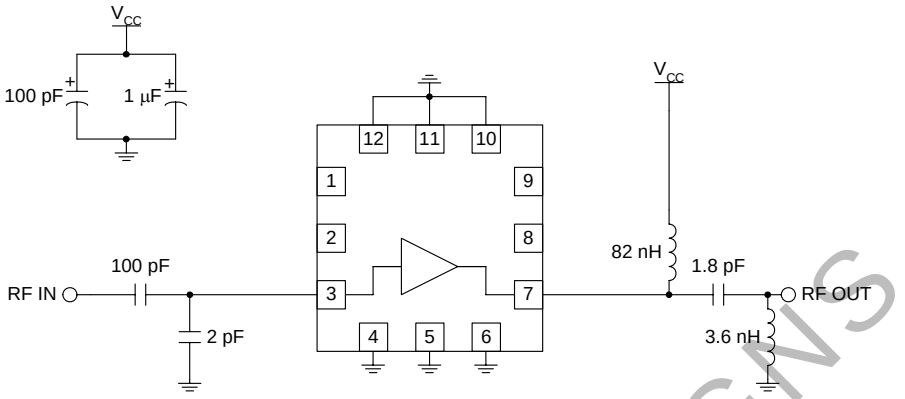
Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					
AC Specifications (2GHz)					V_{CC}=5V, RF_{IN}=-10dBm, Freq=2.0GHz, with 2GHz application schematic.
Frequency	300		3000	MHz	
Gain (Small Signal)	11.0	12.5		dB	F=2GHz
Input Return Loss		15		dB	F=2GHz
Output Return Loss		15		dB	F=2GHz
Output IP3	+36.5	+40.0		dBm	F_1= 1.99GHz, F_2=2.00GHz, P_{IN}=-5dBm
Output P1dB	+17.0	+23.0		dBm	
Noise Figure		3.0		dB	
AC Specifications (900MHz)					V_{CC}=5V, RF_{IN}=-10dBm, Freq=900MHz, with 900MHz application schematic.
Frequency	300		3000	MHz	
Gain (Small Signal)	17	18		dB	
Input Return Loss		20		dB	
Output Return Loss		20		dB	
Output IP3	38	41		dBm	F_1= 900MHz, F_2=901MHz, P_{IN}=-10dBm
Output P1dB	20	25		dBm	
Noise Figure		2.5		dB	
Thermal					I_{CC}=150mA, P_{DISS}=750mW. (See Note.)
$Theta_{JC}$		88		°C/W	
Maximum Measured Junction Temperature at DC Bias Conditions		146		°C	T_{AMB}=+85°C
Mean Time To Failure		795		years	T_{AMB}=+85°C
DC Specifications					
Device Voltage	4.5	5.0	5.5	V	I_{CC}=150mA
Operating Current Range	120	150	170	mA	V_{CC}=5V

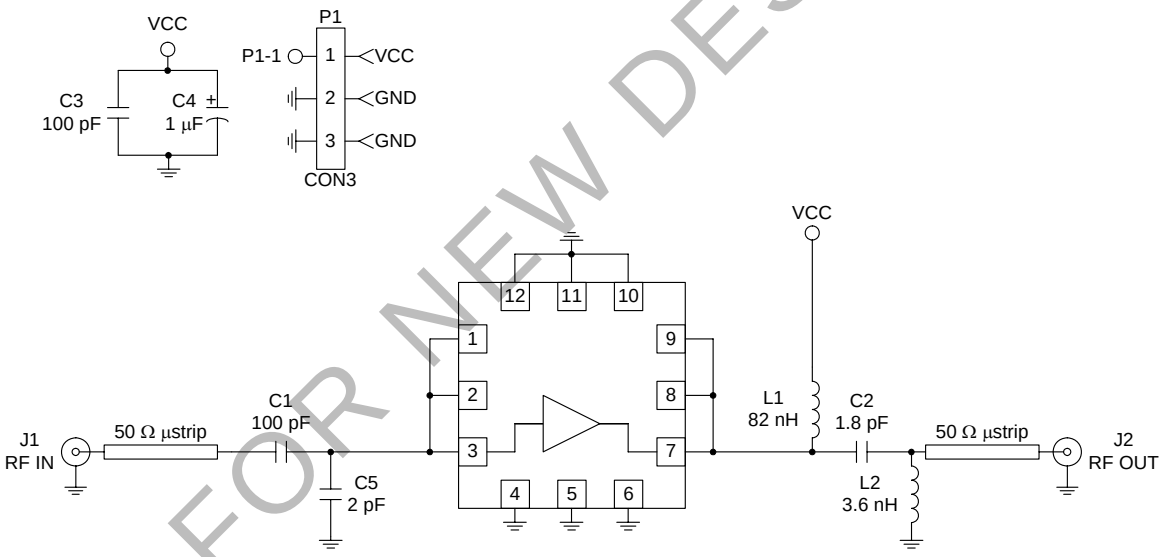
Note: The RF3305 must be operated at or below 150mA in order to achieve the thermal performance listed above. While the RF3305 may be operated at higher bias currents, 150mA is the recommended bias to ensure the highest possible reliability and electrical performance.

Pin	Function	Description	Interface Schematic
1	NC	Not internally connected.	
2	NC	Not internally connected.	
3	RF IN	RF input pin. This pin is not internally DC-blocked. A DC blocking capacitor, suitable for the frequency of operation, should be used in most applications.	
4	GND	Ground.	
5	GND	Ground.	
6	GND	Ground.	
7	RF OUT	RF output and bias pin. For biasing, an RF choke is needed. Because DC is present on this pin, a DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. See application schematic for configuration and value.	
8	NC	Not internally connected.	
9	NC	Not internally connected.	
10	GND	Ground.	
11	GND	Ground.	
12	GND	Ground.	
Pkg Base	GND	Ground connection.	

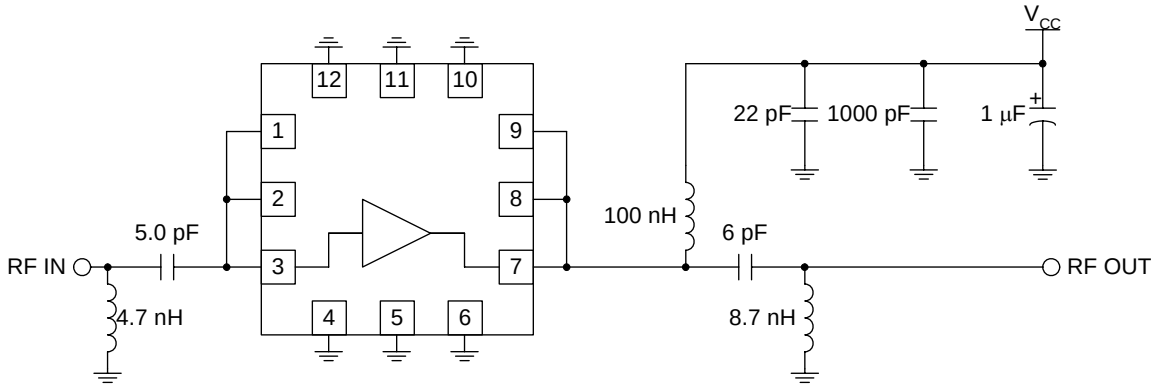
Typical Application Schematic for 2GHz



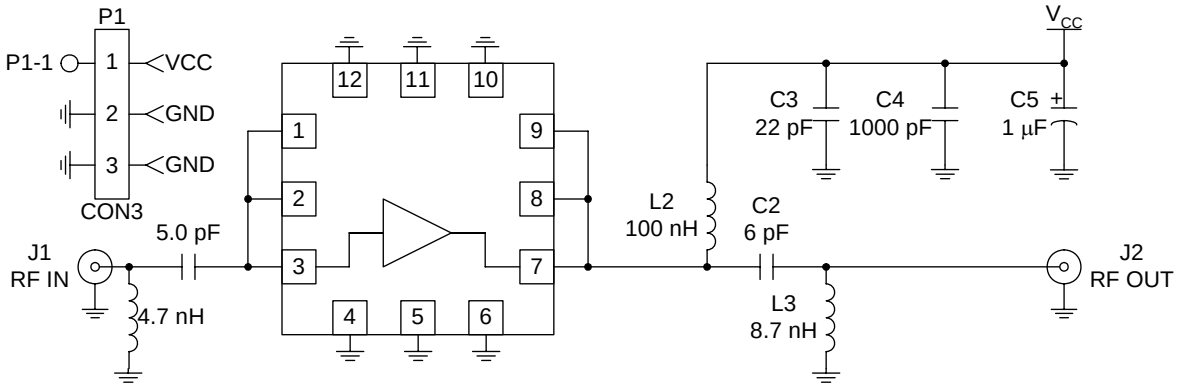
Evaluation Board Schematic for 2GHz



Typical Application Schematic for 900MHz



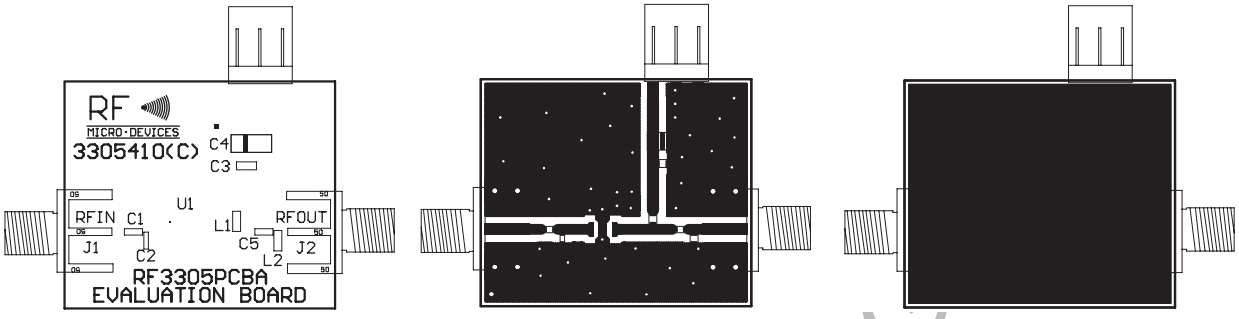
Evaluation Board Schematic for 900MHz



Evaluation Board Layout for 2GHz
Board Size 1.195" x 1.000"

Board Thickness 0.033", Board Material FR-4

Note: A small amount of ground inductance is required to achieve datasheet performance. The necessary inductance may be generated by ensuring that no ground vias are placed directly below the footprint of the part.



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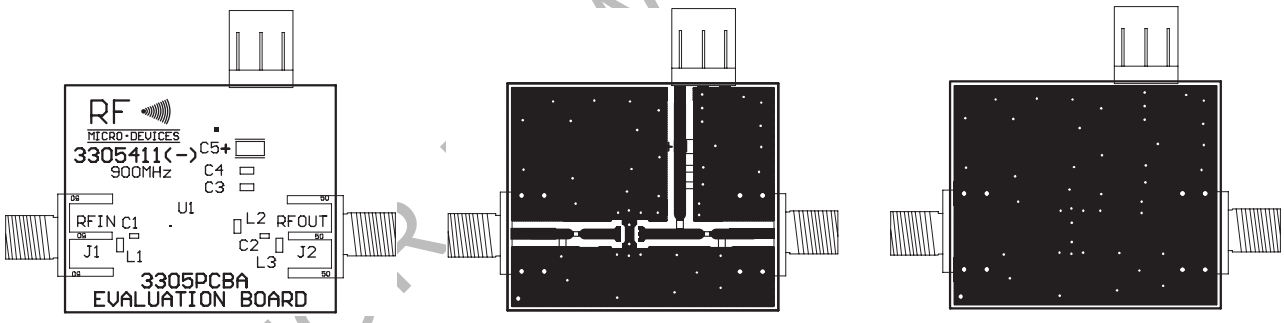
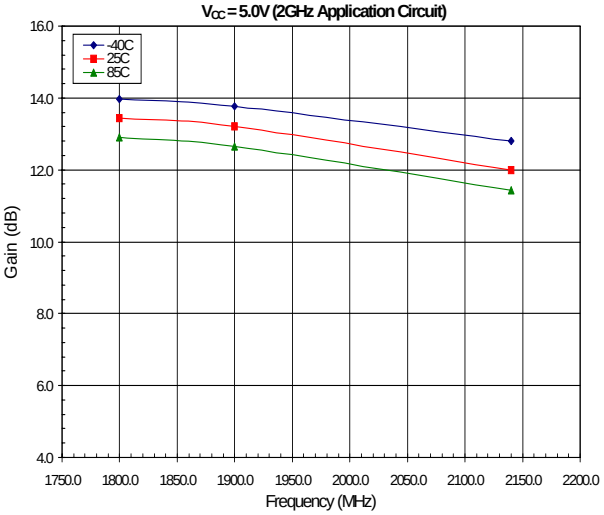
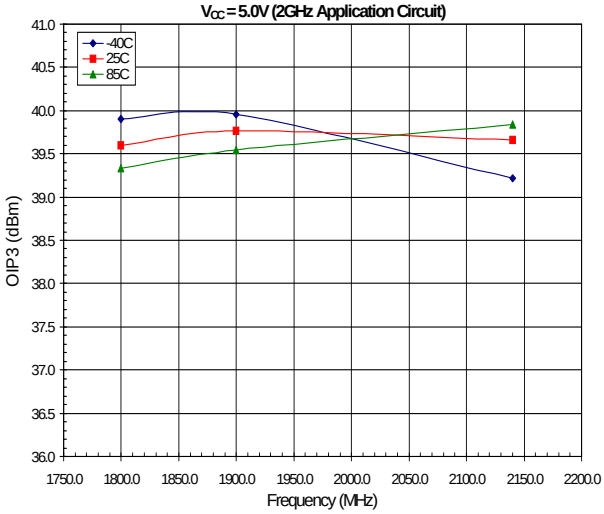


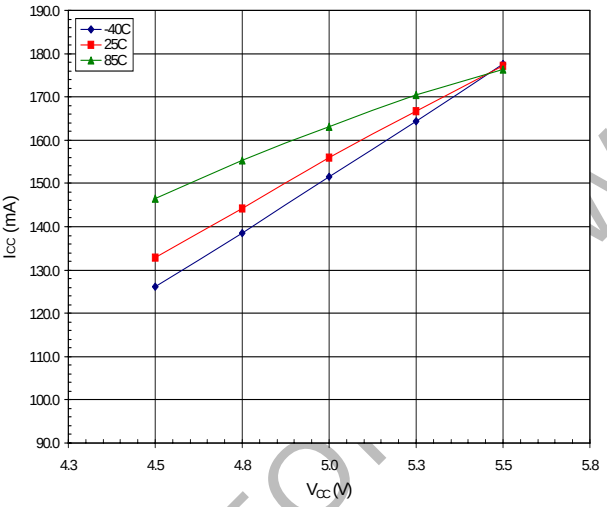
Gain versus Frequency Across Temperature
V_{CC} = 5.0V (2GHz Application Circuit)



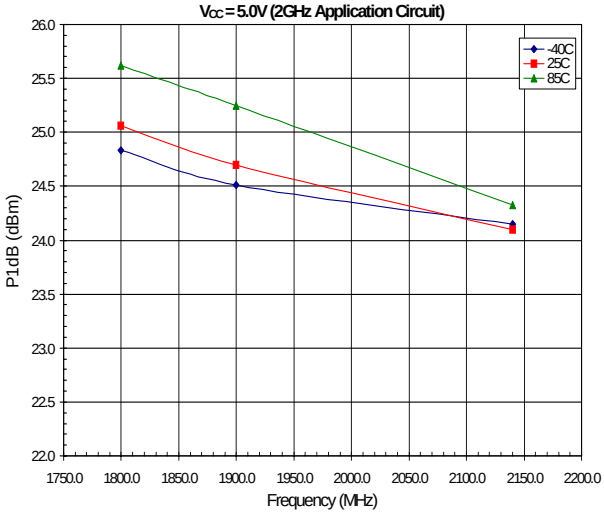
OIP3 versus Frequency Across Temperature
V_{CC} = 5.0V (2GHz Application Circuit)



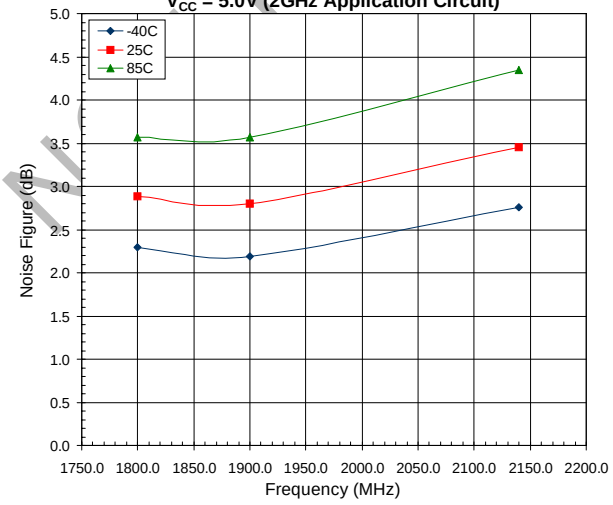
I_{CC} versus V_{CC} Across Temperature



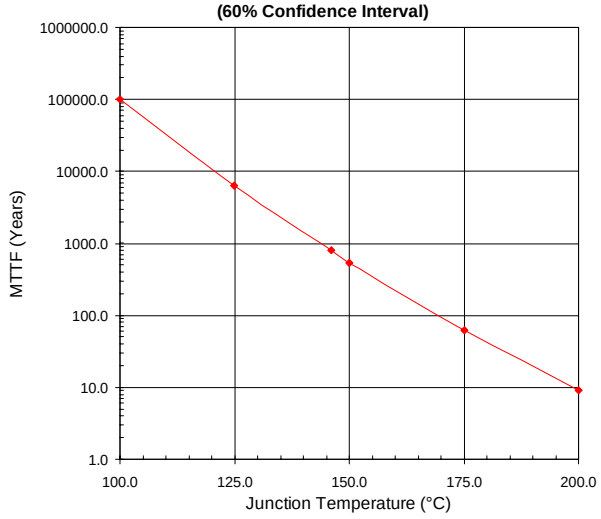
P1dB versus Frequency Across Temperature
V_{CC} = 5.0V (2GHz Application Circuit)

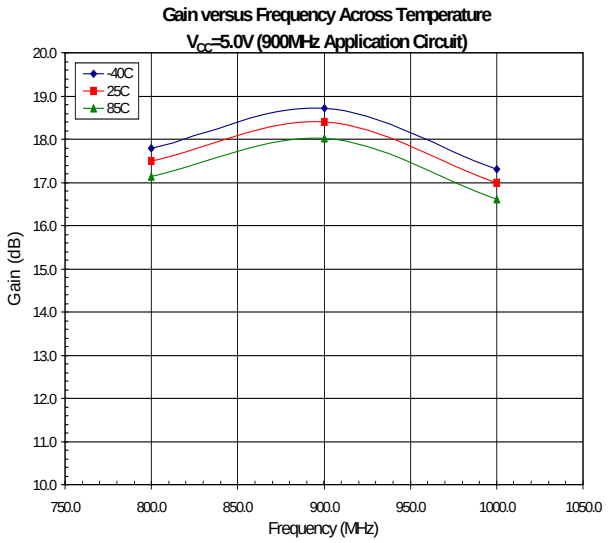


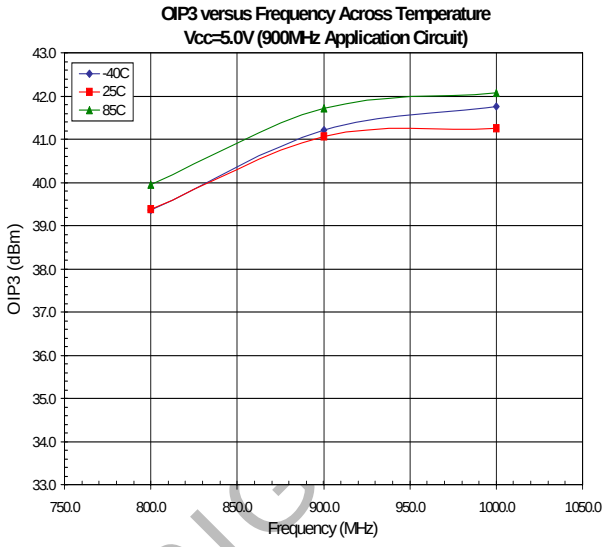
Noise Figure versus Frequency Across Temperature
V_{CC} = 5.0V (2GHz Application Circuit)

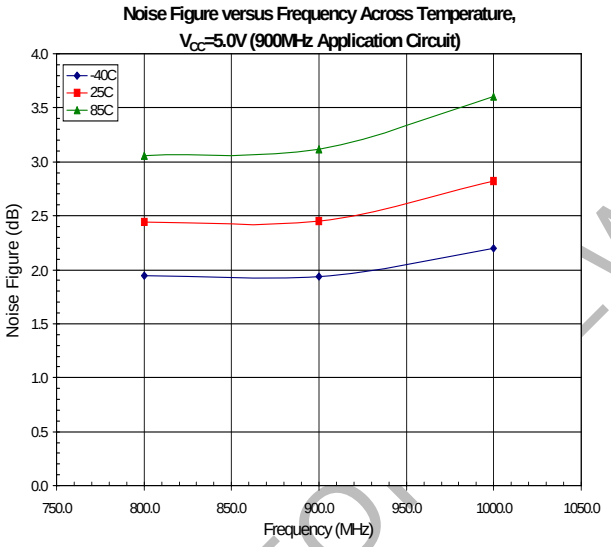


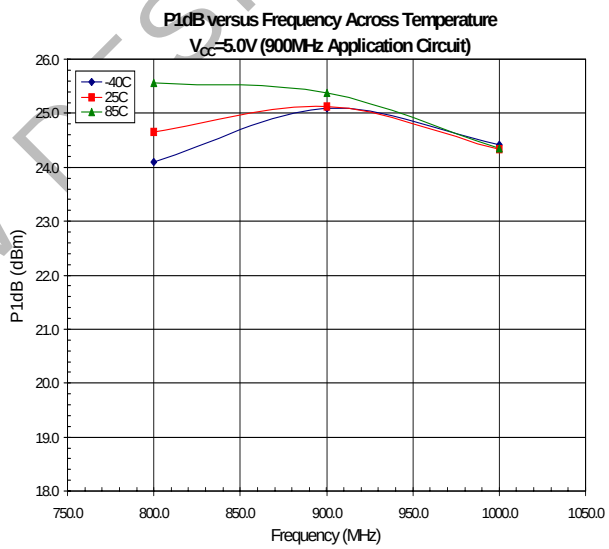
MTTF versus Junction Temperature
(60% Confidence Interval)



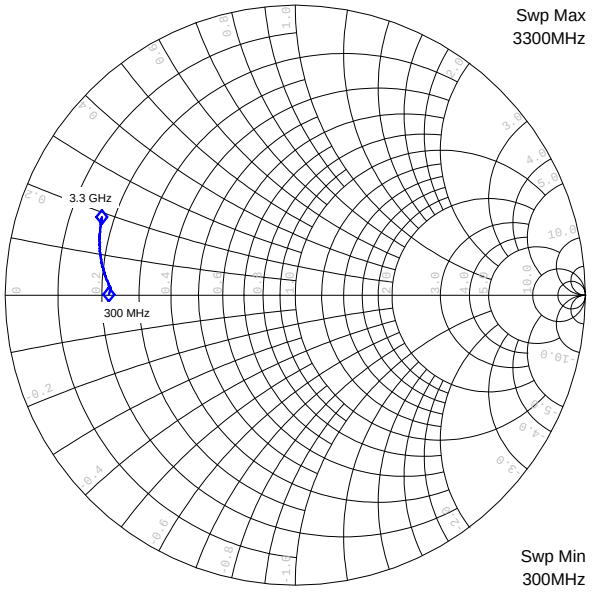




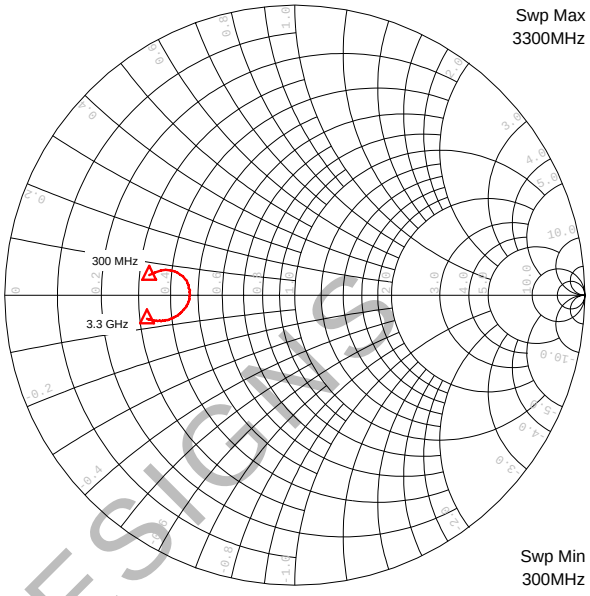




S11



S22



PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is Electroless Nickel, immersion Gold. Typical thickness is 3μinch to 8μinch Gold over 180μinch Nickel.

PCB Land Pattern Recommendation

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; however, it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

PCB Metal Land Mask Pattern

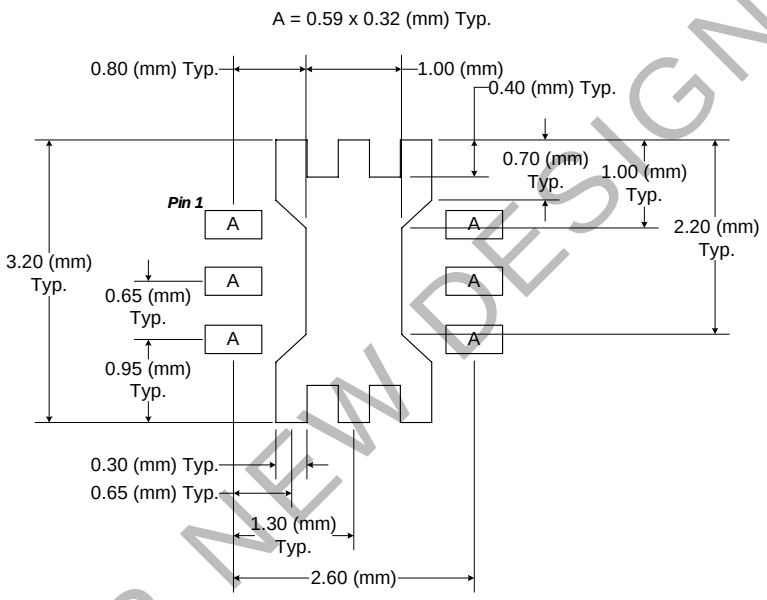


Figure 1. PCB Metal Land Pattern (Top View)

PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

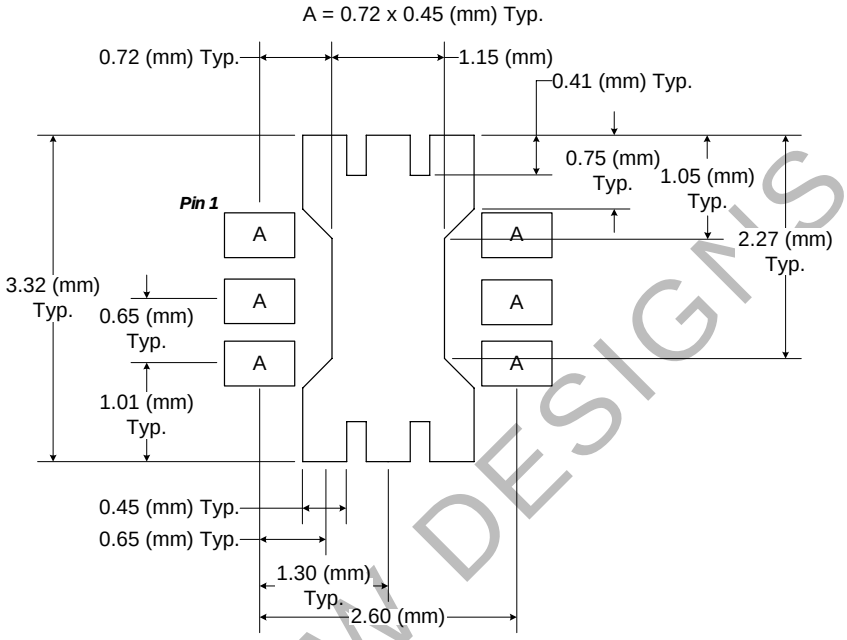


Figure 2. PCB Solder Mask (Top View)

Thermal Pad and Via Design

The PCB metal land pattern has been designed with a thermal pad that matches the exposed die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

NOTE: A small amount of ground inductance is required to achieve data sheet performance. The necessary inductance may be generated by ensuring that no ground vias are placed directly below the footprint of the part.