TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VHCT74F, TC74VHCT74FN, TC74VHCT74FS

DUAL D-TYPE FLIP-FLOP WITH PRESET AND CLEAR

The TC74VHCT74 is an advanced high speed CMOS D-FLIP FLOP fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CK pulse.

$\overline{CLR}$ and $\overline{PR}$ are independent of the CK and are accomplished by setting the appropriate input low.

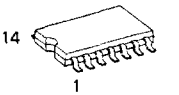
The input voltage are compatible with TTL output voltage.

This device may be used as a level converter for interfacing 3.3V to 5V system.

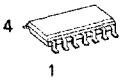
Input protection and output circuit ensure that 0 to 7V can be applied to the input and output pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input/output voltages such as battery back up, hot board insertion, etc.

FEATURES:

- High Speed ····· f_{MAX} = 160MHz(typ.) at V_{CC} = 5V
- Low Power Dissipation····· I_{CC} = 2μA(Max.) at Ta = 25°C
- Compatible with TTL outputs ··· V_{IL} = 0.8V (Max.), V_{IH} = 2.0V (Min.)
- Power Down Protection is provided on all inputs and outputs
- Balanced Propagation Delays····· $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74ALS74



F (SOP14-P-300-1.27)
Weight : 0.18g (TYP.)



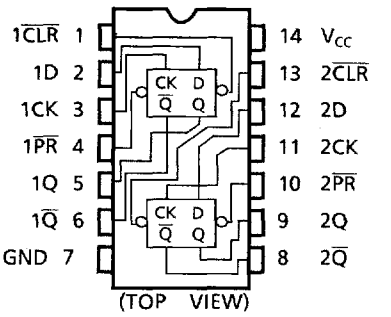
FN (SOL14-P-150-1.27)
Weight : 0.12g (TYP.)

FS (SSOP14-P-225-0.65)
Weight : 0.07g (TYP.)

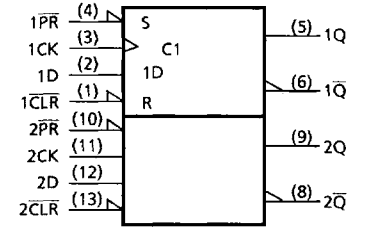
APPLICATION NOTE

This device can drive the components with CMOS input level by adding a external pull up resistor to output terminal.

PIN ASSIGNMENT



IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	—
H	H	L	↑	L	H	—
H	H	H	↑	H	L	—
H	H	X	↓	Q_n	$\overline{Q}_n$	NO CHANGE

X : Don't Care

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ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~7.0	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	−20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~5.5	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dv	0~20	ns / v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITON		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			4.5~5.5	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			4.5~5.5	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	4.5	3.15	3.65	—	3.15	—	V
			I_{OH} = −8mA	4.5	2.50	—	—	2.40	—	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	4.5	—	0.0	0.10	—	0.10	V
			I_{OL} = 8mA	4.5	—	—	0.36	—	0.44	
Input Leakage Current	I_{IN}	V_{IN} = 5.5V or GND		0~5.5	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	2.0	—	20.0	μA
	I_{CCT}	PER INPUT : V_{IN} = 3.4V OTHER INPUT : VCC or GND		5.5	—	—	1.35	—	1.50	mA
Output Leakage Current	I_{OPD}	V_{OUT} = 5.5V		0	—	—	+0.5	—	+5.0	μA

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TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C LIMIT	Ta = −40~85°C LIMIT	UNIT
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$		5.0 ± 0.5	5.0	5.0	ns
Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	$t_{W(L)}$		5.0 ± 0.5	5.0	5.0	
Minimum Set-up Time	t_s		5.0 ± 0.5	5.0	5.0	
Minimum Hold Time	t_h		5.0 ± 0.5	0.0	0.0	
Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	t_{rem}		5.0 ± 0.5	3.5	3.5	

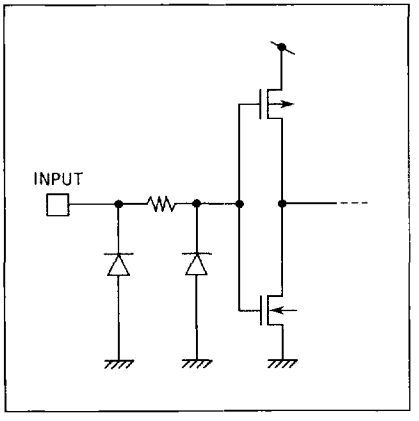
AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	CL (pF)	Ta = 25°C MIN.	TYP.	MAX.	Ta = −40~85°C MIN.	MAX.	UNIT
Propagation Delay Time (CK - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		5.0 ± 0.5	15	—	5.8	7.8	1.0	9.0	ns
				50	—	6.3	8.8	1.0	10.0	
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		5.0 ± 0.5	15	—	7.6	10.4	1.0	12.0	
				50	—	8.1	11.4	1.0	13.0	
Maximum Clock Frequency	f_{MAX}		5.0 ± 0.5	15	100	160	—	80	—	MHz
				50	80	140	—	65	—	
Input Capacitance	C_{IN}				—	4	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 1)			—	24	—	—	—	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation :

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 2 \text{ (per F/F)}$$

INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT