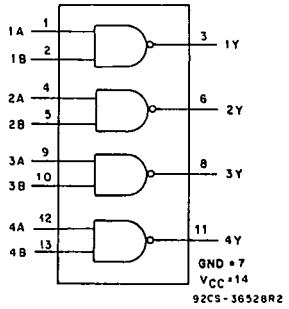
T-43-21-00

CD54/74HC03
CD54/74HCT03

File Number **1832**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Quad 2-Input NAND Gate With Open Drain

Type Features:

- *Buffered inputs*
- *Typical propagation delay = 8 ns @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25° C*
- *Output pull-up to 10 V*

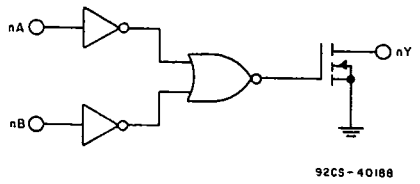
The RCA-CD54/74HC03 and CD54/74HCT03 logic gates utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The 54HCT/74HCT logic family is functionally as well as pin compatible with the standard 54LS/74LS logic family.

These open-drain NAND gates can drive into resistive loads to output voltages as high as 10 V. Minimum values of R_L required vs. load voltage are shown in Fig. 2.

The CD54HC03 and CD54HCT03 are supplied in 14-lead dual-in-line frit-seal ceramic packages (F suffix). The CD74HC03 and CD74HCT03 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High noise immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}, @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL input logic compatibility
  V_{IL} = 0.8 V max., V_{IH} = 2 V Min.
  CMOS input compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



LOGIC DIAGRAM

TRUTH TABLE

A	B	Y	
L	L	Z #	H *
H	L	Z #	H *
L	H	Z #	H *
H	H	L	

* Requires pull-up (R_L to V_L)
\# Without pull-up (high impedance)

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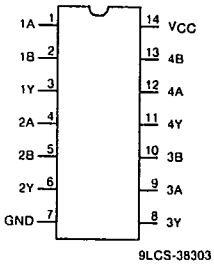
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V) ..... -20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O$) ..... -25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) ..... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Lineary at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 In. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}: *			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input Voltage V_I	0	V_{CC}	V
DC Load Voltage V_L	0	10 #	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

* Unless otherwise specified, all voltages are referenced to Ground.
# With pull-up resistor whose value limits output current to 25 mA.



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TERMINAL ASSIGNMENT

CD54/74HC03
CD54/74HCT03

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC03/CD54HC03										CD74HCT03/CD54HCT03									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C		
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	2	—	20	—	40	V_{CC} or Gnd	5.5	—	—	2	—	20	—	40	μA
Additional Quiescent Device Current per Input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA
Output Leakage Current I_{OZ}	V_{IL}	V_O = 10 V thru 1 KΩ	6	—	—	0.5	—	5	—	10	$V_I = V_{IL}$ V_O = 10 V thru 1 KΩ	5.5	—	—	0.5	—	5	—	10	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS *
nA, nB	1

* Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

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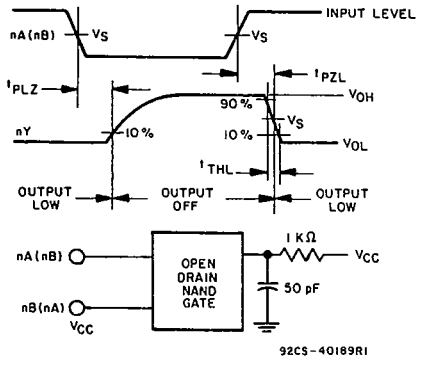
SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL VALUES HC	TYPICAL VALUES HCT	UNITS
Propagation Delay, (Fig. 1)	t_{PZL}, t_{PLZ}	15	8	9	ns
Power Dissipation Capacitance *	C_{PD}	—	6.4	9	pF

* C_{PD} is used to determine the dynamic power consumption, per gate.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) + \Sigma (V_L^2/R_L)$ (Duty Factor "Low")
where f_i = input frequency; f_o = output frequency; C_L = output load capacitance; V_{CC} = supply voltage
Duty factor "low" = percent of time output is "low"; V_L = output voltage; R_L = pull-up resistor

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	TEST CONDITIONS V_{CC} V	LIMITS 25°C HC Min.	25°C HC Max.	25°C HCT Min.	25°C HCT Max.	-40°C to +85°C 74HC Min.	-40°C to +85°C 74HC Max.	-40°C to +85°C 74HCT Min.	-40°C to +85°C 74HCT Max.	-55°C to +125°C 54HC Min.	-55°C to +125°C 54HC Max.	-55°C to +125°C 54HCT Min.	-55°C to +125°C 54HCT Max.	UNITS
Propagation Delay t_{PLZ} Output Low to t_{PZL} High Impedance and High Impedance to Output Low	2	—	100	—	—	—	125	—	—	—	150	—	—	ns
	4.5	—	20	—	24	—	25	—	30	—	30	—	36	
	6	—	17	—	—	—	21	—	—	—	26	—	—	
Transition Times t_{THL} (Figure 1)	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
	6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 1 - Transition times, propagation delay times, and test circuit.

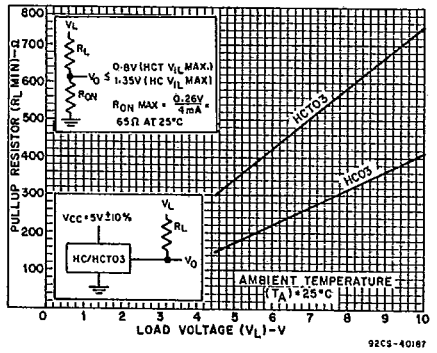


Fig. 2 - Minimum resistive load vs load voltage.