DATA SHEET

74F841/842/843/845/846
Bus interface latches

Product specification

1999 Jun 23

Replaces datasheet 74F841/842/843/844/845/846 of 1999 Jan 08
IC15 Data Handbook

Philips
Semiconductors

PHILIPS

Bus interface latches

74F841/74F842/74F843/ 74F845/74F846

74F841/74F842 10-bit bus interface latches, non-inverting/inverting (3-State)
74F843 9-bit bus interface latch, non-inverting (3-State)
74F845/74F846 8-bit bus interface latches, non-inverting/inverting (3-State)

FEATURES

- High speed parallel latches
- Extra data width for wide address/data paths or buses carrying parity
- High impedance NPN base input structure minimizes bus loading
- IIL is 20μA vs 1000A for AM29841 series
- Buffered control inputs to reduce AC effects
- Ideal where high speed, light loading, or increased fan-in are required as with MOS microprocessors
- Positive and negative over-shoots are clamped to ground
- 3-State outputs glitch free during power-up and power-down
- 48mA sink current
- Slim dual in-line 300 mil package
- Broadside pinout
- Pin-for-pin and function compatible with AMD AM29841-846 series

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F841, 74F842	5.5ns	60mA
74F843, 74F845	5.5ns	75mA
74F846	6.2ns	60mA

DESCRIPTION

The 74F841–74F846 bus interface latch series are designed to provide extra data width for wider address/data paths of buses carrying parity.

The 74F841–74F846 series are funcitonally an pin compatible to the AMD AM29841–AM29846 series.

The 74F841 consists of ten D-type latches with 3-State outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is High. This allows asynchronous operation, as the output transition follows the data in transition. On the LE High-to-Low transition, the data that meets the setup and hold time is latched.

Data appears on the bus when the Output Enable ($\overline{OE}$) is Low. When $\overline{OE}$ is High the output is in the High-impedance state.

The 74F842 is the inverted output version of the 74F841.

The 74F843 consists of nine D-type latches with 3-State outputs. In addition to the LE and $\overline{OE}$ pins, the 74F843 has a Master Reset ($\overline{MR}$) pin and Preset ($\overline{PRE}$) pin. These pins are ideal for parity bus interfacing in high performance systems. When $\overline{MR}$ is Low, the outputs are Low if $\overline{OE}$ is Low. When $\overline{MR}$ is High, data can be entered into the latch. When $\overline{PRE}$ is Low, the outputs are High, if $\overline{OE}$ is Low, $\overline{PRE}$ overrides $\overline{MR}$.

The 74F845 consists of eight D-type latches with 3-State outputs. In addition to the LE, $\overline{OE}$, $\overline{MR}$ and $\overline{PRE}$ pins, the 74F845 has two addtitional $\overline{OE}$ pins making a total of three Output Enables ($\overline{OE}$0, $\overline{OE}$1, $\overline{OE}$2) pins.

The multiple Ouptut Enables ($\overline{OE}$0, $\overline{OE}$1, $\overline{OE}$2) allow multi-user control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$.

The 74F846 is the inverted output version of the 74F845.

ORDERING INFORMATION

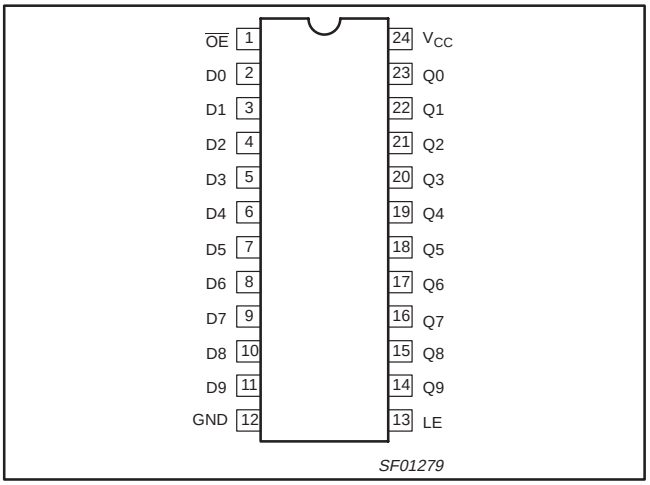
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_{amb} = 0°C to +70°C	PACKAGE DRAWING NUMBER
24-pin plastic Slim DIP (300 mil)	N74F841N, N74F842N, N74F843N, N74F845N, N74F846N	SOT222-1
24-pin plastic SOL	N74F841D, N74F842D, N74F843D, N74F845D, N74F846D	SOT137-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

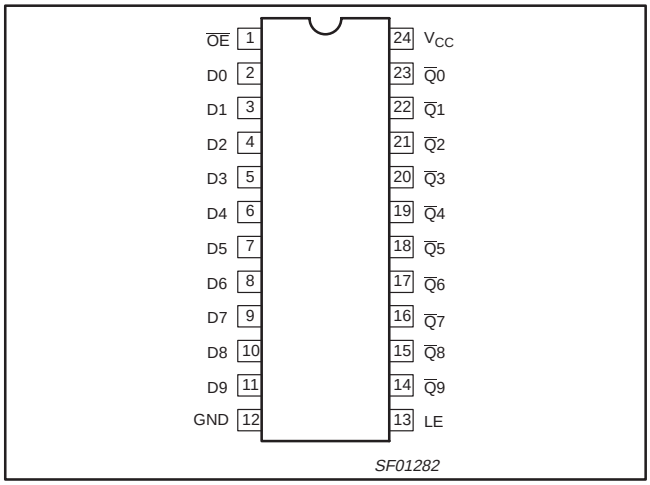
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dn	Data inputs	1.0/0.033	20μA/20μA
LE	Latch Enable input	1.0/0.033	20μA/20μA
$\overline{OE}$, $\overline{OE}$n	Output Enable input (active Low)	1.0/0.033	20μA/20μA
$\overline{MR}$	Master Reset input (active Low)	1.0/0.033	20μA/20μA
$\overline{PRE}$	Preset input (active Low)	1.0/0.033	20μA/20μA
Qn	Data outputs	1200/80	24mA/48mA
$\overline{Q}$n	Data outputs	1200/80	24mA/48mA

NOTE: One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

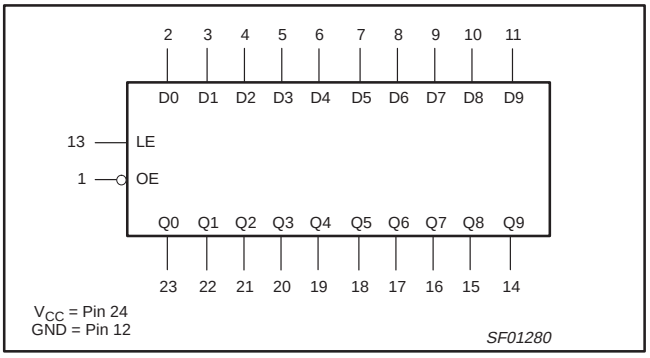
PIN CONFIGURATION for 74F841



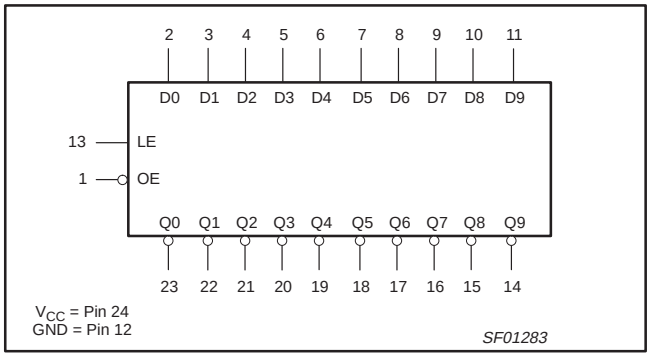
PIN CONFIGURATION for 74F842



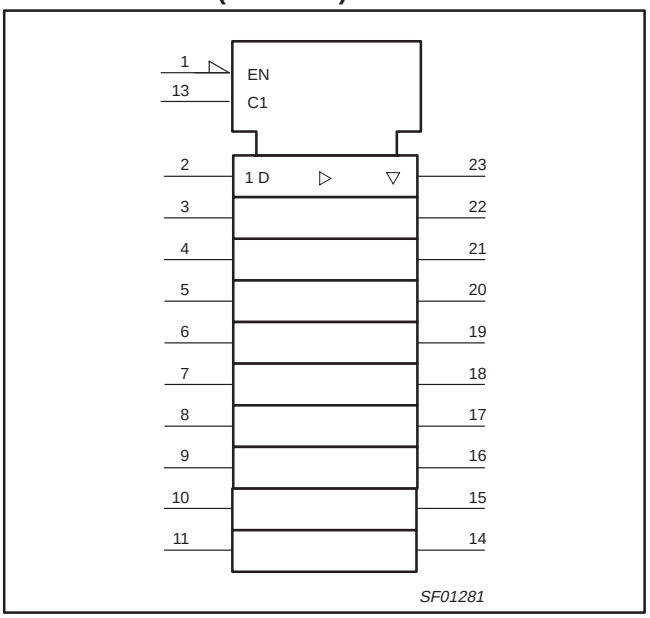
LOGIC SYMBOL for 74F841



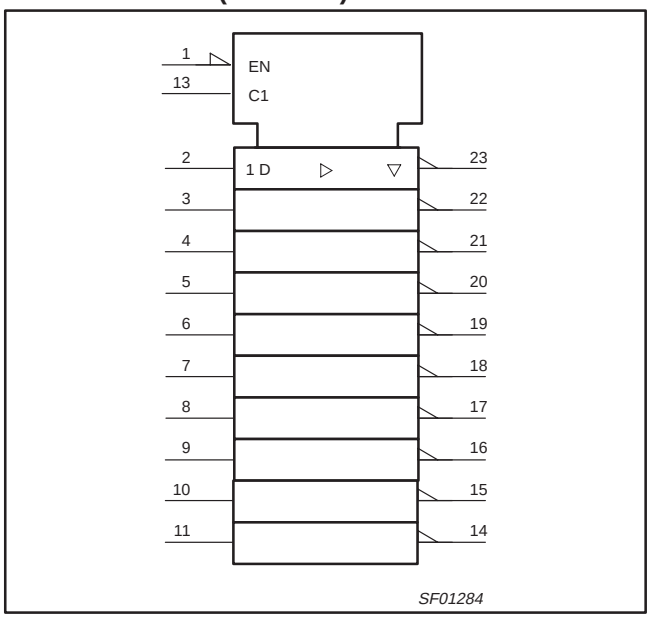
LOGIC SYMBOL for 74F842



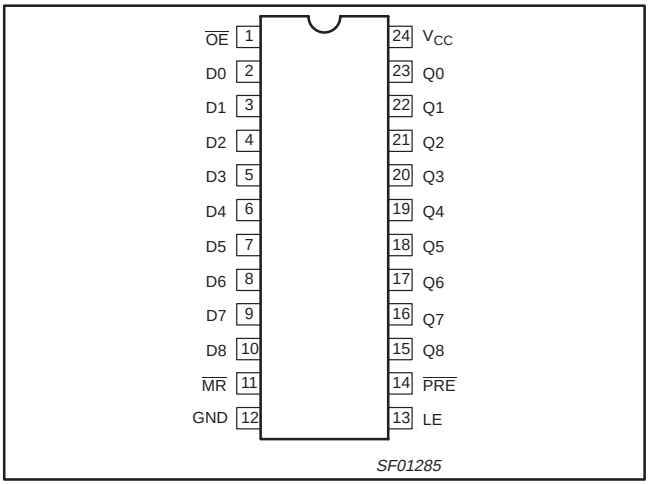
LOGIC SYMBOL (IEEE/IEC) for 74F841



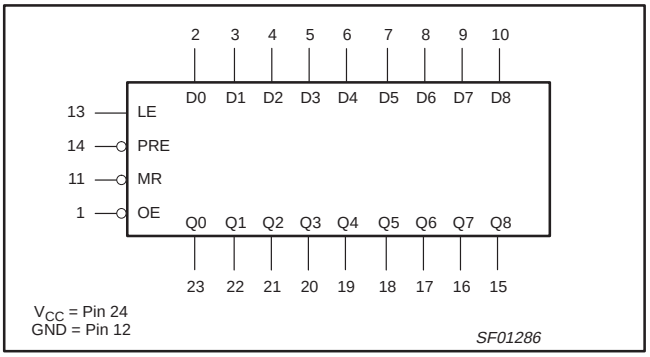
LOGIC SYMBOL (IEEE/IEC) for 74F842



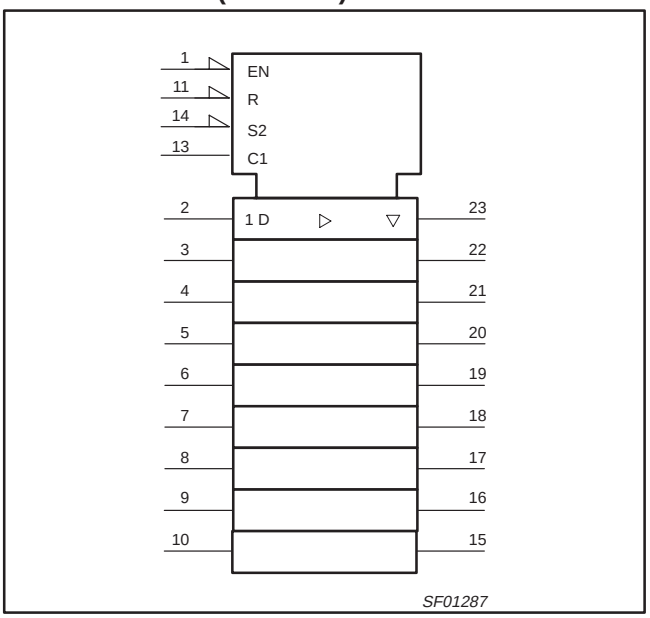
PIN CONFIGURATION for 74F843



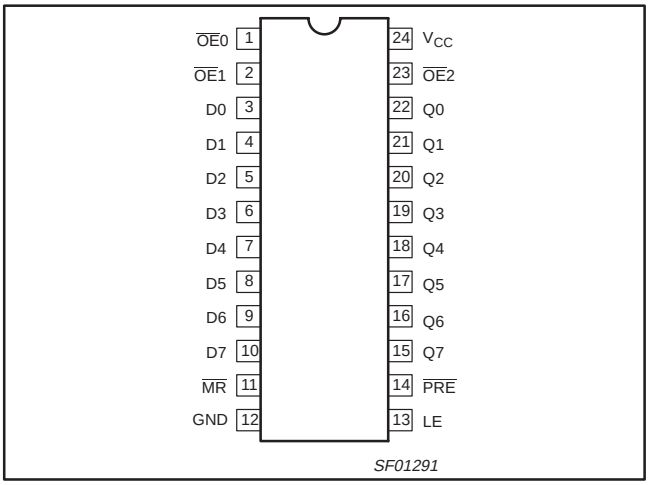
LOGIC SYMBOL for 74F843



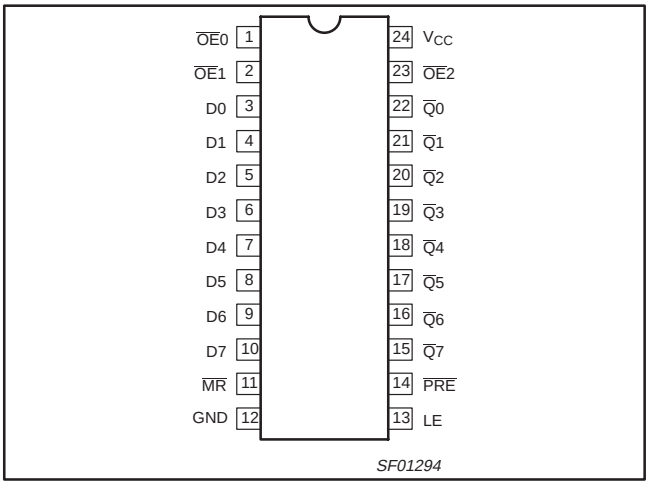
LOGIC SYMBOL (IEEE/IEC) for 74F843



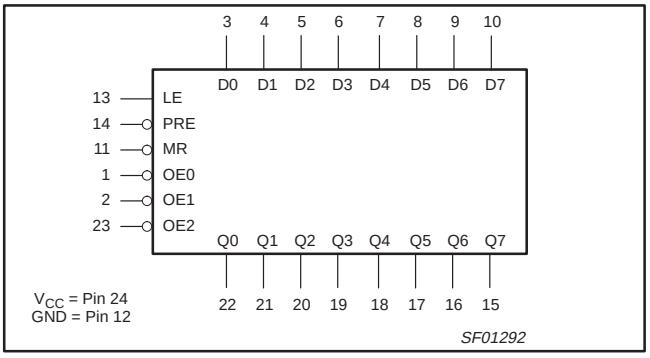
PIN CONFIGURATION for 74F845



PIN CONFIGURATION for 74F846



LOGIC SYMBOL for 74F845



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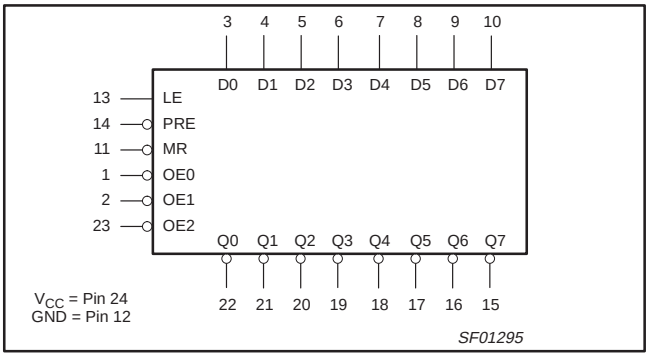
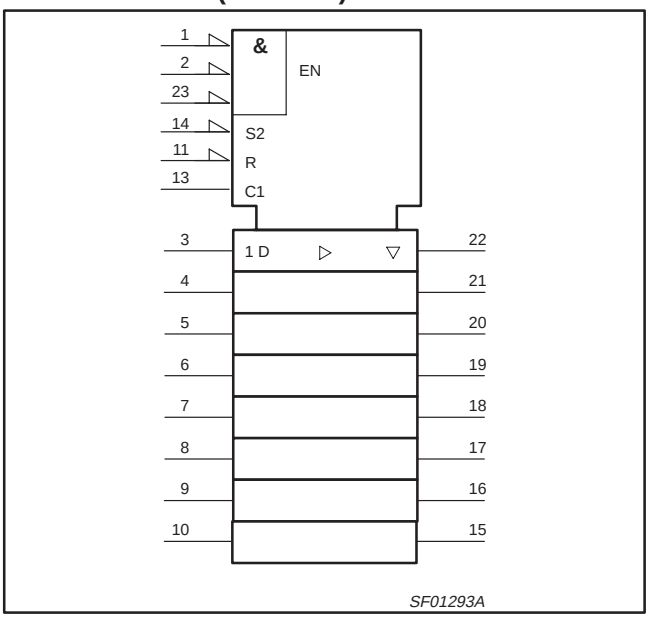
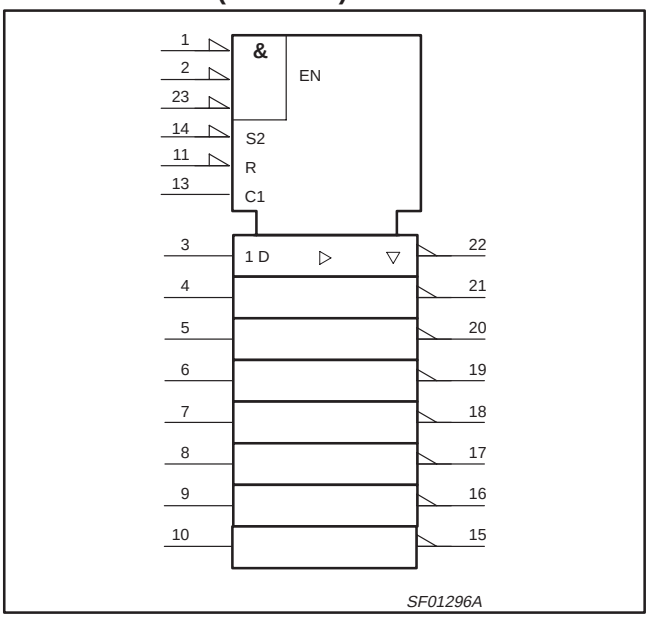


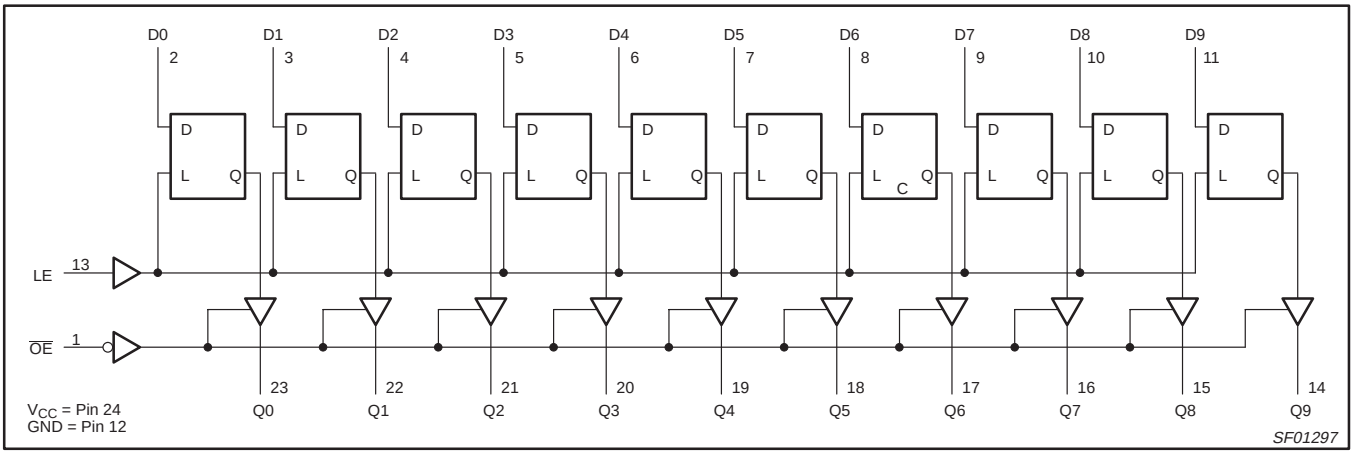
LOGIC SYMBOL (IEEE/IEC) for 74F845



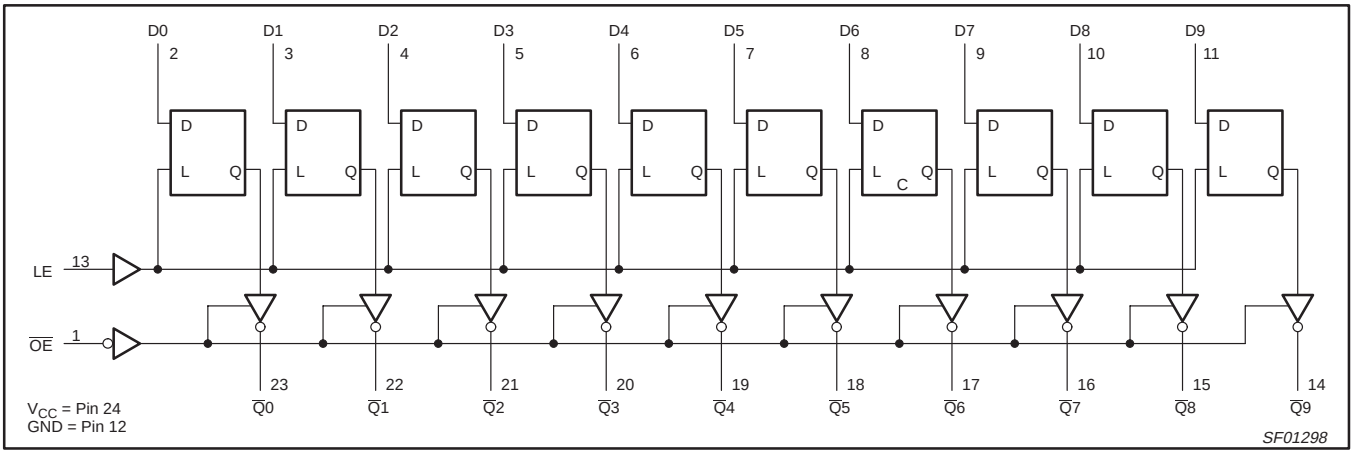
LOGIC SYMBOL (IEEE/IEC) for 74F846



LOGIC DIAGRAM for 74F841



LOGIC DIAGRAM for 74F842

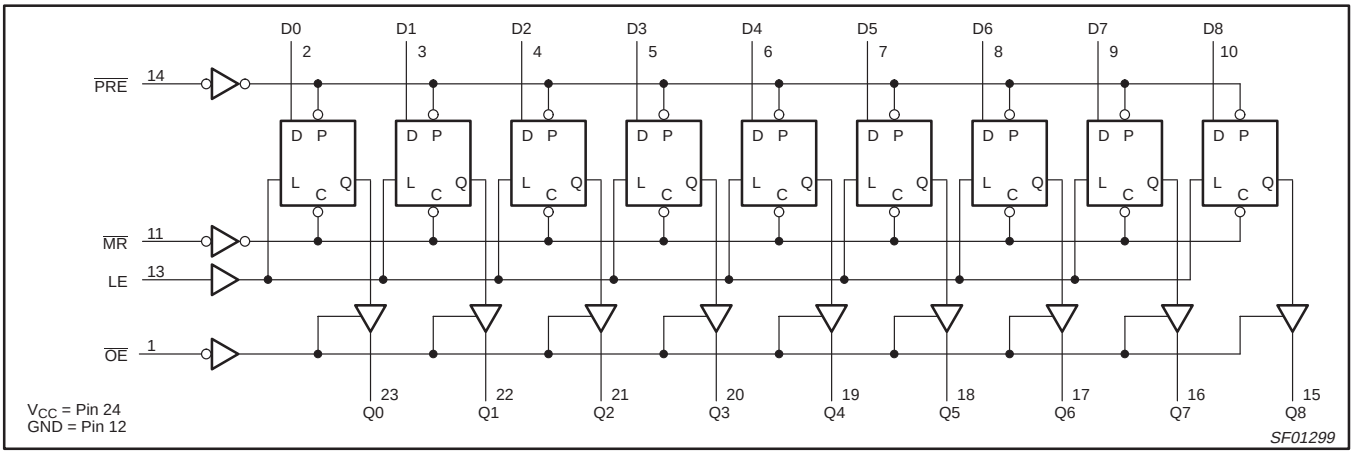


FUNCTION TABLE for 74F841 and 74F842

INPUTS			OUTPUTS		OPERATING MODE
			74F841	74F842	
$\overline{OE}$	LE	Dn	Qn	$\overline{Q}n$	
L	H	L	L	H	Transparent
L	H	H	H	L	
L	↓	l	L	H	Latched
L	↓	h	H	L	
H	X	X	Z	Z	High Impedance
L	L	X	NC	NC	Hold

H = High voltage level
L = Low voltage level
h = High state one setup time before the High-to-Low LE transition
l = Low state one setup time before the High-to-Low LE transition
↓ = High-to-Low transition
X = Don't care
NC= No change
Z = High impedance "off" state

LOGIC DIAGRAM for 74F843

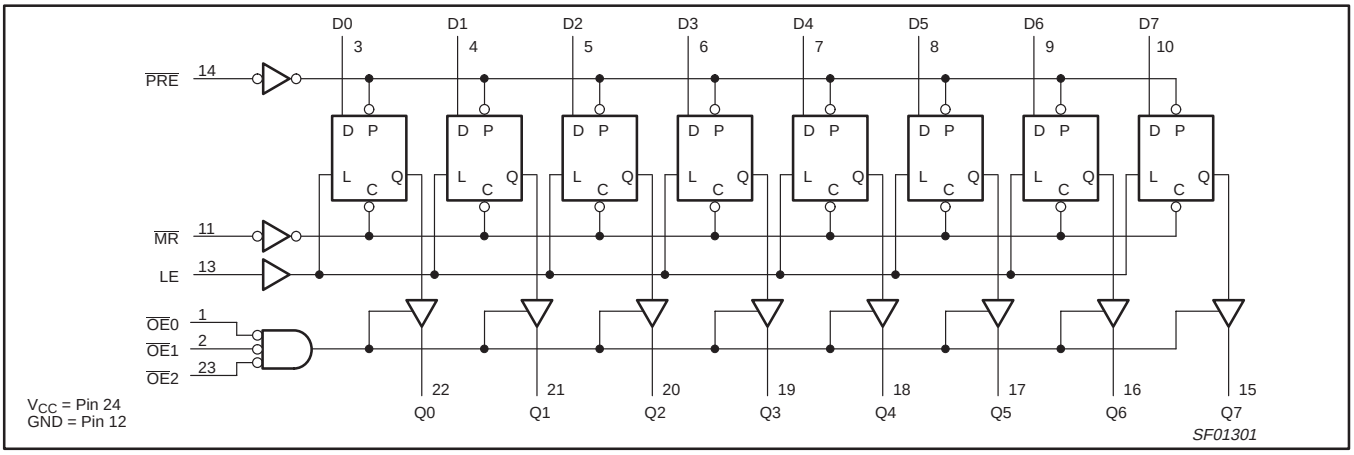


FUNCTION TABLE for 74F843

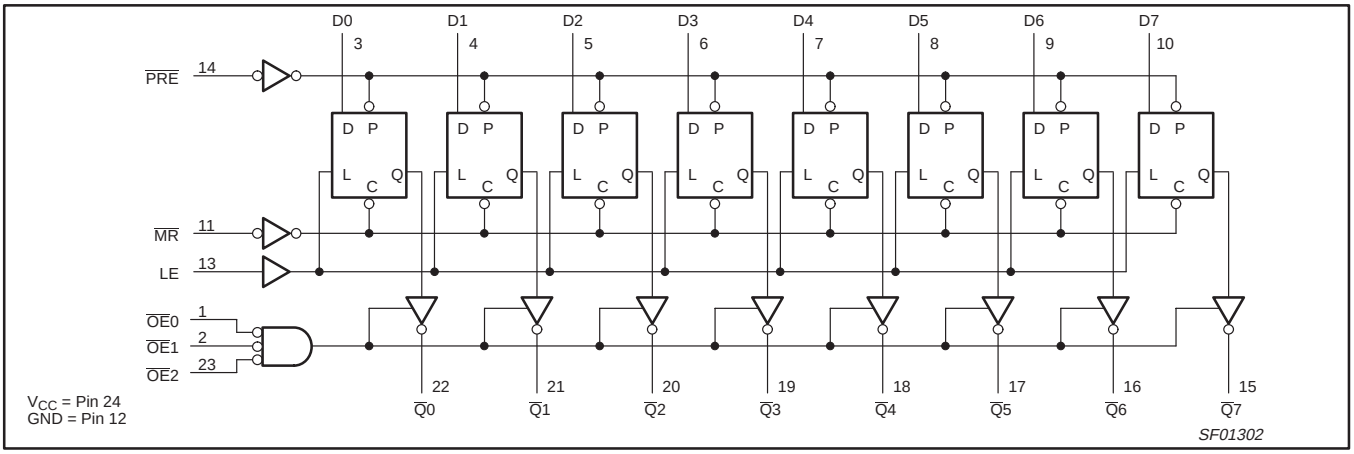
INPUTS					OUTPUTS	OPERATING MODE
					74F843	
$\overline{OE}$	$\overline{PRE}$	$\overline{MR}$	LE	Dn	Qn	
L	L	X	X	X	H	Preset
L	H	L	X	X	L	Clear
L	H	H	H	L	L	Transparent
L	H	H	H	H	H	
L	H	H	↓	l	L	Latched
L	H	H	↓	h	H	
H	X	X	X	X	Z	High Impedance
L	H	H	L	X	NC	Hold

H = High voltage level
L = Low voltage level
h = High state one setup time before the High-to-Low LE transition
l = Low state one setup time before the High-to-Low LE transition
↓ = High-to-Low transition
X = Don't care
NC= No change
Z = High impedance "off" state

LOGIC DIAGRAM for 74F845



LOGIC DIAGRAM for 74F846



FUNCTION TABLE for 74F845 and 74F846

INPUTS					OUTPUTS		OPERATING MODE
					74F845	74F846	
$\overline{OE}$	$\overline{PRE}$	$\overline{MR}$	LE	Dn	Qn	$\overline{Q}$n	
L	L	X	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	H	H	H	L	L	H	Transparent
L	H	H	H	H	H	L	
L	H	H	↓	l	L	H	Latched
L	H	H	↓	h	H	L	
H	X	X	X	X	Z	Z	High Impedance
L	H	H	L	X	NC	NC	Hold

H = High voltage level
L = Low voltage level
h = High state one setup time before the High-to-Low LE transition
l = Low state one setup time before the High-to-Low LE transition
↓ = High-to-Low transition
X = Don't care
NC = No change
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	84	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–24	mA
I_{OL}	Low-level output current			48	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –15mA	±10%V_{CC}	2.2			V
					±5%V_{CC}	2.2	3.3		V
				I_{OH} = –24mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 32mA	±10%V_{CC}		0.38	0.55	V
				I_{OL} = 48mA	±5%V_{CC}		0.38	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					–50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			–100		–225	mA
I_{CC}	Supply current (total)	74F841	I_{CCH}	V_{CC} = MAX			50	65	mA
			I_{CCL}				60	80	mA
			I_{CCZ}				70	92	mA
		74F842	I_{CCH}	V_{CC} = MAX			40	60	mA
			I_{CCL}				65	90	mA
			I_{CCZ}				60	90	mA
		74F843 74F845	I_{CCH}	V_{CC} = MAX			65	90	mA
			I_{CCL}				75	100	mA
			I_{CCZ}				85	115	mA
		74F846	I_{CCH}	V_{CC} = MAX			50	70	mA
			I_{CCL}				70	95	mA
			I_{CCZ}				70	95	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS for 74F841/74F842

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	74F841	Waveform 1, 2	2.0 2.5	4.0 4.5	7.5 7.5	2.0 2.5	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay LE to Qn		Waveform 1, 2	4.5 4.0	6.5 6.0	9.5 9.0	4.0 3.5	10.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay Dn to $\overline{Q}$n	74F842	Waveform 1, 2	3.5 3.0	5.5 5.0	8.5 8.0	4.5 4.0	9.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay LE to $\overline{Q}$n		Waveform 1, 2	5.0 4.5	7.0 6.5	10.0 9.0	3.0 3.0	10.5 9.5	ns
t_{PZH} t_{PZL}	Output enable time High or Low-level $\overline{OE}$n to Qn or $\overline{Q}$n		Waveform 5 Waveform 6	2.5 4.0	4.5 6.0	8.0 9.5	2.0 3.0	8.5 10.5	ns
t_{PHZ} t_{PLZ}	Output disable time High or Low-level $\overline{OE}$n to Qn or $\overline{Q}$n		Waveform 5 Waveform 6	1.0 1.0	4.5 5.0	8.0 8.0	1.0 1.0	8.5 8.5	ns

AC SETUP REQUIREMENTS for 74F841/74F842

SYMBOL	PARAMETER		TEST CONDITION	LIMITS				UNIT
				T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω		T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low Dn to LE		Waveform 4	0.0 0.0		1.0 1.0		ns
t_h(H) t_h(L)	Hold time, High or Low Dn to LE	74F841	Waveform 4	2.5 3.0		3.0 4.0		ns
t_w(H)	LE pulse width, High		Waveform 4	3.5		4.0		ns
t_h(H) t_h(L)	Hold time, High or Low Dn to LE	74F842	Waveform 4	3.0 3.5		3.5 4.5		ns
t_w(H)	LE pulse width, High		Waveform 4	3.0		3.0		ns

AC ELECTRICAL CHARACTERISTICS for 74F843/74F845

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	Waveform 1, 2	2.0 2.5	4.5 4.5	7.5 8.0	2.0 2.5	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay LE to Qn	Waveform 1, 2	4.5 4.0	6.5 6.0	9.5 8.5	4.5 4.0	10.0 8.5	ns
t_{PLH}	Propagation delay $\overline{PRE}$ to Qn	Waveform 3	3.5	5.5	8.5	3.0	9.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn	Waveform 3	2.0	4.5	7.5	2.0	8.0	ns
t_{PZH} t_{PZL}	Output enable time High or Low-level $\overline{OE}$n to Qn	Waveform 5 Waveform 6	2.5 4.0	4.5 6.0	7.5 9.5	2.0 3.0	8.0 10.5	ns
t_{PHZ} t_{PLZ}	Output disable time High or Low-level $\overline{OE}$n to Qn	Waveform 5 Waveform 6	1.0 1.0	4.5 5.0	8.0 8.0	1.0 1.0	8.5 8.5	ns

AC SETUP REQUIREMENTS for 74F843/74F845

SYMBOL	PARAMETER	TEST CONDITION	LIMITS				UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω		T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low Dn to LE	Waveform 4	1.0 1.0		0.0 0.0		ns
t_h(H) t_h(L)	Hold time, High or Low Dn to LE	Waveform 4	3.0 4.0		3.0 4.0		ns
t_w(H)	LE pulse width, High	Waveform 4	3.0		3.0		ns
t_w(L)	$\overline{PRE}$ pulse width, Low	Waveform 3	4.0		5.0		ns
t_w(H)	$\overline{MR}$ pulse width, Low	Waveform 3	4.0		5.0		ns
t_{REC}	$\overline{PRE}$ recovery time	Waveform 3	0.0		0.0		ns
t_{REC}	$\overline{MR}$ recovery time	Waveform 3	3.5		4.5		ns

AC ELECTRICAL CHARACTERISTICS for 74F846

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to $\overline{Q}$n	Waveform 1, 2	3.5 3.0	5.5 5.0	8.5 8.0	3.0 3.0	9.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay LE to $\overline{Q}$n	Waveform 1, 2	5.0 4.5	7.0 6.5	10.0 9.0	5.0 4.5	10.5 9.5	ns
t_{PLH}	Propagation delay $\overline{PRE}$ to $\overline{Q}$n	Waveform 3	3.5	5.5	8.5	3.0	9.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to $\overline{Q}$n	Waveform 3	5.0	7.0	10.0	4.5	10.5	ns
t_{PZH} t_{PZL}	Output enable time High or Low-level $\overline{OE}$n to $\overline{Q}$n	Waveform 5 Waveform 6	2.5 4.0	5.0 6.0	7.5 9.5	2.0 3.0	8.0 10.5	ns
t_{PHZ} t_{PLZ}	Output disable time High or Low-level $\overline{OE}$n to $\overline{Q}$n	Waveform 5 Waveform 6	1.0 1.0	4.5 5.0	8.0 8.0	1.0 1.0	8.5 8.5	ns

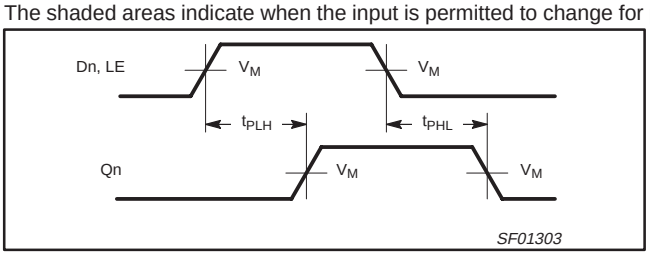
AC SETUP REQUIREMENTS for 74F846

SYMBOL	PARAMETER	TEST CONDITION	LIMITS				UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω		T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low Dn to LE	Waveform 4	0.0 0.0		0.0 0.0		ns
t_h(H) t_h(L)	Hold time, High or Low Dn to LE	Waveform 4	3.0 4.0		3.0 4.0		ns
t_w(H)	LE pulse width, High	Waveform 4	3.0		3.0		ns
t_w(L)	$\overline{PRE}$ pulse width, Low	Waveform 3	4.0		5.0		ns
t_w(H)	$\overline{MR}$ pulse width, Low	Waveform 3	4.0		5.0		ns
t_{REC}	$\overline{PRE}$ recovery time	Waveform 3	0.0		0.0		ns
t_{REC}	$\overline{MR}$ recovery time	Waveform 3	3.5		4.5		ns

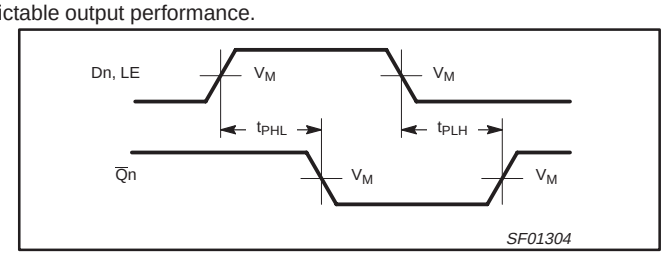
AC WAVEFORMS

For all waveforms, V_M = 1.5V.

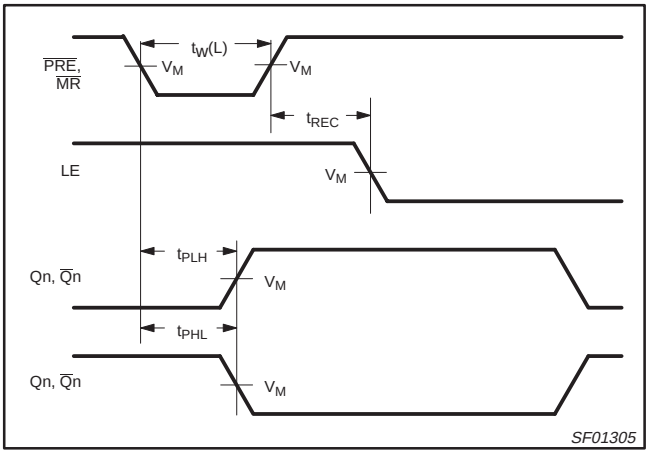
The shaded areas indicate when the input is permitted to change for predictable output performance.



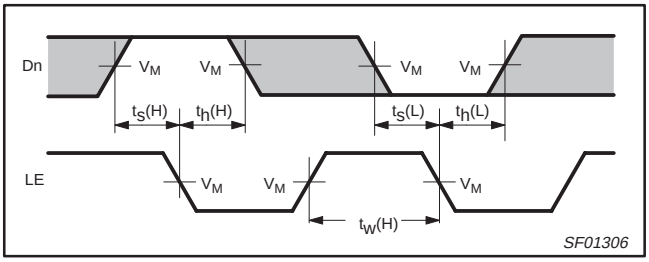
Waveform 1. Propagation Delay, Non-Inverting Path



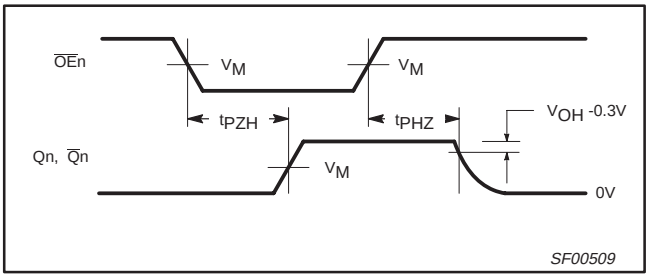
Waveform 2. Propagation Delay, Inverting Path



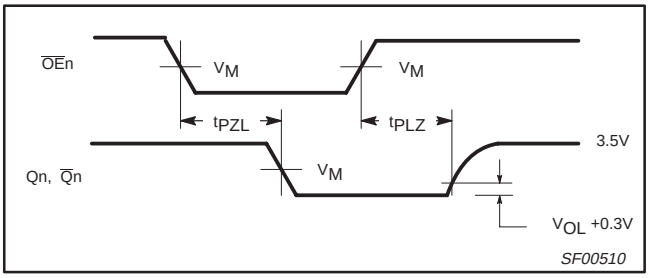
Waveform 3. Master Reset and Preset Pulse Width, Master Reset and Preset to Output Delay, and Master Reset and Preset to Latch Enable Recovery Time



Waveform 4. Data Setup and Hold Times

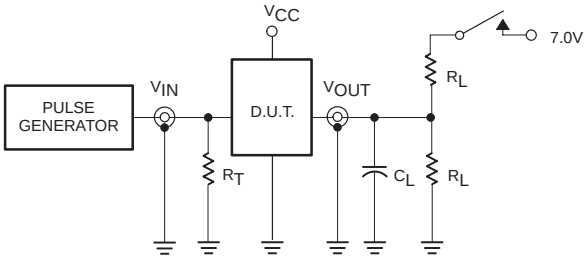


Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level

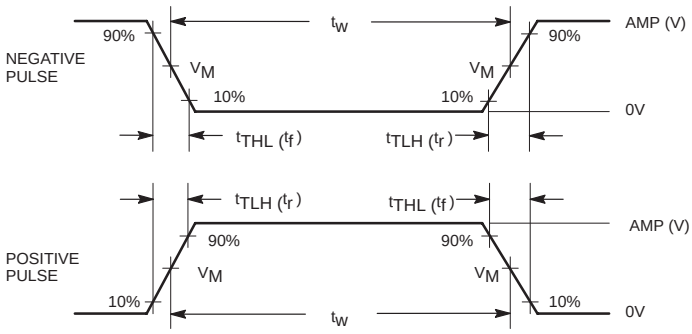


Waveform 6. 3-State Output Enable Time to Low Level and Output Disable time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

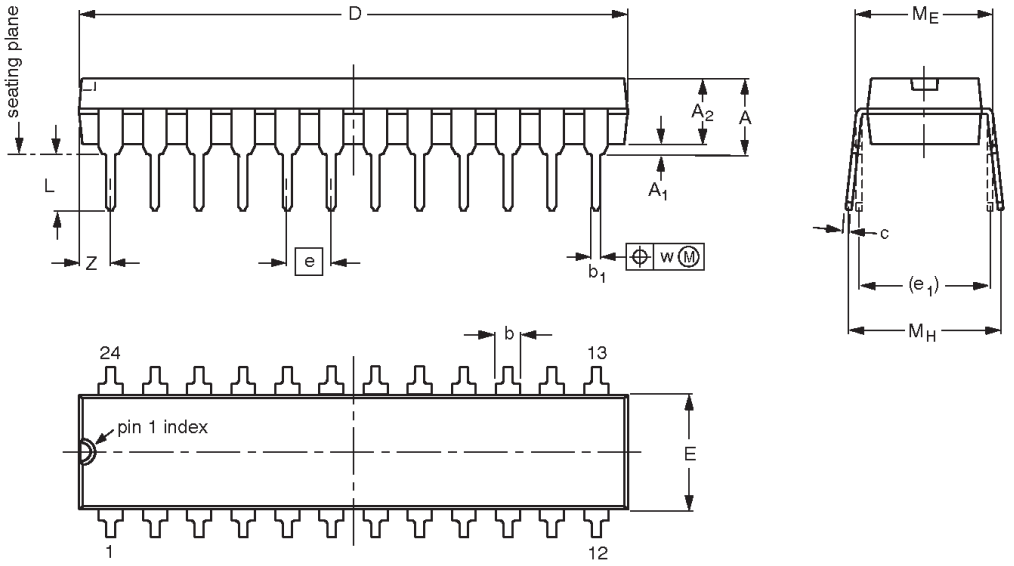
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

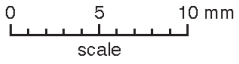
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

DIP24: plastic dual in-line package; 24 leads (300 mil) **SOT222-1**





DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

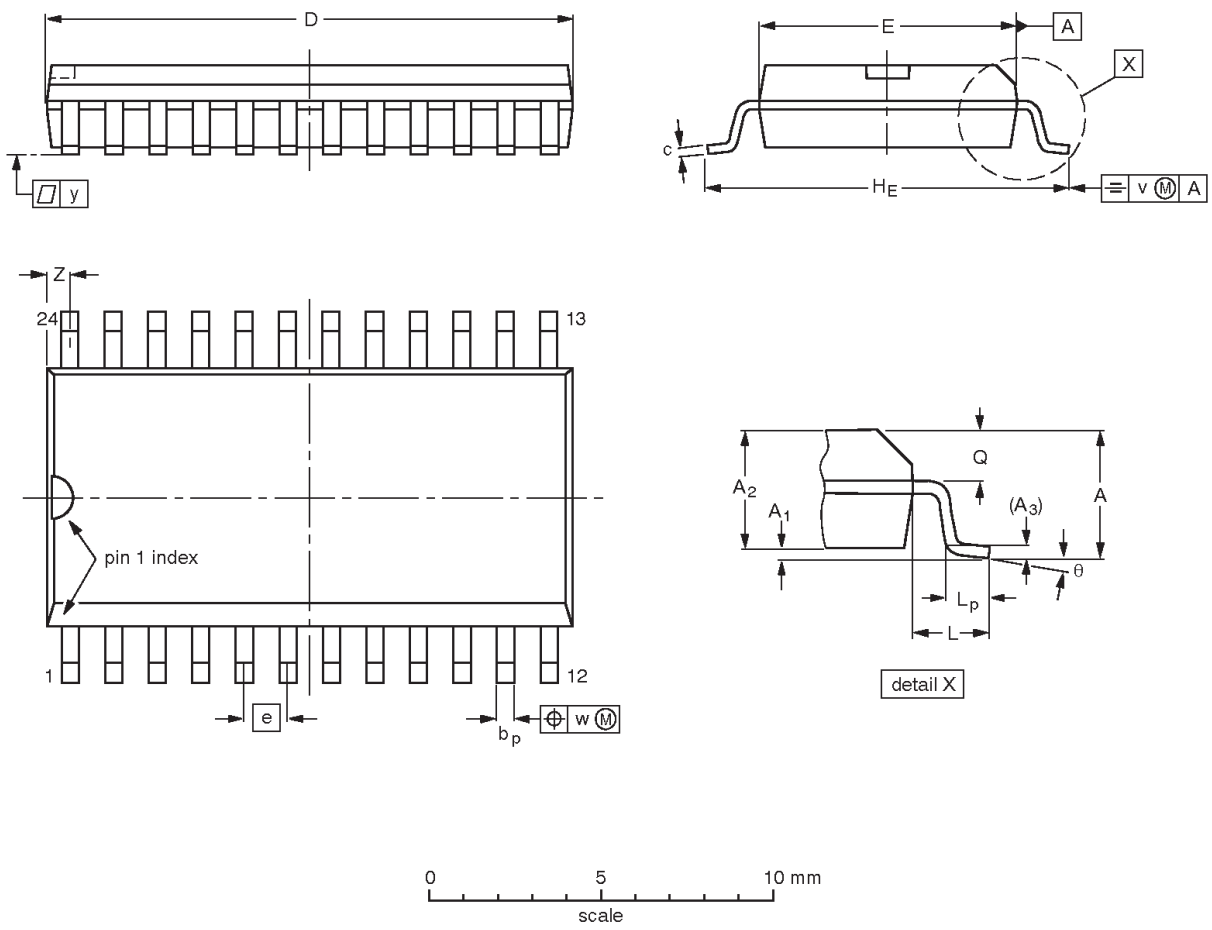
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

SO24: plastic small outline package; 24 leads; body width 7.5 mm SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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