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National Semiconductor

LMC662AM/LMC662AI/LMC662C CMOS Dual Operational Amplifier

General Description

The LMC662 CMOS Dual operational amplifier is ideal for operation from a single supply. It is fully specified for operation from +5V to +15V and features rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS}, drift, and broadband noise as well as voltage gain into realistic loads (2 kΩ and 600Ω) are all equal to or better than widely accepted bipolar equivalents.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC660 datasheet for a Quad CMOS operational amplifier with these same features.

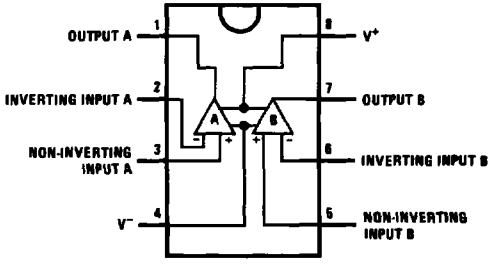
Features

- Rail-to-rail output swing
- Specified for 2 kΩ and 600Ω loads
- High voltage gain 126 dB
- Low input offset voltage 3 mV max
- Low offset voltage drift 1.3 μV/°C
- Ultra low input bias current 40 fA
- Input common-mode includes GND
- Operation guaranteed from +5V to +15V
- I_{SS} = 400 μA/amplifier; independent of V^+
- Low distortion 0.01% at 10 kHz
- Slew rate 1.1 V/μs
- Insensitive to latch-up
- Symmetrical gain when sourcing and sinking current

Applications

- High-impedance buffer
- Precision current-to-voltage converter
- Long-term integrator
- High-impedance preamplifier
- Active filter
- Sample-and-hold circuit
- Peak detector

Connection Diagram



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Ordering Information

Package	Temperature Range			NSC Drawing
	Military	Industrial	Commercial	
8-Pin Cavity DIP	LMC662AMD	LMC662AID		D08C
8-Pin Small Outline		LMC662AIM	LMC662CM	M08A
8-Pin Molded DIP		LMC662AIN	LMC662CN	N08E

3

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Either Input beyond V^+ or V^-	0.7V
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to GND (Note 1)	Continuous
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature (Note 2)	150°C
ESD Tolerance (Note 10)	500V

Operating Conditions

Temperature Range	
LMC662AM	$-55°C \le T_J \le +125°C$
LMC662AI	$-40°C \le T_J \le +85°C$
LMC662C	$0°C \le T_J \le +70°C$
Supply Voltage Range	4.75V to 15.5V

DC Electrical Characteristics

unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L > 1M$ unless otherwise specified.

Parameter	Conditions	Typ	LMC662AM		LMC662AI		LMC662C		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Input Offset Voltage		1	3		3	**3.3**	6	**6.3**	mV max
			3.5						
Input Offset Voltage Average Drift		1.3							µV/°C
Input Bias Current	(Note 9)	0.04	20		20	**4**		**2**	pA max
			100						
Input Offset Current	(Note 9)	0.01	20		20	**2**		**1**	pA max
			100						
Input Resistance		>1							Teraω
Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$	83	70		70	**68**	63	**62**	dB min
			68						
Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$	83	70		70	**68**	63	**62**	dB min
			68						
Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	84		84	**83**	74	**73**	dB min
			82						
Input Common-Mode Voltage Range	$V^+ = 5V$ & 15V For CMRR ≥ 50 dB	−0.4	−0.1		−0.1	**0**	−0.1	**0**	V max
			0						
		$V^+ - 1.9$	$V^+ - 2.3$		$V^+ - 2.3$	$\mathbf{V^+ - 2.5}$	$V^+ - 2.3$	$\mathbf{V^+ - 2.4}$	V min
			$\mathbf{V^+ - 2.6}$						
Large Signal Voltage Gain	$R_L = 2k\Omega$ (Note 6)								
	Sourcing	2000	400		400	**440**	200	**300**	V/mV min
			300						
	Sinking	500	180		180	**120**	90	**80**	V/mV min
			70						
	$R_L = 600\Omega$ (Note 6)								
	Sourcing	1000	200		200	**220**	100	**150**	V/mV min
			150						
	Sinking	250	100		100	**60**	50	**40**	V/mV min
			35						

DC Electrical Characteristics (Continued)

unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L > 1M$ unless otherwise specified.

Parameter	Conditions	Typ	LMC662AM		LMC662AI		LMC662C		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Output Swing	$V^+ = 5V$ $R_L = 2k\Omega$ to $V^+/2$	4.87	4.82		4.82	**4.79**	4.78	**4.76**	V min
			4.77						
		0.10	0.15		0.15	**0.17**	0.19	**0.21**	V max
			0.19						
	$V^+ = 5V$ $R_L = 600\Omega$ to $V^+/2$	4.61	4.41		4.41	**4.31**	4.27	**4.21**	V min
			4.24						
		0.30	0.50		0.50	**0.56**	0.63	**0.69**	V max
			0.63						
	$V^+ = 15V$ $R_L = 2k\Omega$ to $V^+/2$	14.63	14.50		14.50	**14.44**	14.37	**14.32**	V min
			14.40						
		0.26	0.35		0.35	**0.40**	0.44	**0.48**	V max
			0.43						
	$V^+ = 15V$ $R_L = 600\Omega$ to $V^+/2$	13.90	13.35		13.35	**13.15**	12.92	**12.76**	V min
			13.02						
		0.79	1.16		1.16	**1.32**	1.45	**1.58**	V max
			1.42						
Output Current $V^+ = 5V$	Sourcing, $V_O = 0V$	22	16		16	**14**	13	**11**	mA min
			12						
	Sinking, $V_O = 5V$	21	16		16	**14**	13	**11**	mA min
			12						
Output Current $V^+ = 15V$	Sourcing, $V_O = 0V$	40	19		28	**25**	23	**21**	mA min
			19						
	Sinking, $V_O = 13V$	39	19		28	**24**	23	**20**	mA min
			19						
Supply Current	Both Amplifiers $V_O = 1.5V$	0.75	1.3		1.3	**1.5**	1.6	**1.8**	mA max
			1.8						

AC Electrical Characteristics

unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L > 1M$ unless otherwise specified.

Parameter	Conditions	Typ	LMC662AM		LMC662AI		LMC662C		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Slew Rate	(Note 7)	1.1	0.8		0.8	**0.6**	0.8	**0.7**	V/μs min
			0.5						
Gain-Bandwidth Product		1.4							MHz
Phase Margin		50							Deg
Gain Margin		17							dB
Amp-to-Amp Isolation	(Note 8)	130							dB
Input Referred Voltage Noise	F = 1 kHz	22							$nV/\sqrt{Hz}$
Input Referred Current Noise	F = 1 kHz	0.0002							$pA/\sqrt{Hz}$
Total Harmonic Distortion	F = 10 kHz, $A_V = -10$ $R_L = 2\,k\Omega$, $V_O = 8\,V_{PP}$	0.01							%

Note 1: Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C.

Note 2: The junction-to-ambient thermal resistance of the molded plastic DIP (N) is 101°C/W, the molded plastic SO (M) package is 152°C/W, and the cavity DIP (D) package is 124°C/W. All numbers apply for packages soldered directly into a PC board.

Note 3: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 4: These limits are guaranteed and are used in calculating outgoing AQL.

Note 5: These limits are guaranteed, but are not used in calculating outgoing AQL.

Note 6: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.

Note 7: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

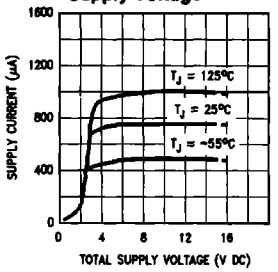
Note 8: Input referred. $V^+ = 15V$ and $R_L = 10\,k\Omega$ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce $V_O = 13\,V_{PP}$.

Note 9: The specifications in the Design Limit column reflect the true performance of the part, while those in the Tested Limit column are degraded to allow for the unavoidable inaccuracies involved in cost-effective high-speed automatic testing.

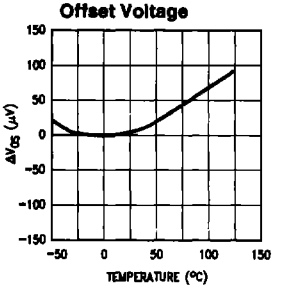
Note 10: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified

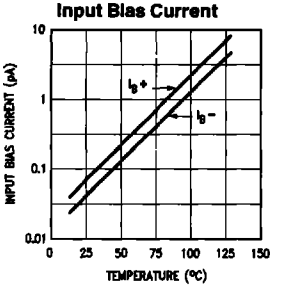
Supply Current vs Supply Voltage



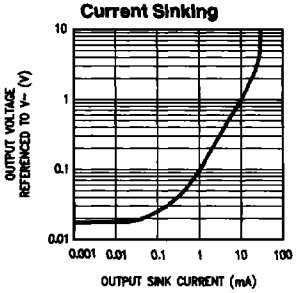
Offset Voltage



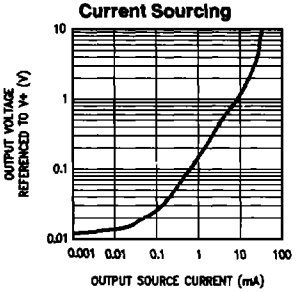
Input Bias Current



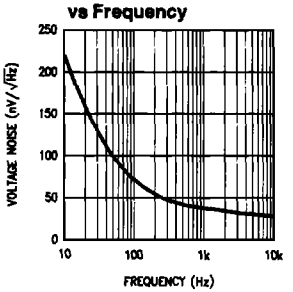
Output Characteristics Current Sinking



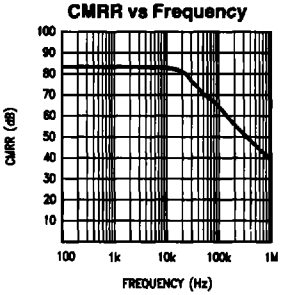
Output Characteristics Current Sourcing



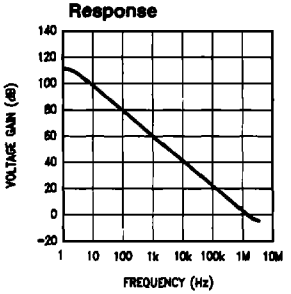
Input Voltage Noise vs Frequency



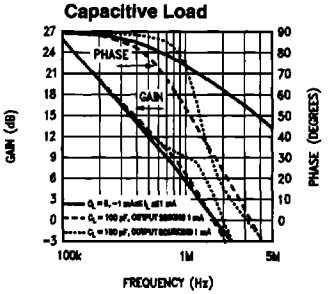
CMRR vs Frequency



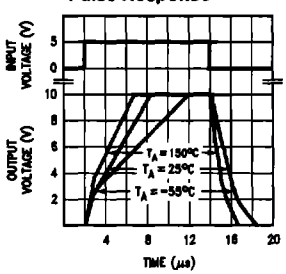
Open-Loop Frequency Response



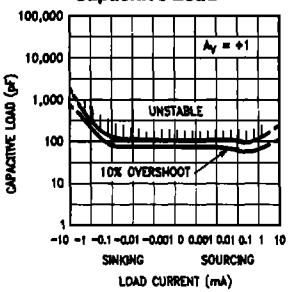
Frequency Response vs Capacitive Load



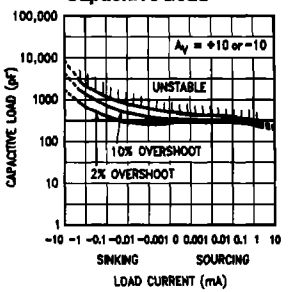
Non-Inverting Large Signal Pulse Response



Stability vs Capacitive Load



Stability vs Capacitive Load



TL/H/9763–3

Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

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3

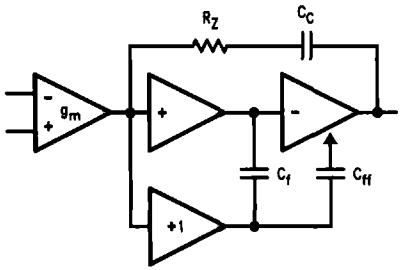
Application Hints

AMPLIFIER TOPOLOGY

The topology chosen for the LMC662 is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.

LMC662 Circuit Topology (Each Amplifier)



TL/H/9763–4

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, even with a 600Ω load. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, under heavy load (600Ω) the gain will be reduced as indicated in the Electrical Characteristics.

COMPENSATING INPUT CAPACITANCE

The high input resistance of the LMC662 op amps allows the use of large feedback and source resistor values without losing gain accuracy due to loading. However, the circuit will be especially sensitive to its layout when these large-value resistors are used.

Every amplifier has some capacitance between each input and AC ground, and also some differential capacitance between the inputs. When the feedback network around an amplifier is resistive, this input capacitance (along with any additional capacitance due to circuit board traces, the socket, etc.) and the feedback resistors create a pole in the feedback path. In the following General Operational Amplifier Circuit, the frequency of this pole is

$$f_p = \frac{1}{2\pi C_S R_P}$$

where C_S is the total capacitance at the inverting input, including amplifier input capacitance and any stray capacitance from the IC socket (if one is used), circuit board traces, etc., and R_P is the parallel combination of R_F and R_{IN}. This formula, as well as all formulae derived below, apply to inverting and non-inverting op-amp configurations.

When the feedback resistors are smaller than a few kΩ, the frequency of the feedback pole will be quite high, since C_S is generally less than 10 pF. If the frequency of the feedback pole is much higher than the "ideal" closed-loop bandwidth (the nominal closed-loop bandwidth in the absence of C_S), the pole will have a negligible effect on stability, as it will add only a small amount of phase shift.

However, if the feedback pole is less than approximately 6 to 10 times the "ideal" −3 dB frequency, a feedback capacitor, C_F, should be connected between the output and the inverting input of the op amp. This condition can also be stated in terms of the amplifier's low-frequency noise gain: To maintain stability, a feedback capacitor will probably be needed if

$$\left(\frac{R_F}{R_{IN}} + 1\right) \leq \sqrt{6 \times 2\pi \times GBW \times R_F \times C_S}$$

where

$$\left(\frac{R_F}{R_{IN}} + 1\right)$$

is the amplifier's low-frequency noise gain and GBW is the amplifier's gain bandwidth product. An amplifier's low-frequency noise gain is represented by the formula

$$\left(\frac{R_F}{R_{IN}} + 1\right)$$

regardless of whether the amplifier is being used in an inverting or non-inverting mode. Note that a feedback capacitor is more likely to be needed when the noise gain is low and/or the feedback resistor is large.

If the above condition is met (indicating a feedback capacitor will probably be needed), and the noise gain is large enough that:

$$\left(\frac{R_F}{R_{IN}} + 1\right) \geq 2\sqrt{GBW \times R_F \times C_S},$$

the following value of feedback capacitor is recommended:

$$C_F = \frac{C_S}{2\left(\frac{R_F}{R_{IN}} + 1\right)}$$

If

$$\left(\frac{R_F}{R_{IN}} + 1\right) < 2\sqrt{GBW \times R_F \times C_S},$$

the feedback capacitor should be:

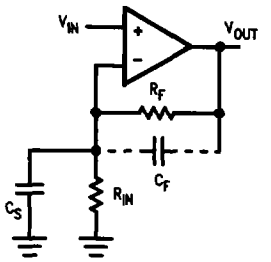
$$C_F = \sqrt{\frac{C_S}{GBW \times R_F}}$$

Note that these capacitor values are usually significantly smaller than those given by the older, more conservative formula:

$$C_F = \frac{C_S R_{IN}}{R_F}.$$

Application Hints (Continued)

General Operational Amplifier Circuit



TL/H/9763–6

C_S consists of the amplifier's input capacitance plus any stray capacitance from the circuit board and socket. C_F compensates for the pole caused by C_S and the feedback resistor.

Using the smaller capacitors will give much higher bandwidth with little degradation of transient response. It may be necessary in any of the above cases to use a somewhat larger feedback capacitor to allow for unexpected stray capacitance, or to tolerate additional phase shifts in the loop, or excessive capacitive load, or to decrease the noise or bandwidth, or simply because the particular circuit implementation needs more feedback capacitance to be sufficiently stable. For example, a printed circuit board's stray capacitance may be larger or smaller than the breadboard's, so the actual optimum value for C_F may be different from the one estimated using the breadboard. In most cases, the value of C_F should be checked on the actual circuit, starting with the computed value.

INPUT OVERDRIVE

Input overdrive protection has been built into the LMC662, so that no latching, "output phase changes", or activation of parasitic junctions occurs when the inputs are taken outside the power supply rails. In addition, this protection inhibits ESD damage whether or not the device is powered up, and even if the power supply pins are floating. The protection consists of 200Ω series input resistors and diodes connected from each input to each power supply rail.

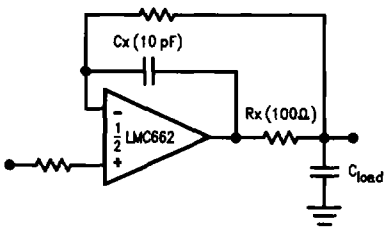
If the input to the LMC662 is set above the LMC662's input common-mode range, the LMC662's output will go to the positive supply rail. This output will stay at the positive supply rail until the input voltage is dropped back into the input common-mode range.

CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LMC662 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. The addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.

Rx, Cx Improve Capacitive Load Tolerance



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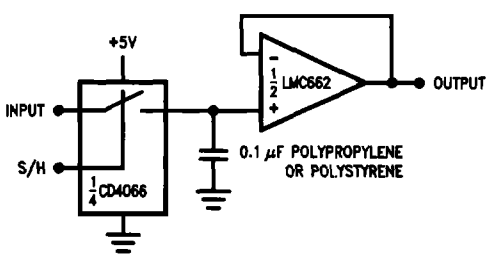
Typical Single-Supply Applications

(V^+ = 5.0 V_{DC})

Additional single-supply applications ideas can be found in the LM358 datasheet. The LMC662 is pin-for-pin compatible with the LM358 and offers greater bandwidth and input resistance over the LM358. These features will improve the performance of many existing single-supply applications. Note, however, that the supply voltage range of the LM662 is smaller than that of the LM358.

Low-Leakage Sample-and-Hold



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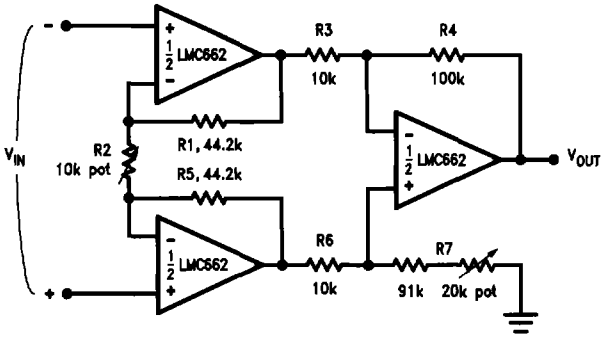
Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

Instrumentation Amplifier



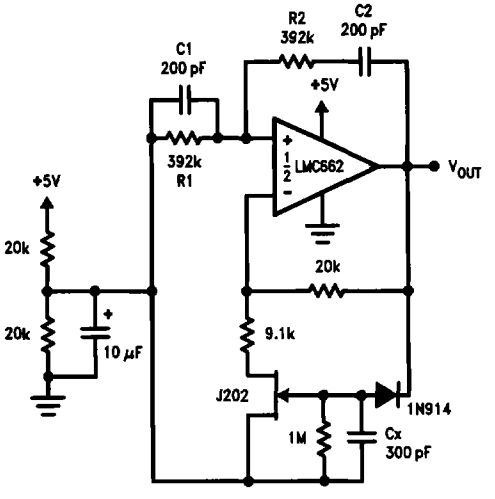
TL/H/9763–7

$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3}$$ if R1 = R5; R3 = R6, and R4 = R7.

= 100 for circuit shown.

All resistors should be at least 1% tolerance. Matching of R1 to R5, R3 to R6, and R4 to R7 affects CMRR. Gain may be adjusted through R2. CMRR may be adjusted through R7.

Sine-Wave Oscillator



TL/H/9763–8

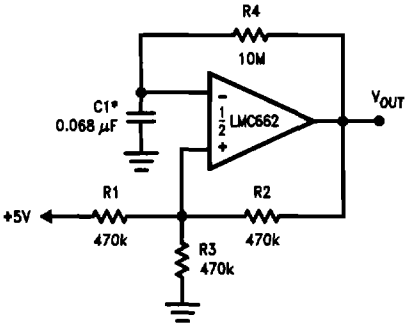
Oscillator frequency is determined by R1, R2, C1, and C2:

$$f_{OSC} = 1/2\pi RC$$

where R = R1 = R2 and C = C1 = C2.

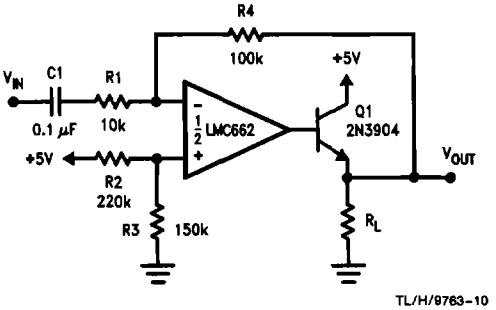
This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.5V

1 Hz Square-Wave Oscillator



TL/H/9763–9

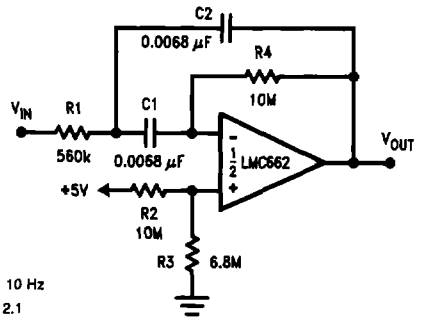
Power Amplifier



TL/H/9763–10

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

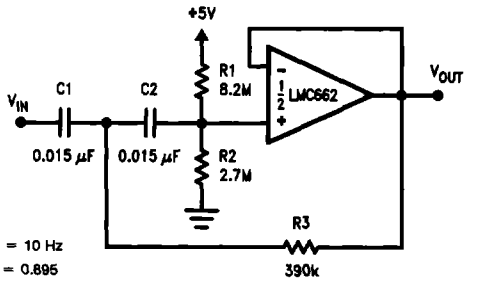
10 Hz Bandpass Filter



f_O = 10 Hz
Q = 2.1
Gain = −6.8

TL/H/9763–11

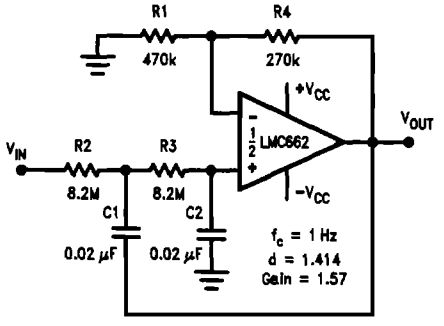
10 Hz High-Pass Filter (2 dB Dip)



f_c = 10 Hz
d = 0.895
Gain = 1

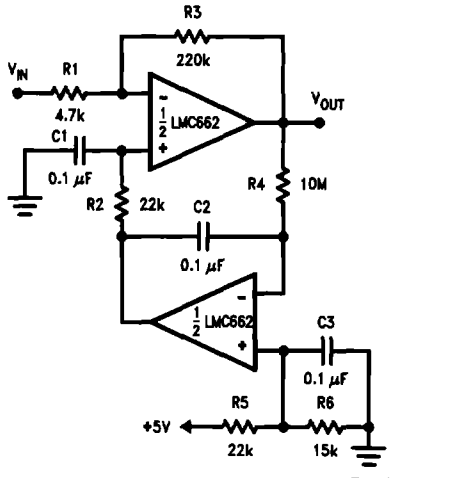
TL/H/9763–12

1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)



TL/H/9763–13

High Gain Amplifier with Offset Voltage Reduction



TL/H/9763–14

Gain = −46.8

Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV).

3