PRELIMINARY DATA SHEET

GD74F257

QUAD 2-INPUT MULTIPLEXER WITH TRI-STATE OUTPUTS

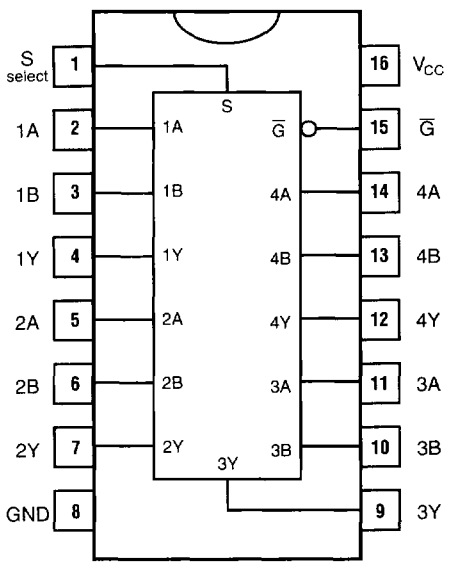
Features

- 3-State outputs interface directly with system bus
- Non-inverting 3-State outputs

Description

The GD74F257 is a quad 2-input multiplexer with TRI-STATE outputs. Four bits of data from two sources can be selected using a Common Data Selected input. The four outputs present the selected data in true (non-inverted) form. The outputs may be switched to a high impedance state with a High on the common Output Control ($\overline{G}$) input, allowing the outputs to interface directly with bus-oriented systems.

Pin Configuration



Package Type: 16 DIP, 16 SOP Available

Function Table

Input				Output
$\overline{G}$	S	A	B	Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

S: Common Data Input
$\overline{G}$: Tri-State Output Enable Input (Active Low)
nA, nB: Data Inputs
nY: Output
X: Immaterial

Recommended Operating Conditions

- Free Air Ambient Temperature ..... 0°C to 70°C
- Supply Voltage ..... 4.5 V to 5.5 V

Absolute Maximum Ratings

- Storage Temperature ..... −65°C to 150°C
- Ambient Temperature Under Bias ..... −55°C to 125°C
- Junction Temperature Under Bias ..... −0.5°C to 175°C
- V_{CC} Voltage ..... −0.5 V to 7.0 V
- Input Voltage ..... −5.0 V to 7.0 V
- Input Current ..... −30 mA to 5.0 mA
- Output Voltage ..... −0.5 V to 5.5 V

Note: Absolute Maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

AC Characteristics

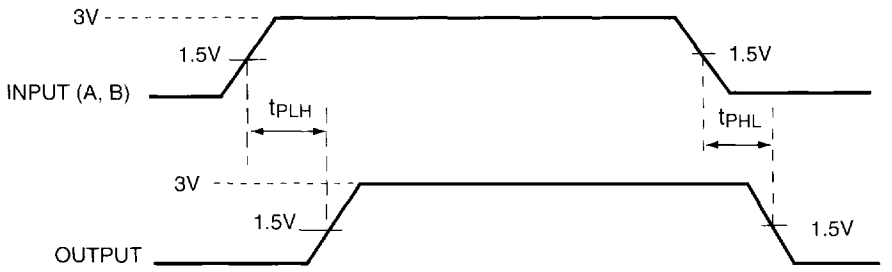
SYMBOL	PARAMETER	TEST CONDITIONS						UNIT
		TA = 25°C, V_{CC} = 5.0 V, C_L = 50 pF			TA = 0°C to 70°C, V_{CC} = 5 V ±10%, C_L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} t_{PHL}	Propagation Delay A, B to Y	2.5 2.0	4.5 4.2	5.5 5.5	2.0 2.0	— —	6.0 6.0	ns
t_{PLH} t_{PHL}	Propagation Delay S to Y	4.0 2.5	5.0 6.5	9.5 7.0	3.5 2.5	— —	10.5 8.0	ns
t_{PZH} t_{PZL}	Output Enable Time	2.0 2.5	5.9 5.5	6.0 7.0	2.0 2.5	— —	7.0 8.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 2.0	4.3 4.5	6.0 6.0	2.0 2.0	— —	7.0 7.0	ns

DC Electrical Characteristics over recommended operating free-air temperature range

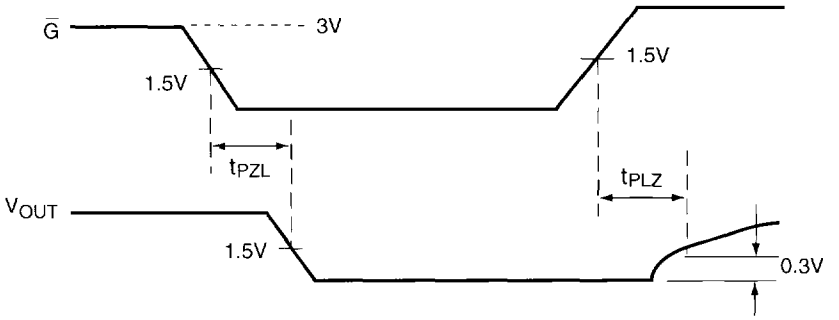
SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT	V_{CC}	Test Circuit
V_{IH}	Input High Voltage	———	2.0			V		
V_{IL}	Input Low Voltage	———			0.8	V		
V_{CD}	Input Clamp Diode Voltage	I_{IN} = −18 mA			−1.2	V	Min	Fig. 1
V_{OH}	Output High Voltage	I_{OH} = −1 mA I_{OH} = −3 mA I_{OH} = −1 mA I_{OH} = −3 mA	2.5 2.4 2.7 2.7			V	4.5 4.5 4.75 4.75	Fig. 2
V_{OL}	Output Low Voltage	I_{OL} = 24 mA			0.5	V	Min	
I_I	Input High Current Breakdown Test	V_{IN} = 7.0 V			7.0	µA	Max	
I_{IH}	Input High Current	V_{IN} = 2.7 V			5.0	µA	Max	Fig. 3
I_{IL}	Input Low Current	V_{IN} = 0.5 V Measure A port when S is low			−0.6	mA	Max	
I_{ILK}	Input Leakage Circuit Current	V_{IN} = 4.75 V All other pins grounded			1.9	µA	0.0	Fig. 4
I_{OLK}	Output Leakage Circuit Current	V_{OUT} = 150 mA All other pins grounded			3.75	µA	0.0	
I_{OZH}	Tri-State Output Off Current (High)	V_{OUT} = 2.7 V			50	µA	Max	
I_{OZL}	Tri-State Output Off Current (Low)	V_{OUT} = 0.5 V			−50	µA	Max	Fig. 5
I_{OS}	Output Short Circuit Current	V_{OUT} = 0 V	−60		−150	mA	Max	Fig. 6
I_{CCH} I_{CCL} I_{CCZ}	Supply Current	V_{OUT} = High V_{OUT} = Low V_{OUT} = High Z		9.0 14.5 15	15 22 23	mA	Max	Fig. 7

For I_{OS}, not more than one output should be shorted at a time, and duration should not exceed one second.

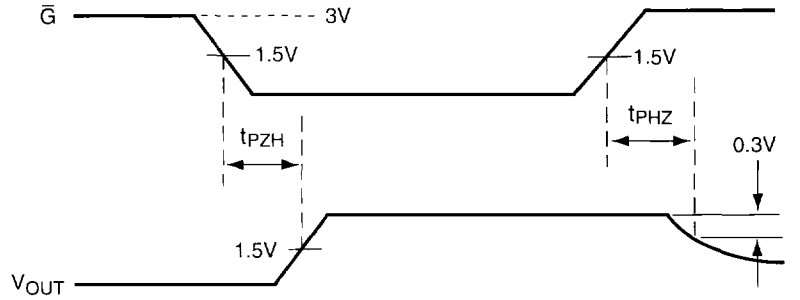
Waveform of Functions



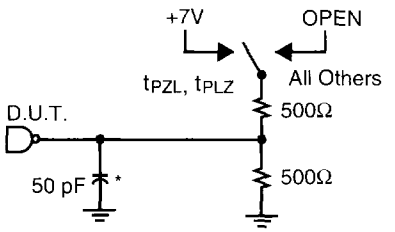
3-State Output Low Enable and Disable Times



3-State Output High Enable and Disable Times



AC Test Circuit



* Include Jig and Probe Capacitance

Input Condition

Frequency	:	1.0 MHZ
Duty Cycle	:	50%
Rising Time	:	2.5 ns
Falling Time	:	2.5 ns
Amplitude	:	0 to 3V

DC Test Circuit

FIG. 1 V_{CD} Test
(force I_{IN} and measure V_{CD})

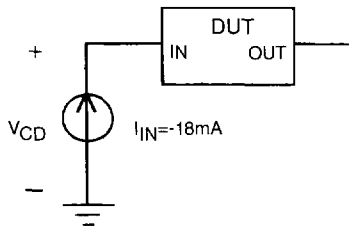


FIG. 2 V_{OH} & V_{OL} Test
(force I_O and measure V_{OH} or V_{OL})

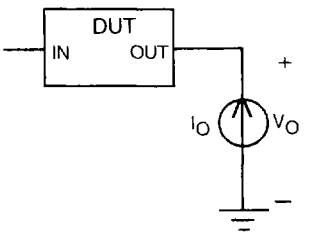


FIG. 3 I_I, I_{IH} & I_{IL} Test
(force V_{IN} and measure I_I, I_{IH} or I_{IL})

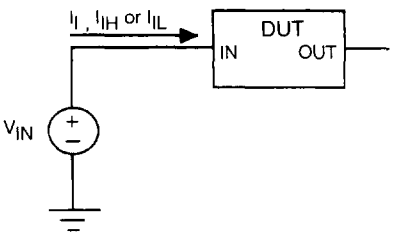


FIG. 5 I_{OZH} & I_{OZL} Test

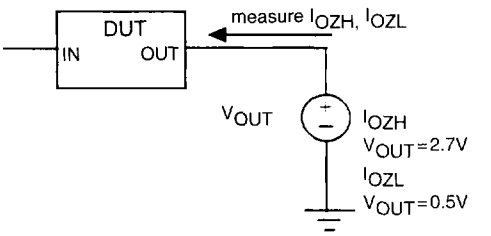
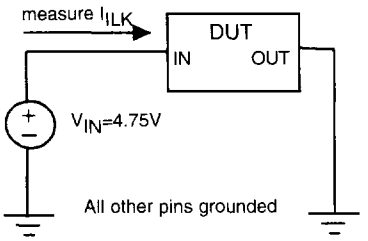


FIG. 4 I_{ILK} Test & I_{OLK} Test



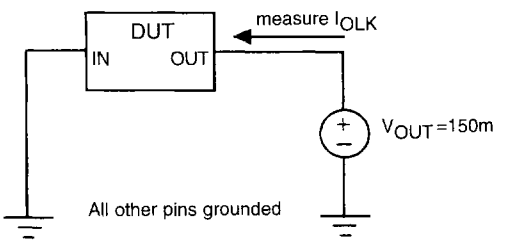


FIG. 6 I_{OS} Test

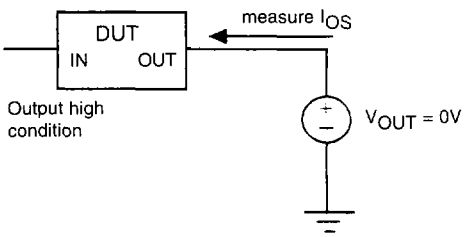


FIG. 7 I_{CC} Test