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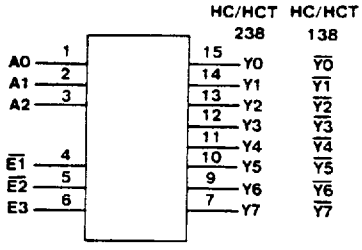
CD54/74HC138, CD54/74HCT138
CD54/74HC238, CD54/74HCT238

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

3-to-8 Line Decoder/Demultiplexer Inverting and Non-Inverting

Type Features:

- *Select one of eight data output [active LOW for 138, active HIGH for 238]*
- *I/O port or memory selector*
- *3 Enable Inputs to simplify cascading*
- *Typical propagation delay of 13ns @ V_{CC} = 5 V, C_L = 15 pF, T_A = +25° C*

The Harris CD54/74HC138,238 and CD54/74HCT138,238 are high speed silicon gate CMOS decoders well suited to memory address decoding or data routing applications. Both circuits feature low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL logic. Both circuits have 3 binary select inputs (A_0, A_1, and A_2). If the device is enabled these inputs determine which one of the eight normally high outputs of the HC/HCT138 series will go low or which of the normally low outputs of the HC/HCT238 series will go high.

Two active low and one active high enables ($\overline{E}_1$, $\overline{E}_2$, and E_3) are provided to ease the cascading of decoders. The decoder's outputs can drive 10 low power Schottky TTL equivalent loads.

The CD54HC138, CD54HC238 and CD54HCT138, CD54HCT238 are supplied in 16-lead hermetic dual-in-line ceramic package (F suffix). The CD54HC138, CD54HC238 and CD74HCT138, CD54HCT238 are supplied in 16-lead dual-in-line plastic package (E suffix) and in 16-lead dual-in-line surface mount plastic package (M suffix) and 16 lead dual-in-line shrink small outline plastic package (SM suffix). All types are also available in chip form (H suffix).

Family Features:

- *Fanout [Over Temperature Range]:*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  -55 to +125°C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

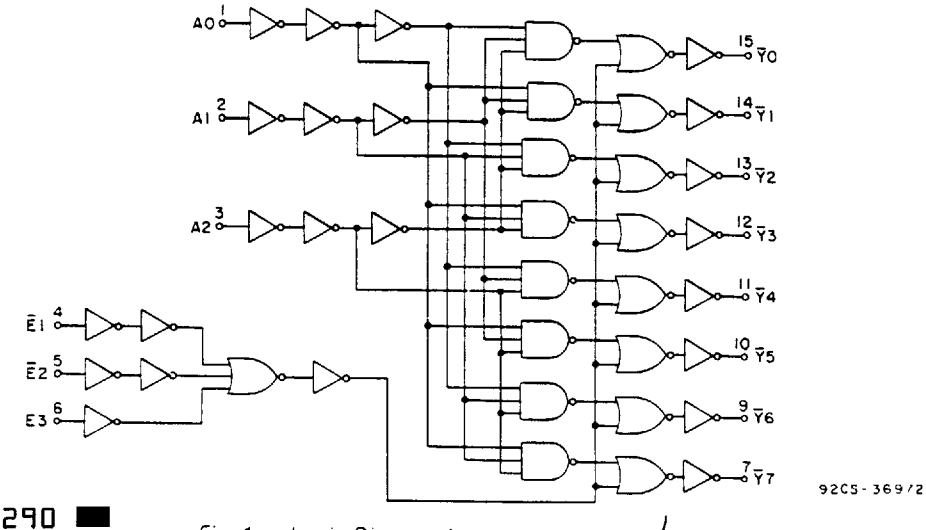


Fig. 1 — Logic Diagram for HC/HCT 138

CD54/74HC138, CD54/74HCT138
CD54/74HC238, CD54/74HCT238

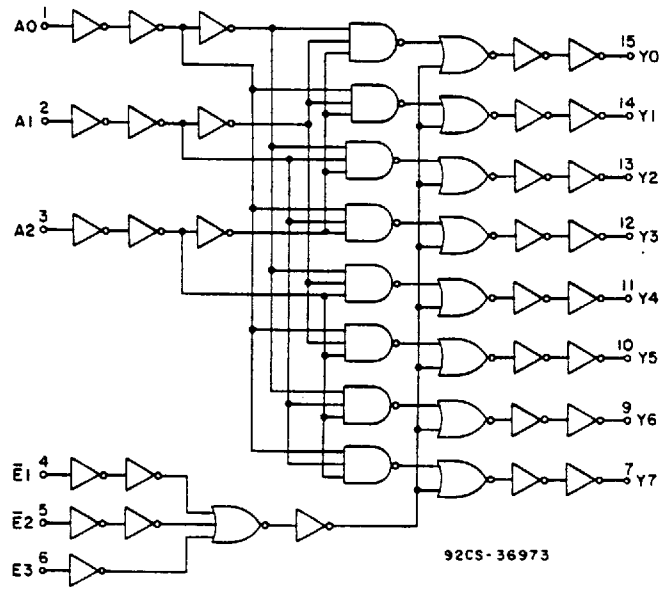


Fig. 2 — Logic Diagram for HC/HCT 238

TRUTH TABLE
CD54/74HC138, CD54/74HCT138

INPUTS						OUTPUTS							
ENABLE			ADDRESS										
E3	$\overline{E2}$	$\overline{E1}$	A2	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = High level, L = low level, X = don't care

TRUTH TABLE
CD54/74HC238, CD54/74HCT238

INPUTS						OUTPUTS							
ENABLE			ADDRESS										
E3	$\overline{E2}$	$\overline{E1}$	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	L	H	L	L	L	H	L	L	L	L	L
H	L	L	L	H	H	L	L	L	H	L	L	L	L
H	L	L	H	L	L	L	L	L	L	H	L	L	L
H	L	L	H	L	H	L	L	L	L	L	H	L	L
H	L	L	H	H	L	L	L	L	L	L	L	H	L
H	L	L	H	H	H	L	L	L	L	L	L	L	H

H = High level, L = low level, X = don't care

CD54/74HC138, CD54/74HCT138
CD54/74HC238, CD54/74HCT238

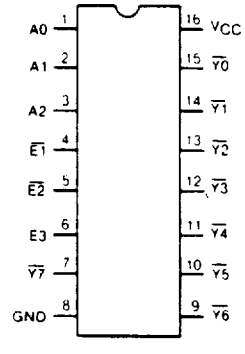
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5V) ..... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5V) ..... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR $-0.5\ V < V_o < V_{CC} + 0.5V$) ..... ±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) ..... ±50mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E, F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E, F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_{in}, V_{out}	0	V_{CC}	V
Operating Temperature T_A	−55	+125	°C
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.



92CS 36809

TERMINAL ASSIGNMENT FOR HC/HCT138
FOR HC/HCT238 ALL $\overline{Y}$'s ARE Y's

CD54/74HC138, CD54/74HCT138
CD54/74HC238, CD54/74HCT238

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC138/238, CD54HC138/238										CD74HCT138/238, CD54HCT138/238									UNITS
	TEST CONDITIONS			AMBIENT TEMPERATURE (T_A)							TEST CONDITIONS		AMBIENT TEMPERATURE (T_A)							
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C		
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
A0-A2	1.5
$\overline{E1}$, $\overline{E2}$	1.25
E3	1

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC138, CD54/74HCT138
CD54/74HC238, CD54/74HCT238

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	Typical		
		HC	HCT	Unit
Propagation Delay, Address to Output Y (C_L=15 pF) (Fig. 3)	t_{PLH} t_{PHL}	13	14	ns
Power Dissipation Capacitance*	*C_{PD}	67	67	pF

*C_{PD} is used to determine the dymanic power consumption, per package.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r,t_f = 6 ns)

CHARACTERISTIC		TEST CONDITIONS V_{CC} (V)	AMBIENT TEMPERATURE (T_A) +25°C HC Min.	HC Max.	HCT Min.	HCT Max.	-40°C to +85°C HC Min.	HC Max.	HCT Min.	HCT Max.	-55°C to +125°C HC Min.	HC Max.	HCT Min.	HCT Max.	UNITS
Propagation Delay Address to Output (Fig. 3)	t_{PLH} t_{PHL}	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
		4.5	—	30	—	35	—	38	—	44	—	45	—	53	
		6	—	26	—	—	—	33	—	—	—	38	—	—	
Propagation Delay, Enable to Output (Fig. 3) HC/HCT138	t_{PLH} t_{PHL}	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
		4.5	—	30	—	35	—	38	—	44	—	45	—	53	
		6	—	26	—	—	—	33	—	—	—	38	—	—	
Propagation Delay Enable to Output (Fig. 4) HC/HCT238	t_{PLH} t_{PHL}	2	—	175	—	—	—	220	—	—	—	265	—	—	ns
		4.5	—	35	—	40	—	44	—	50	—	53	—	60	
		6	—	30	—	—	—	37	—	—	—	45	—	—	
Output Transition Times	t_{TLH} t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF

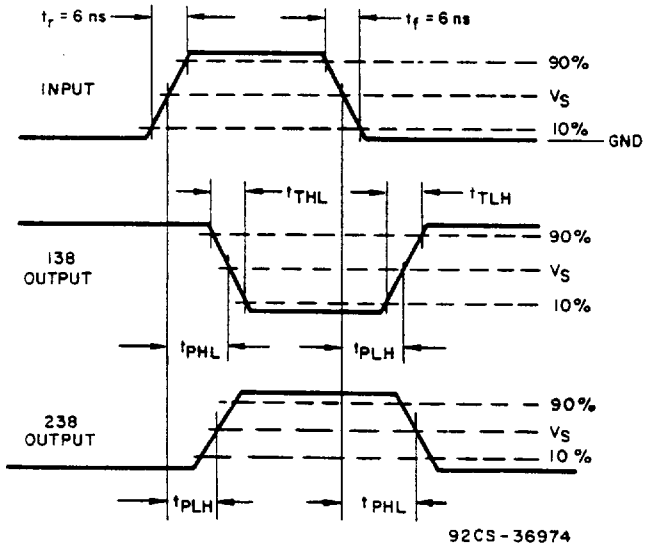


Fig. 3 — Transition times and propagation delay times.

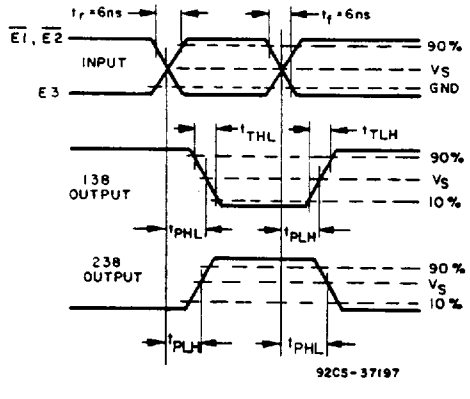


Fig. 4 — Transition times and propagation delay times.

	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3V
V_S	50% V_{CC}	1.3V

	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3V
V_S	50% V_{CC}	1.3V