Hybrid Systems CORPORATION

HS 7528

Dual 8-Bit Buffered MDAC

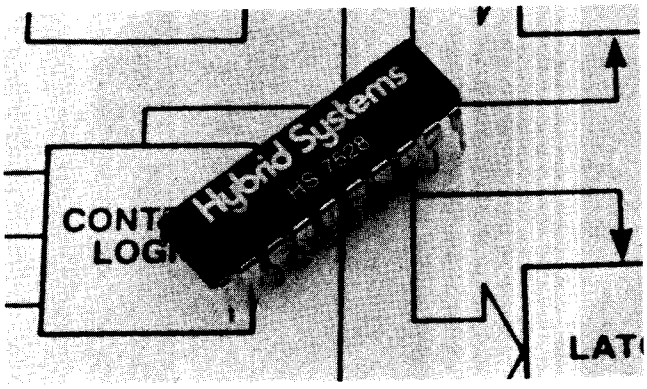
DESCRIPTION

The HS 7528 is a monolithic dual 8-Bit digital/analog converter produced in a small 0.3" wide 20-pin DIP, featuring excellent DAC-to-DAC matching.

Separate on-chip latches are provided for each DAC to allow easy microprocessor interface.

Data is transferred into either of the two DAC data latches via a common 8-Bit TTL/CMOS compatible input port. Control input $\overline{\text{DAC A}}$/DAC B determines which DAC is to be loaded. The HS 7528's load cycle is similar to the write cycle of a random access memory and the device is bus compatible with most 8-Bit microprocessors, including 6800, 8080, 8085, Z80.

The device operates from a +5V to +15V power supply, dissipating only 20 mW of power.



Both DACs offer excellent four quadrant multiplication characteristics with a separate reference input and feedback resistor for each DAC.

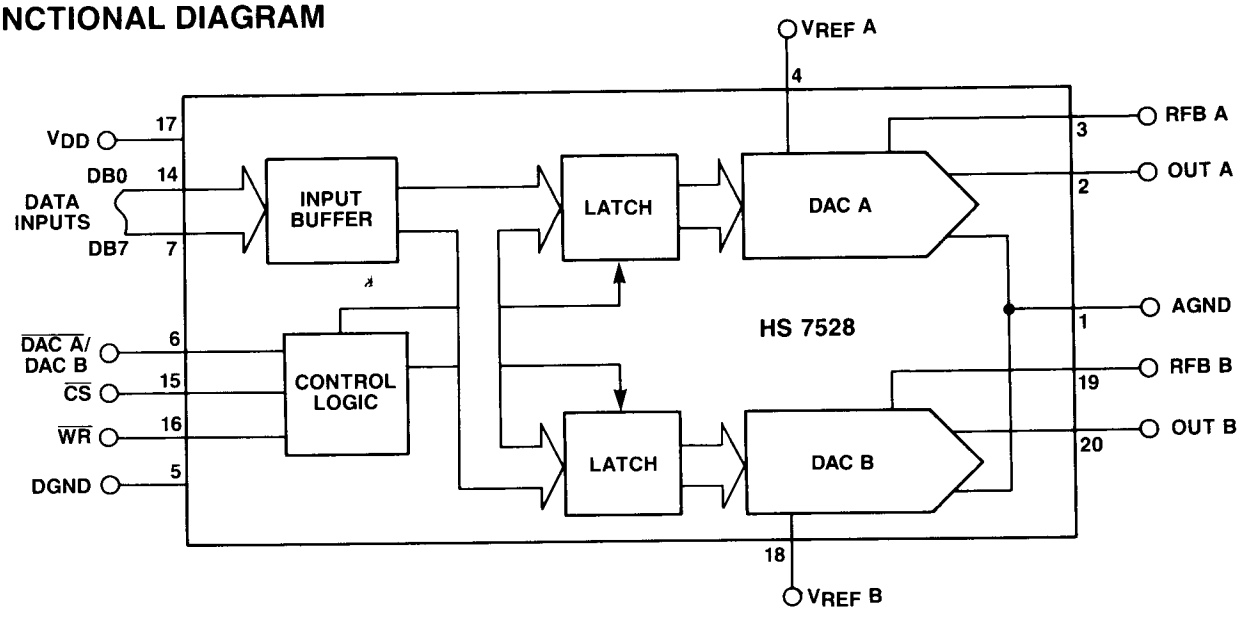
FEATURES

1. On-Chip Latches for Both DACs
2. Two 8-Bit DACs on a Single Chip
3. Low Power (20 mW)
4. MIL-STD-883 Processing Available

BENEFITS

1. Allows Direct Interface to 8-Bit Bus Structures Without External Latches
2. Precise Matching and Tracking Between DAC A and DAC B
3. Reduces System Level Power Requirements, Ideal for Battery Powered Applications
4. Suitable for Military and High Reliability Applications

FUNCTIONAL DIAGRAM



SPECIFICATIONS

(V_{REF} A = V_{REF} B = +10V; OUT A = OUT B = 0V unless otherwise specified)

Parameter	Version[1]	V_{DD} = +5V T_A = +25°C	V_{DD} = +5V T_{Min}, T_{Max}	V_{DD} = +15V T_A = +25°C	V_{DD} = +15V T_{Min}, T_{Max}	Units	Test Conditions/Comments
STATIC PERFORMANCE[2]							
Resolution	All	8	8	8	8	Bits	
Relative Accuracy	J,A,S	±1	±1	±1	±1	LSB max	This is an Endpoint Linearity Specification
	K,B,T	±½	±½	±½	±½	LSB max	
	L,C,U	±¼	±¼	±¼	±¼	LSB max	All Grades Guaranteed Monotonic Over Full Operating Temperature Range
Differential Nonlinearity	All	±½	±½	±½	±½	LSB max	
Gain Error	J,A,S	±4	±6	±4	±5	LSB max	Measured Using Internal RFB A and RFB B
	K,B,T	±2	±4	±2	±3	LSB max	Both DAC Latches Loaded with 11111111
	L,C,U	±1	±3	±1	±1	LSB max	Gain Error is Adjustable Using Circuits of Figures 4 and 5
Gain Temperature Coefficient ΔGain/ΔTemperature	All	±0.007	±0.007	±0.0035	±0.0035	%/%°C max	
Output Leakage Current							
OUT A (Pin 2)	All	±50	±400	±50	±200	nA max	DAC Latches Loaded with 00000000
OUT B (Pin 20)	All	±50	±400	±50	±200	nA max	
Input Resistance							
(V_{REF} A, V_{REF} B)	All	8	8	8	8	kΩmin	Input Resistance TC = −300ppm/°C typ
		15	15	15	15	kΩmax	Input Resistance is 11k
Input Resistance Match (V_{REF} A, V_{REF} B)	All	±1	±1	±1	±1	% max	
DIGITAL INPUTS[3]							
Input High Voltage V_{IH}	All	2.4	2.4	13.5	13.5	V min	
Input Low Voltage V_{IL}	All	0.8	0.8	1.5	1.5	V max	
Input Current I_{IN}	All	±1	±10	±1	±10	μA max	V_{IN} = 0 or V_{DD}
Input Capacitance							
DB0-DB7	All	10	10	10	10	pF max	
WR, CS, DAC A, DAC B	All	15	15	15	15	pF max	
SWITCHING CHARACTERISTICS[4]							See Timing Diagram
Chip Select to Write Set Up Time t_{CS}	All	200	230	60	80	ns min	
Chip Select to Write Hold Time t_{CH}	All	20	30	10	15	ns min	
DAC Select to Write Set Up Time t_{AS}	All	200	230	60	80	ns min	
DAC Select to Write Hold Time t_{AH}	All	20	30	10	15	ns min	
Data Valid to Write Set Up Time t_{DS}	All	110	130	30	40	ns min	
Data Valid to Write Hold Time t_{DH}	All	0	0	0	0	ns min	
Write Pulse Width t_{WR}	All	180	200	60	80	ns min	
POWER SUPPLY							See Figure 3
I_{DD}	All	1	1	1	1	mA max	All Digital Inputs V_{IL} or V_{IH}
		100	500	100	500	μA max	All Digital Inputs 0V or V_{DD}

AC PERFORMANCE CHARACTERISTICS

(V_{REF} A = V_{REF} B = +10V; OUT A = OUT B = 0V unless otherwise specified)

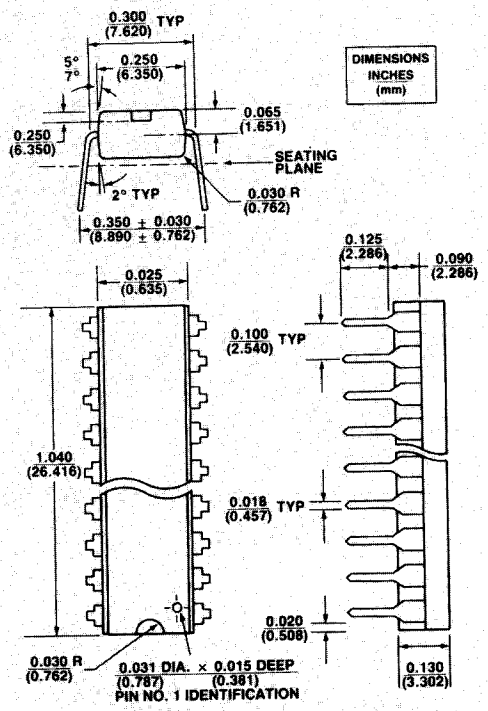
Parameter	Version[1]	V_{DD} = +5V T_A = +25°C	V_{DD} = +5V T_{Min}, T_{Max}	V_{DD} = +15V T_A = +25°C	V_{DD} = +15V T_{Min}, T_{Max}	Units	Test Conditions/Comments
DC SUPPLY REJECTION (ΔGAIN/ΔV_{DD})	All	0.02	0.04	0.01	0.02	%/% max	ΔV_{DD} = ±5%
PROPAGATION DELAY							V_{REF} A = V_{REF} B = +10V
(From Digital Input to 90% of Final Analog Output Current)	All	220	270	80	100	ns max	OUT A, OUT B Load = 100Ω C_{EXT} = 13pF $\overline{WR}$, $\overline{CS}$ = 0V DB0-DB7 = 0V to V_{DD} or V_{DD} to 0V
GLITCH ENERGY	All	160	—	440	—	nV sec typ	For code Transition 00000000 to 11111111
OUTPUT CAPACITANCE							
C_{OUT} A	All	50	50	50	50	pF max	DAC Latches Loaded with 00000000
C_{OUT} B		50	50	50	50	pF max	
C_{OUT} A		120	120	120	120	pF max	DAC Latches Loaded with 11111111
C_{OUT} B		120	120	120	120	pF max	
AC FEEDTHROUGH[6]							
V_{REF} A to OUT A	All	−70	−65	−70	−65	dB max	V_{REF} A, V_{REF} B = 20Vp-p Sine Wave
V_{REF} B to OUT B		−70	−65	−70	−65	dB max	@ 100kHz
CHANNEL TO CHANNEL ISOLATION							Both DAC Latches Loaded with 11111111
V_{REF} A to OUT B	All	−77	—	−77	—	dB typ	V_{REF} A = 20Vp-p Sine Wave @ 100kHz V_{REF} B = 0V. See Figure 6.
V_{REF} B to OUT A		−77	—	−77	—	dB typ	V_{REF} A = 20Vp-p Sine Wave @ 100kHz V_{REF} A = 0V. See Figure 6.
DIGITAL CROSSTALK	All	30	—	60	—	nV sec typ	Measured for Code Transition 00000000 to 11111111
HARMONIC DISTORTION	All	−85	—	−85	—	dB typ	V_{IN} = 6V rms @ 1kHz

NOTES:

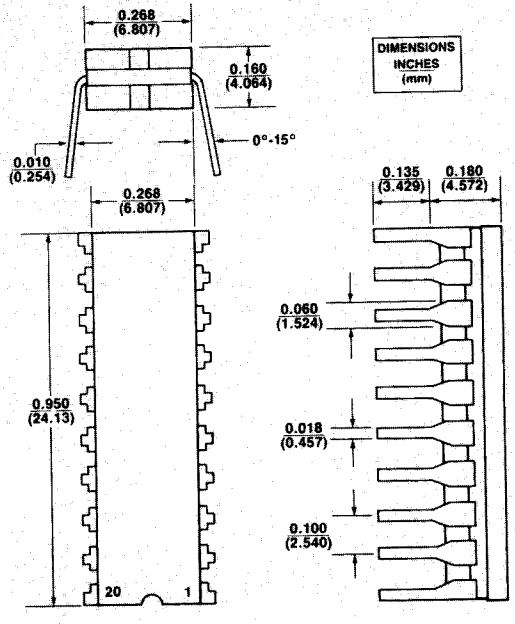
1. Temperature Ranges are: JN, KN, LN — 0 to +70°C
   AD, BD, CD — −25°C to +85°C
   SD, TD, UD — −55°C to +125°C
2. Specification applies to both DACs in HS 7528
3. Logic Inputs are MOS Gates. Typical input current (+25°C) is less than 1nA.
4. Guaranteed by design but not production tested.
5. These characteristics are for design guidance only and are not subject to test.
6. Feedthrough can be further reduced by connecting the metal lid on the ceramic package (suffix D) to DGND.

PACKAGE OUTLINE

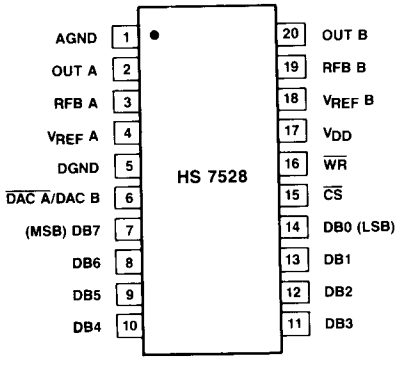
20-PIN PLASTIC DIP (Suffix N)



20-PIN CERDIP (Suffix D)



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND	0V, +17V
V_{DD} to DGND	0V, +17V
AGND to DGND	V_{DD}
DGND to DGND	V_{DD}
Digital Input Voltage to DGND	−0.3V, +15V
$V_{PIN\ 2}$, $V_{PIN\ 20}$ to AGND	−0.3V, +15V
V_{REF} A, V_{REF} B to AGND	±25V
V_{RFB}A, V_{RFB} B to AGND	±25V
Power Dissipation (Any Package) to +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature Range	
Commercial (JN, KN, LN) Grades	0 to +70°C
Industrial (AD, BD, CD) Grades	−25°C to +85°C
Military (SD, TD, UD) Grades	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 secs.)	+300°C

TERMINOLOGY

Relative Accuracy. Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is normally expressed in LSBs or as a percentage of full scale reading.

Differential Nonlinearity. Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ± 1 LSB max over the operating temperature range ensures monotonicity.

Gain Error. Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For the HS 7528, ideal full-scale is V_{REF} − 1 LSB. Gain error of both DACs is adjustable to zero with external resistance.

Output Capacitance. Capacitance from OUT A or OUT B TO AGND.

Glitch Energy. The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA secs or nV secs depending upon whether the glitch is measured as a current or voltage signal. Glitch energy is measured with V_{REF} A, V_{REF} B = AGND.

Propagation Delay. This is a measure of the internal delays of the circuit and is described as the time from a digital input change to the analog output current reaching 90% of its final value.

Channel-to-Channel Isolation. The proportion of input signal from one DAC's reference input which appears at the output of the other DAC, expressed as a ratio in dB.

Digital Crosstalk. The glitch energy transferred to the output of one converter due to a change in digital input code to the other converter. Specified in nV secs. V_{REF} A = V_{REF} B = AGND.

APPLICATIONS INFORMATION

INTERFACE LOGIC INFORMATION

DAC Selection. Both latches share a common 8-Bit input port. The control input $\overline{\text{DAC A}}$/DAC B selects which DAC can accept data from the input port.

Mode Selection. Inputs $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control the operating mode of the selected DAC. See Mode Selection Table below.

Write Mode. When $\overline{\text{CS}}$ and $\overline{\text{WR}}$ are both low the selected DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to activity on DB0-DB7.

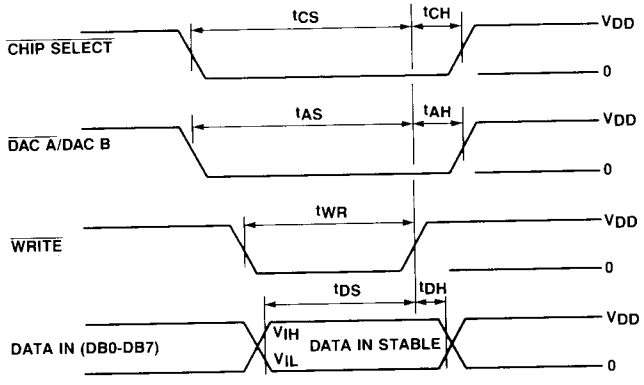
Hold Mode. The selected DAC latch retains the data which was present on DB0-DB7 just prior to $\overline{\text{CS}}$ or $\overline{\text{WR}}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

$\overline{\text{DAC A}}$/ DAC B	$\overline{\text{CS}}$	$\overline{\text{WR}}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State, H = High State, X = Don't Care

Mode Selection Table

WRITE CYCLE TIMING DIAGRAM

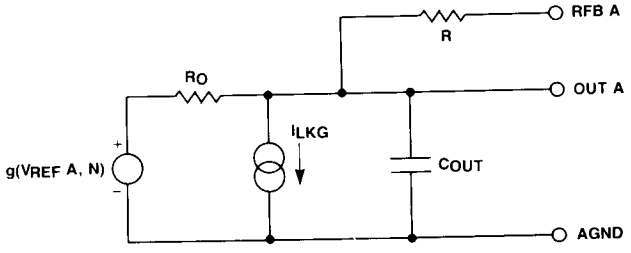


NOTES:
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF VDD. VDD = +5V, $t_r = t_f$ = 20ns; VDD = +15V, $t_r = t_f$ = 40ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

EQUIVALENT CIRCUIT ANALYSIS

Figure 2 shows an approximate equivalent circuit for one of the HS 7528's D/A converters, in this case DAC A. A similar equivalent circuit can be drawn for DAC B. Note that AGND (Pin 1) is common for both DAC A and DAC B.

The current source $I_{LEAKAGE}$ composed of surface and junction leakages and, as with most semiconductor devices, approximately doubles every 10°C. The resistor R_O as shown in Figure 2 is the equivalent output resistance of the device which varies with input code from 0.8R to 2R. R is typically 11kΩ. C_{OUT} is the capacitance due to the N-channel switches and varies from about 50pF to 120pF depending upon the digital input. g(V_{REF} A, N) is the Thevenin equivalent voltage generator due to the reference input voltage V_{REF} A and the transfer function of the R-2R ladder.

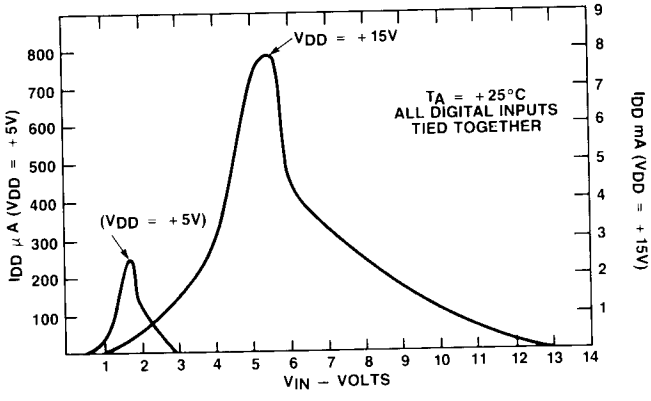


Equivalent Analog Output of DAC A

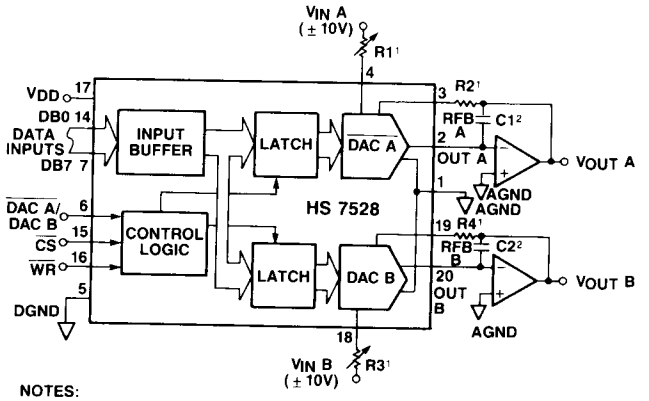
CIRCUIT INFORMATION-DIGITAL SECTION

The input buffers are simple CMOS inverters designed such that when the HS 7528 is operated with V_{DD} = 5V, the buffer converts TTL input levels (2.4V and 0.8V) into CMOS logic levels. When V_{IN} is in the region of 2.0 volts to 3.5 volts the input buffers operate in their linear region and pass a quiescent current, see Figure 3. To minimize power supply currents it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible.

The HS 7528 may be operated with any supply voltage in the range $5 \leqslant V_{DD} \leqslant 15$ volts. With V_{DD} = +15V the input logic levels are CMOS compatible only, i.e., 1.5V and 13.5V.



Typical Plots of Supply Current, I_{DD} vs. Logic Input Voltage V_{IN}, for V_{DD} = +5V and +15V



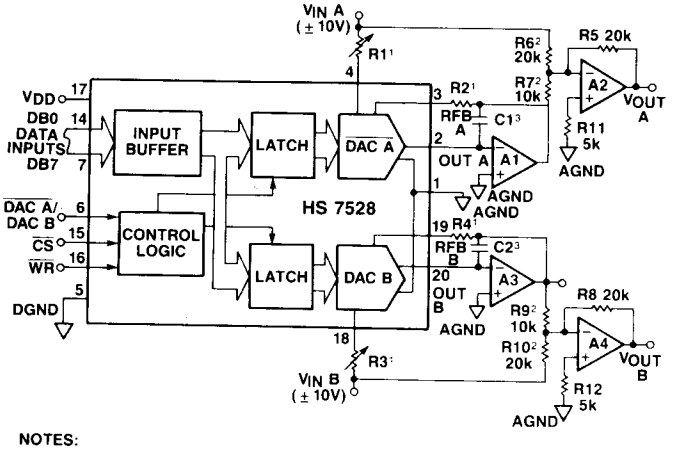
NOTES:
1. R1, R2, AND R3, R4 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED. SEE TABLE 3 FOR RECOMMENDED VALUES.
2. C1, C2 PHASE COMPENSATION (10pF-15pf) IS REQUIRED WHEN USING HIGH SPEED AMPLIFIERS TO PREVENT RINGING OR OSCILLATION

Dual DAC Unipolor Operation (2 Quandrant Multiplication)

DAC Latch Contents MSB LSB	Analog Output (DAC A or DAC B)
11111111	$-V_{IN}\ \frac{255}{256}$
10000001	$-V_{IN}\ \frac{129}{256}$
10000000	$-V_{IN}\ \frac{128}{256} = -\frac{V_{IN}}{2}$
01111111	$-V_{IN}\ \frac{127}{256}$
00000001	$-V_{IN}\ \frac{1}{256}$
00000000	$-V_{IN}\ \frac{0}{256}$

Note: 1 LSB = $(2^{-8})(V_{IN}) = \frac{1}{256}\ (V_{IN})$

Unipolar Binary Code Table



NOTES:
1. R1, R2, AND R3, R4 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED. SEE TABLE 3 FOR RECOMMENDED VALUES.
   ADJUST R1 FOR V_{OUTA} = 0V WITH CODE 10000000 IN DAC A LATCH.
   ADJUST R3 FOR V_{OUTA} = 0V WITH CODE 10000000 IN DAC B LATCH.
2. MATCHING AND TRACKING IS ESSENTIAL FOR RESISTOR PAIRS R6, R7 AND R9, R10.
3. C1, C2 PHASE COMPENSATION (10pF-15pf) MAY BE REQUIRED IF A1/A3 IS A HIGH-SPEED AMPLIFIER.

Dual DAC Bipolar Operation (4 Quadrant Multiplication)

DAC Latch Contents MSB LSB	Analog Output (DAC A or DAC B)
11111111	$+V_{IN}\ \frac{127}{128}$
10000001	$+V_{IN}\ \frac{1}{128}$
10000000	0
01111111	$-V_{IN}\ \frac{1}{128}$
00000001	$-V_{IN}\ \frac{127}{128}$
00000000	$-V_{IN}\ \frac{128}{128}$

Note: 1 LSB = $(2^{-7})(V_{IN}) = \frac{1}{128}\ (V_{IN})$

Bipolar (Offset Binary) Code Table

Trim Resistor	JN/AD/SD	KN/BD/TD	LN/CD/UD
R1:R3	1k	500	200
R2:R4	330	150	82

Recommended Trim Resistor Values vs. Grade

APPLICATION HINTS

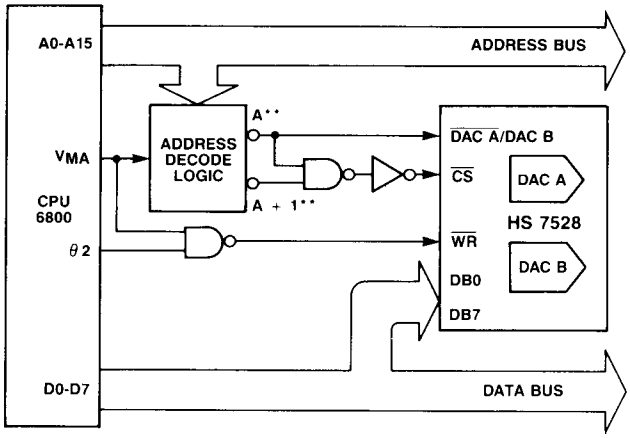
To ensure system performance consistent with HS 7528 specifications, careful attention must be given to the following points:

1. General Ground Management. AC or transient voltages between the HS 7528 AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the HS 7528. In more complex systems where the AGND-DGND intertie is on the back-plane, it is recommended that diodes be connected in inverse parallel between the HS 7528 AGND and DGND pins (1N914 or equivalent).

2. Output Amplifier Offset. CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The effect is a code-dependent differential nonlinearity term at the amplifier output of maximum magnitude 0.67 V_{OS} (V_{OS} is amplifier input offset voltage). This differential nonlinearity term adds to the R/2R differential nonlinearity. To maintain monotonic operation, it is recommended that amplifier V_{OS} be no greater than 10% of 1 LSB over the temperature range of interest.

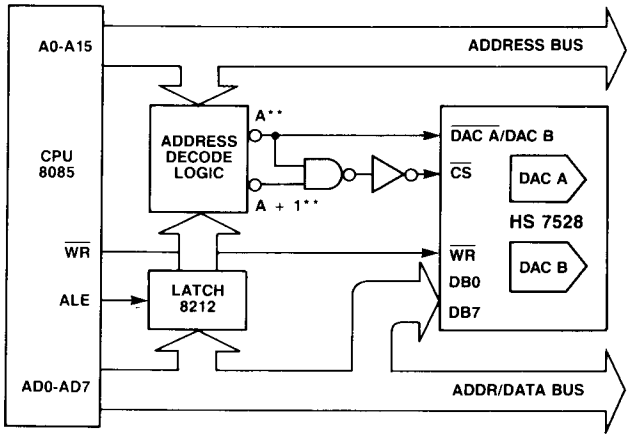
3. High Frequency Considerations. The output capacitance of a CMOS DAC works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This can cause ringing or oscillation. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.

MICROPROCESSOR INTERFACE



*ANALOG CIRCUITRY HAS BEEN OMITTED FOR CLARITY
**A = DECODED 7528 ADDR DAC A
A + 1 = DECODED 7528 ADDR DAC B

HS 7528 Dual DAC to 6800 CPU Interface



*ANALOG CIRCUITRY HAS BEEN OMITTED FOR CLARITY
**A = DECODED 7528 ADDR DAC A
A + 1 = DECODED 7528 ADDR DAC B

NOTE:
8085 INSTRUCTION SHLD (STORE H & L DIRECT) CAN UPDATE BOTH DACs WITH DATA FROM H AND L RESISTERS

HS 7528 Dual DAC to 8085 CPU Interface

ORDERING INFORMATION

RELATIVE ACCURACY	GAIN ERROR	COMMERCIAL PLASTIC 0°C TO +70°C	INDUSTRIAL CERDIP −25°C TO +85°C	EXTENDED TEMP RANGE CERDIP −55°C TO +125°C
±1 LSB	±4 LSB	HS 7528JN	HS 7528AD	HS 7528SD*
±½ LSB	±2 LSB	HS 7528KN	HS 7528BD	HS 7528TD*
±¼ LSB	±1 LSB	HS 7528LN	HS 7528CD	HS 7528UD*

*/883 For MIL-STD-883 Processing

CAUTION:

1. ESD sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not insert this device into powered sockets. Remove power before insertion or removal.

Hybrid Systems CORPORATION

22 Linnell Circle
Billerica, MA 01821
TWX: 710-347-1575 Tel: 617/667-8700

EUROPEAN SALES OFFICES

FRANCE
Hybrid Systems SARL
S.I.L.I.C. 525
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Tel. (1) 687 8336

WEST GERMANY
Hybrid Systems GmbH
Rheinstrasse 32
D-6100 DARMSTADT
Tel: (06151) 291595

UNITED KINGDOM
Hybrid Systems U.K. Ltd.
333 London Road
CAMBERLEY, Surrey GU15 3HQ
Tel: (0276) 28128

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