IS61C64B

8K x 8 HIGH-SPEED CMOS STATIC RAM

July 2002

FEATURES

- High-speed access time: 10, 12, and 15 ns
- Automatic power-down when chip is deselected
- CMOS low power operation
  - — 450 mW (typical) operating
  - — 250 µW (typical) standby
- TTL compatible interface levels
- Single 5V power supply
- Fully static operation: no clock or refresh required
- Three state outputs
- One Chip Enables ($\overline{CE}$) for increased speed

DESCRIPTION

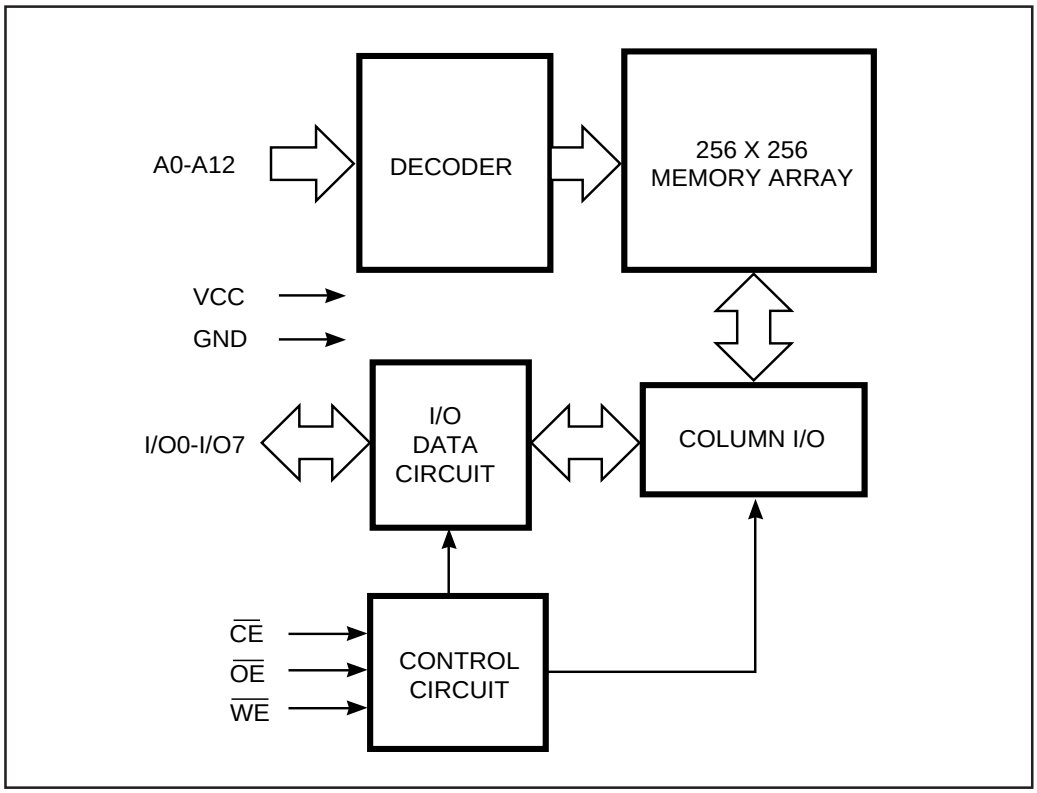
The *ISSI* IS61C64B is a very high-speed, low power, 8192-word by 8-bit static RAM. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 10 ns with low power consumption.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down to 250 µW (typical) with CMOS input levels.

Easy memory expansion is provided by using one Chip Enable input, $\overline{CE}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

The IS61C64B is packaged in the JEDEC standard 28-pin, 300-mil SOJ, and TSOP.

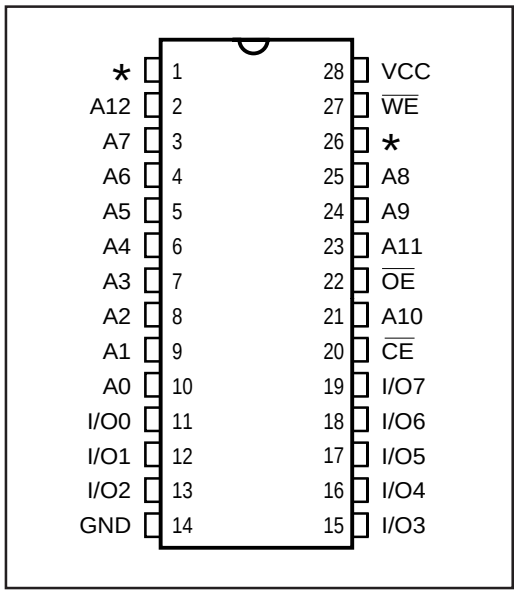
FUNCTIONAL BLOCK DIAGRAM



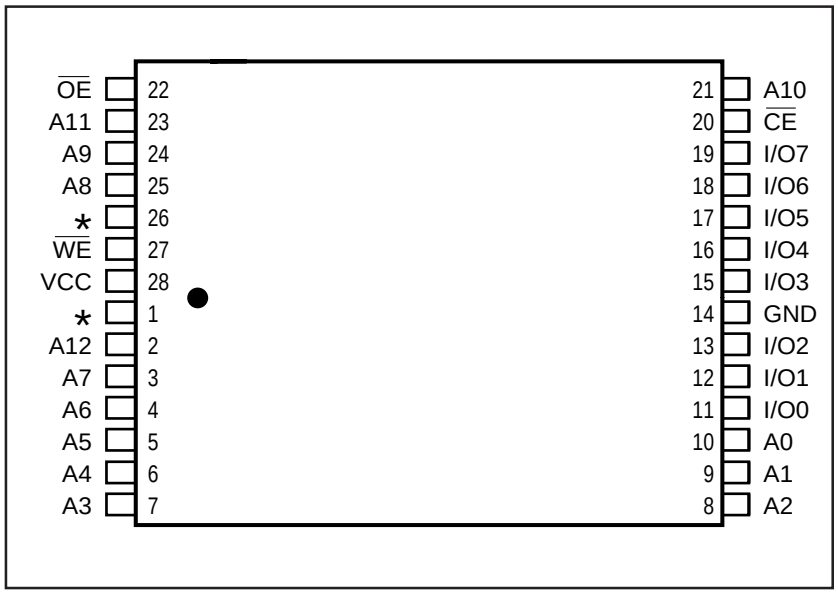
TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	Vcc Current
Not Selected	X	H	X	High-Z	I_{SB1}, I_{SB2}
(Power-down)	X	X	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	High-Z	I_{CC}
Read	H	L	L	D_{OUT}	I_{CC}
Write	L	L	X	D_{IN}	I_{CC}

PIN CONFIGURATION
28-Pin SOJ



PIN CONFIGURATION
28-Pin TSOP (Type 1)



PIN DESCRIPTIONS

A0-A12	Address Inputs
$\overline{CE}$	Chip Enable 1 Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
*	Must be tied to either Vcc or GND
Vcc	Power
GND	Ground

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current (LOW)	20	mA

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	Speed	V_{CC}
Commercial	0°C to +70°C	10 ns	5V ± 5%
		12 ns	5V ± 10%
		15 ns	5V ± 10%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage[1]		–0.5	0.8	V
I_{LI}	Input Leakage	GND - V_{IN} - V_{CC}	–2	2	µA
I_{LO}	Output Leakage	GND - V_{OUT} - V_{CC}, Outputs Disabled	–2	2	µA

Notes:
1. V_{IL} = –3.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions	-10ns Min.	-10ns Max.	-12ns Min.	-12ns Max.	-15ns Min.	-15ns Max.	Unit
I_{CC}	Vcc Dynamic Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX}	—	185	—	175	—	135	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CE1}$ • V_{IH} or CE2 - V_{IL}, f = 0	—	30	—	30	—	30	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., $\overline{CE1}$ • V_{CC} – 0.2V, CE2 - 0.2V, V_{IN} • V_{CC} – 0.2V, or V_{IN} - 0.2V, f = 0	—	10	—	10	—	10	mA

Notes:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	10	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, Vcc = 5.0V.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-10ns Min.	-10ns Max.	-12ns Min.	-12ns Max.	-15ns Min.	-15ns Max.	Unit
t_{RC}	Read Cycle Time	10	—	12	—	15	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	ns
t_{OHA}	Output Hold Time	2	—	2	—	2	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	10	—	12	—	15	ns
t_{DOE}	$\overline{OE}$ Access Time	—	5	—	6	—	7	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	0	—	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	5	—	6	—	6	ns
t_{LZCE1}[2]	$\overline{CE}$ to Low-Z Output	2	—	3	—	3	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	—	5	—	7	—	8	ns

Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1a and 1b

AC TEST LOADS

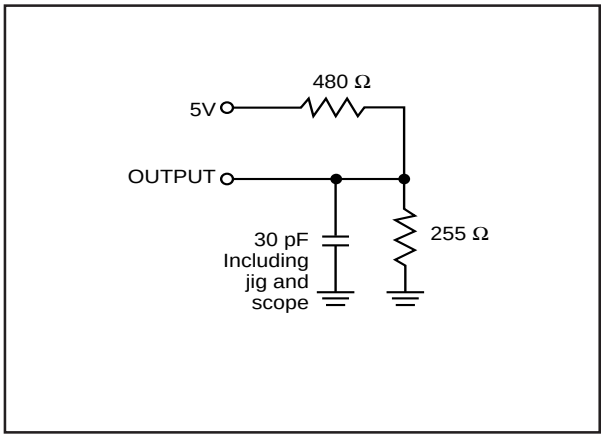


Figure 1a.

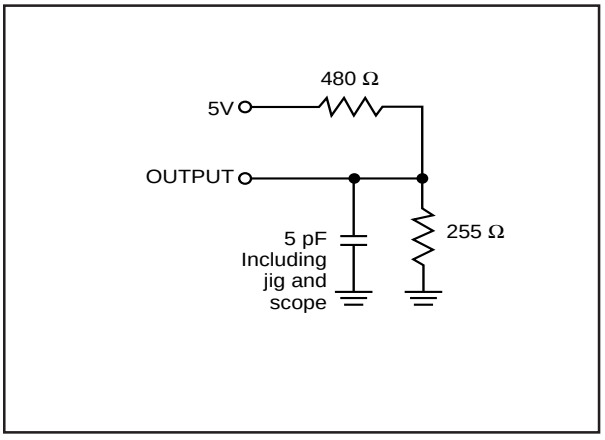
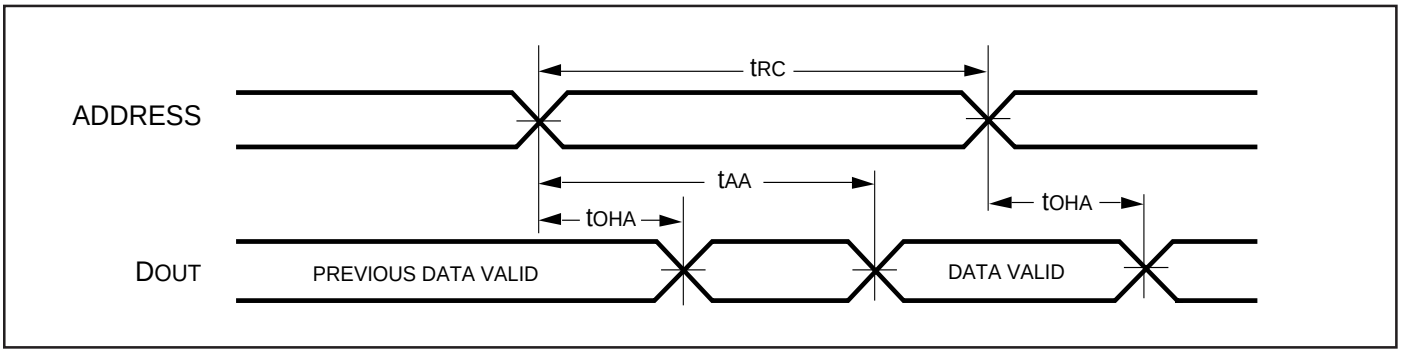


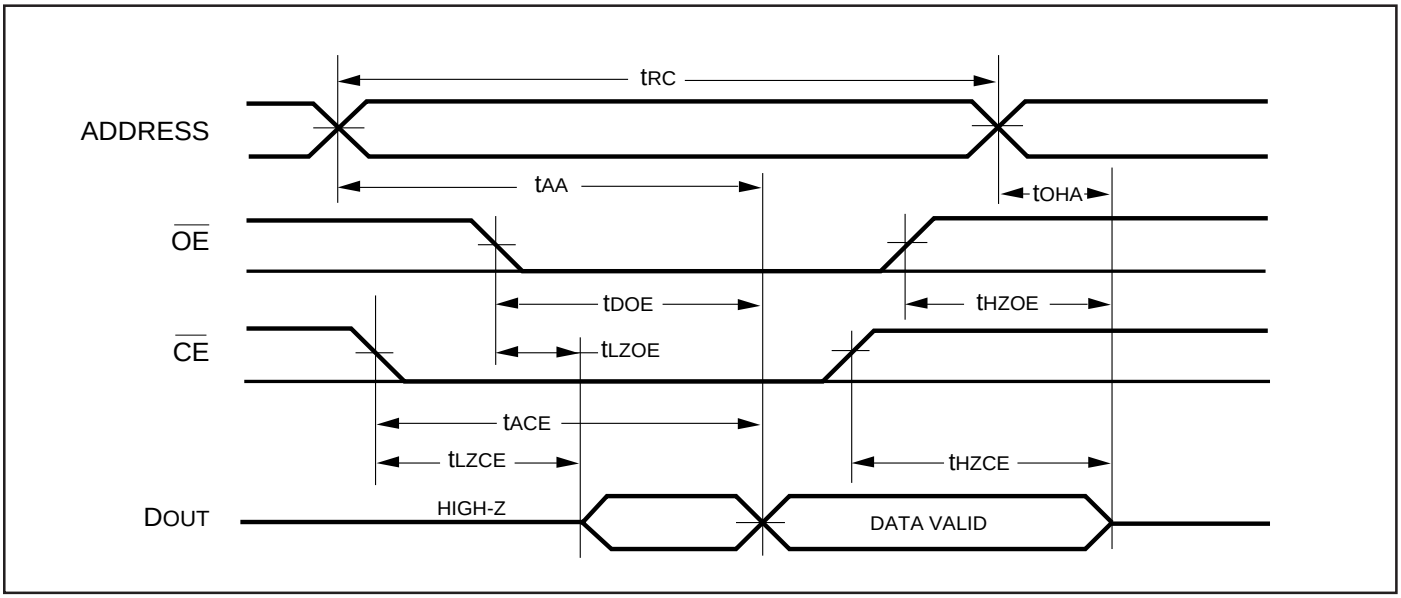
Figure 1b.

AC WAVEFORMS

READ CYCLE NO. 1[1,2]



READ CYCLE NO. 2[1,3]



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

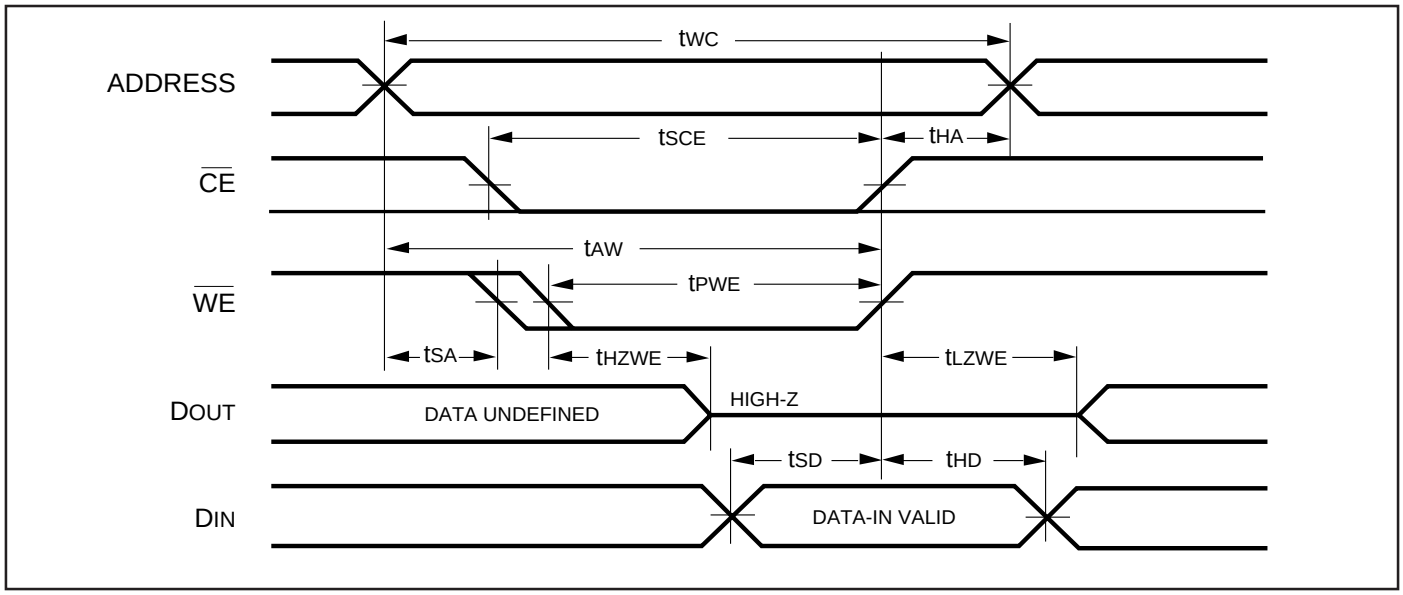
WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

Symbol	Parameter	-10ns Min.	-10ns Max.	-12ns Min.	-12ns Max.	-15ns Min.	-15ns Max.	Unit
t_{WC}	Write Cycle Time	10	—	12	—	15	—	ns
t_{SCE}	$\overline{CE}$ to Write End	9	—	10	—	12	—	ns
t_{AW}	Address Setup Time to Write End	9	—	10	—	12	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	ns
t_{PWE}[4]	$\overline{WE}$ Pulse Width	8	—	8	—	10	—	ns
t_{SD}	Data Setup to Write End	8	—	8	—	9	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	—	6	—	6	—	7	ns
t_{LZWE}[2]	$\overline{WE}$ HIGH to Low-Z Output	0	—	0	—	0	—	ns

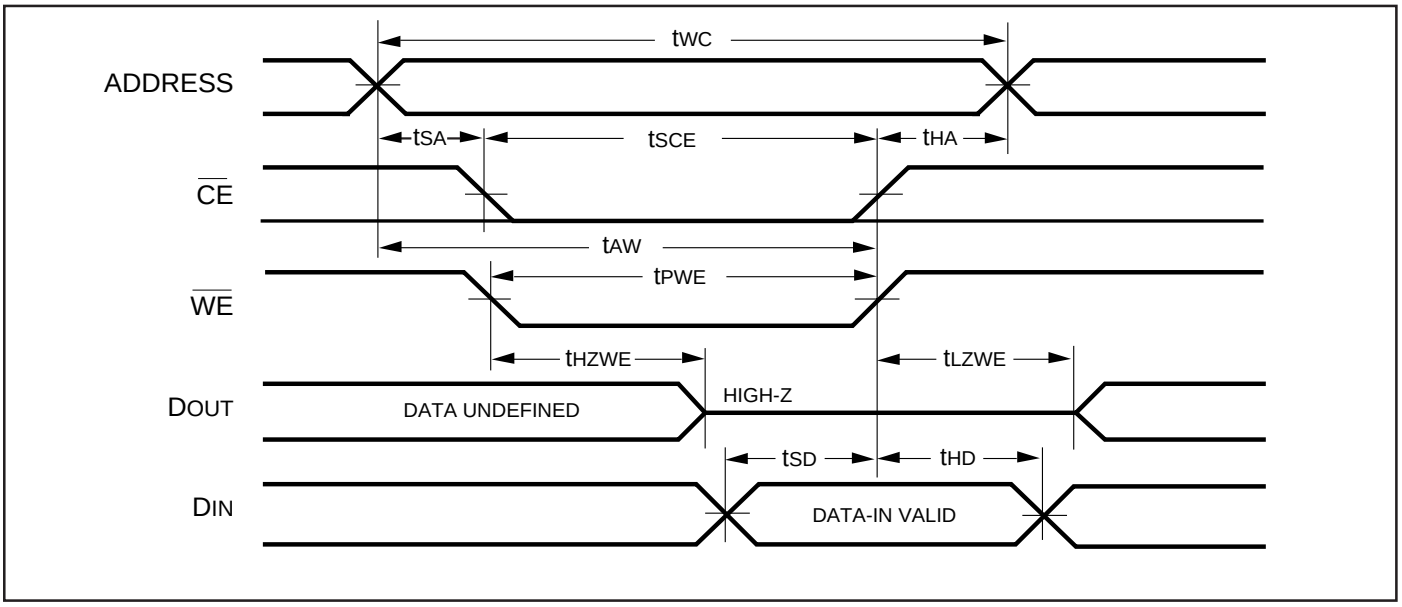
Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

AC WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)[1,2]



WRITE CYCLE NO. 2 ($\overline{CE}$1, CE2 Controlled)[1,2]



Notes:
1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
2. I/O will assume the High-Z state if $\overline{OE}$ = V_{IH}.

ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
10	IS61C64B-10J	300-mil Plastic SOJ
	IS61C64B-10T	Plastic TSOP
12	IS61C64B-12J	300-mil Plastic SOJ
	IS61C64B-12T	Plastic TSOP
15	IS61C64B-15J	300-mil Plastic SOJ
	IS61C64B-15T	Plastic TSOP