# DRAM

MT4C1M16C3
MT4LC1M16C3

## FEATURES

- JEDEC- and industry-standard x16 timing, functions, pinouts and packages
- High-performance, low power CMOS silicon-gate process
- Single power supply (+3.3V ±0.3V or 5V ±10%)
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS#-ONLY, CAS#-BEFORE-RAS# (CBR) and HIDDEN
- Optional Self Refresh (S) for low power data retention
- BYTE WRITE and BYTE READ access cycles
- 1,024-cycle refresh (10 row, 10 column addresses)
- 5V-tolerant inputs and I/Os on 3.3V devices

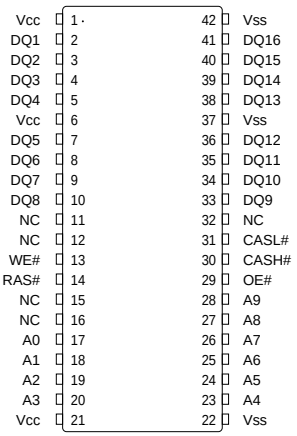
## OPTIONS — MARKING

- Voltage
  - 3.3V — LC
  - 5V — C
- Packages
  - Plastic SOJ (400 mil) — DJ
  - Plastic TSOP (400 mil) — TG
- Timing
  - 60ns access — -6
  - 70ns access (3.3V only) — -7
- Refresh Rate
  - Standard 16ms period — None
  - Self Refresh and 128ms period — S
- Part Number Example: MT4LC1M16C3TG-6

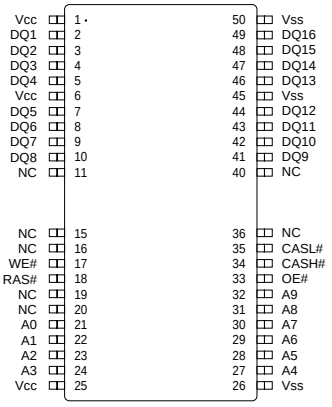
*Note: The 1 Meg x 16 FPM DRAM base number differentiates the offerings in one place -* MT4LC1M16C3. *The third field distinguishes the low voltage offering: LC designates Vcc = 3.3V and C designates Vcc = 5V.*

## PIN ASSIGNMENT (Top View)

### 42-Pin SOJ (DA-7)




### 44/50-Pin TSOP (DB-6)




**Note:** The # symbol indicates signal is active LOW.

## 1 MEG x 16 FPM DRAM PART NUMBERS

| PART NUMBER | Vcc | PACKAGE | REFRESH |
|---|---|---|---|
| MT4LC1M16C3DJ | 3.3V | SOJ | Standard |
| MT4LC1M16C3DJS | 3.3V | SOJ | Self |
| MT4LC1M16C3TG | 3.3V | TSOP | Standard |
| MT4LC1M16C3TGS | 3.3V | TSOP | Self |
| MT4C1M16C3DJ | 5V | SOJ | Standard |
| MT4C1M16C3DJS | 5V | SOJ | Self |
| MT4C1M16C3TG | 5V | TSOP | Standard |
| MT4C1M16C3TGS | 5V | TSOP | Self |

## KEY TIMING PARAMETERS

| SPEED | tRC | tRAC | tPC | tAA | tCAC | tRP |
|---|---|---|---|---|---|---|
| -6 | 110ns | 60ns | 35ns | 30ns | 15ns | 40ns |
| -7 | 130ns | 70ns | 40ns | 35ns | 20ns | 50ns |

## GENERAL DESCRIPTION

The 1 Meg x 16 DRAM is a randomly accessed, solid-state memory containing 16,777,216 bits organized in a x16 configuration. The 1 Meg x 16 DRAM has both BYTE WRITE and WORD WRITE access cycles via two CAS# pins (CASL# and CASH#). These function in an identical manner to a single CAS# of other DRAMs in that either CASL# or CASH# will generate an internal CAS#.

The CAS# function and timing are determined by the first CAS# (CASL# or CASH#) to transition LOW and the last CAS# to transition back HIGH. Use of only one of the two results in a BYTE access cycle. CASL# transitioning LOW selects an access cycle for the lower byte (DQ1-DQ8) and CASH# transitioning LOW selects an access cycle for the upper byte (DQ9-DQ16).

## GENERAL DESCRIPTION (continued)

Each bit is uniquely addressed through the 20 address bits during READ or WRITE cycles. These are entered 10 bits (A0-A9) at a time. RAS# is used to latch the first 10 bits and CAS# the latter 10 bits. The CAS# function is determined by the first CAS# (CASL# or CASH#) to transition LOW and the last one to transition back HIGH. The CAS# function also determines whether the cycle will be a refresh cycle (RAS#-ONLY) or an active cycle (READ, WRITE or READ WRITE) once RAS# goes LOW.

The CASL# and CASH# inputs internally generate a CAS# signal functioning in an identical manner to the single CAS# input of other DRAMs. The key difference is each CAS# input (CASL# and CASH#) controls its corresponding DQ tristate logic (in conjunction with OE# and WE#). CASL# controls DQ1 through DQ8 and CASH# controls DQ9 through DQ16. The two CAS# controls give the 1 Meg x 16 DRAM BYTE WRITE cycle capabilities.

A logic HIGH on WE# dictates READ mode while a logic LOW on WE# dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS, whichever occurs last. Taking WE# LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If WE# goes LOW prior to CAS# going LOW, the output pin(s) remain open (High-Z) until the next CAS# cycle. If WE# goes LOW after CAS# goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as CAS# and OE# remain LOW (regardless of WE# or RAS#). This late WE# pulse results in a READ WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O. Pin direction is controlled by OE# and WE#.

## FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS# followed by a column address strobed-in by CAS#. CAS# may be toggled-in by holding RAS# LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS# HIGH terminates the FAST PAGE MODE operation.

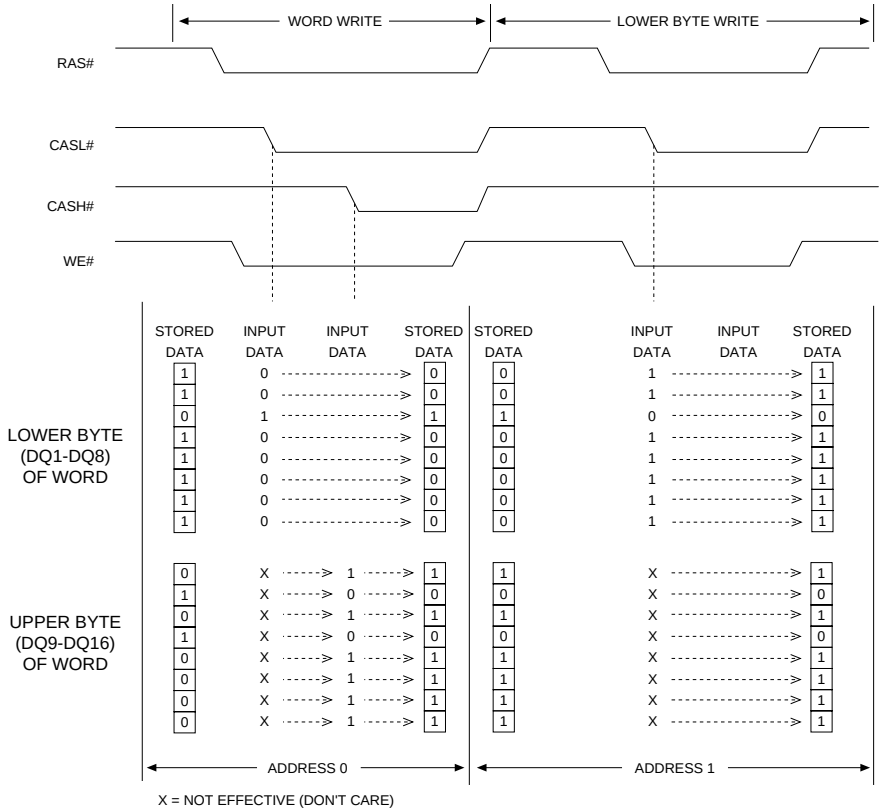



**Figure 1**
**WORD AND BYTE WRITE EXAMPLE**

## FAST PAGE MODE (continued)

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the RAS# HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# refresh cycle (RAS# ONLY, CBR, or HIDDEN) so that all 1,024 combinations of RAS# addresses (A0-A9) are executed at least every 16ms (128ms on the "S" version), regardless of sequence. The CBR Refresh cycle will also invoke the refresh counter and controller for row-address control.

## BYTE ACCESS CYCLE

The BYTE WRITEs and BYTE READs are determined by the use of CASL# and CASH#. Enabling CASL# will select a lower BYTE access (DQ1-DQ8). Enabling CASH# will select an upper BYTE access (DQ9-DQ16). Enabling both CASL# and CASH# selects a WORD WRITE cycle.

The 1 Meg x 16 DRAM may be viewed as two 1 Meg x 8 DRAMs that have common input controls, with the exception of the CAS inputs. Figure 1 illustrates the BYTE WRITE and WORD WRITE cycles. Figure 2 illustrates BYTE READ and WORD READ cycles.

Additionally, both bytes must always be of the same mode of operation if both bytes are active. A CAS# precharge must be satisfied prior to changing modes of operation between the upper and lower bytes. For example, an EARLY WRITE on one byte and a LATE WRITE on the other byte are not allowed during the same cycle. However, an EARLY WRITE on one byte and, after a CAS# precharge has been satisfied, a LATE WRITE on the other byte are permissible.

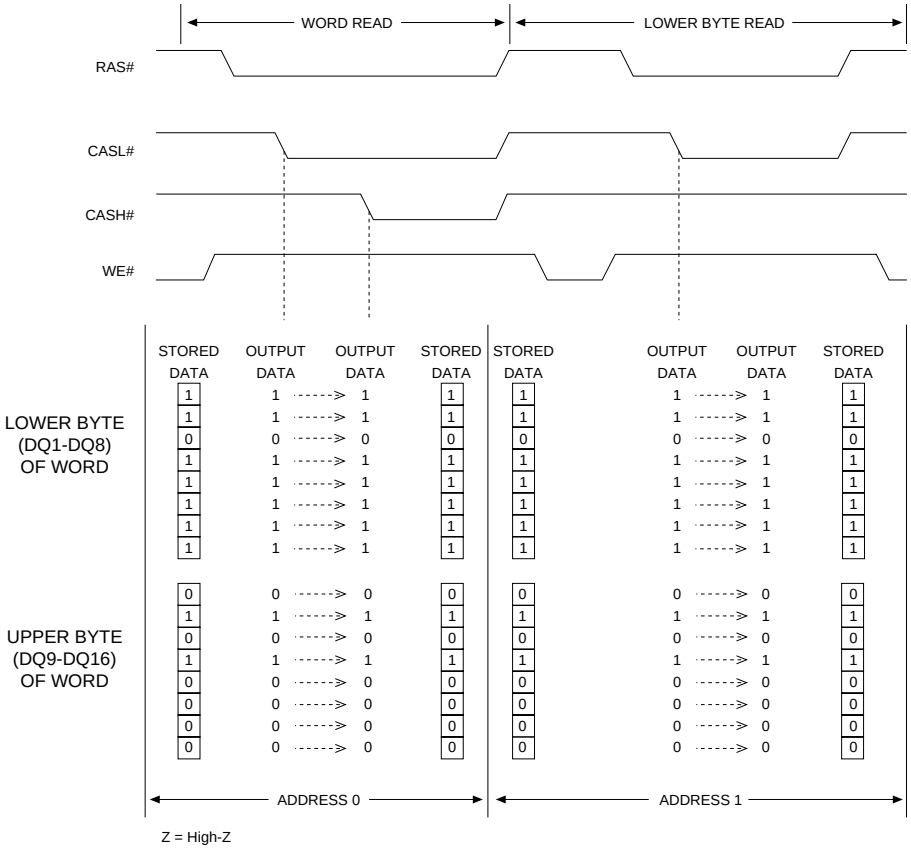



**Figure 2**
**WORD READ EXAMPLE**

## REFRESH

Preserve correct memory cell data by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# refresh cycle (RAS#-ONLY, CBR, or HIDDEN) so that all 1,024 combinations of RAS# addresses are executed within $^{t}$REF (MAX), regardless of sequence. The CBR and Extended and Self Refresh cycles will invoke the internal refresh counter for automatic RAS# addressing.

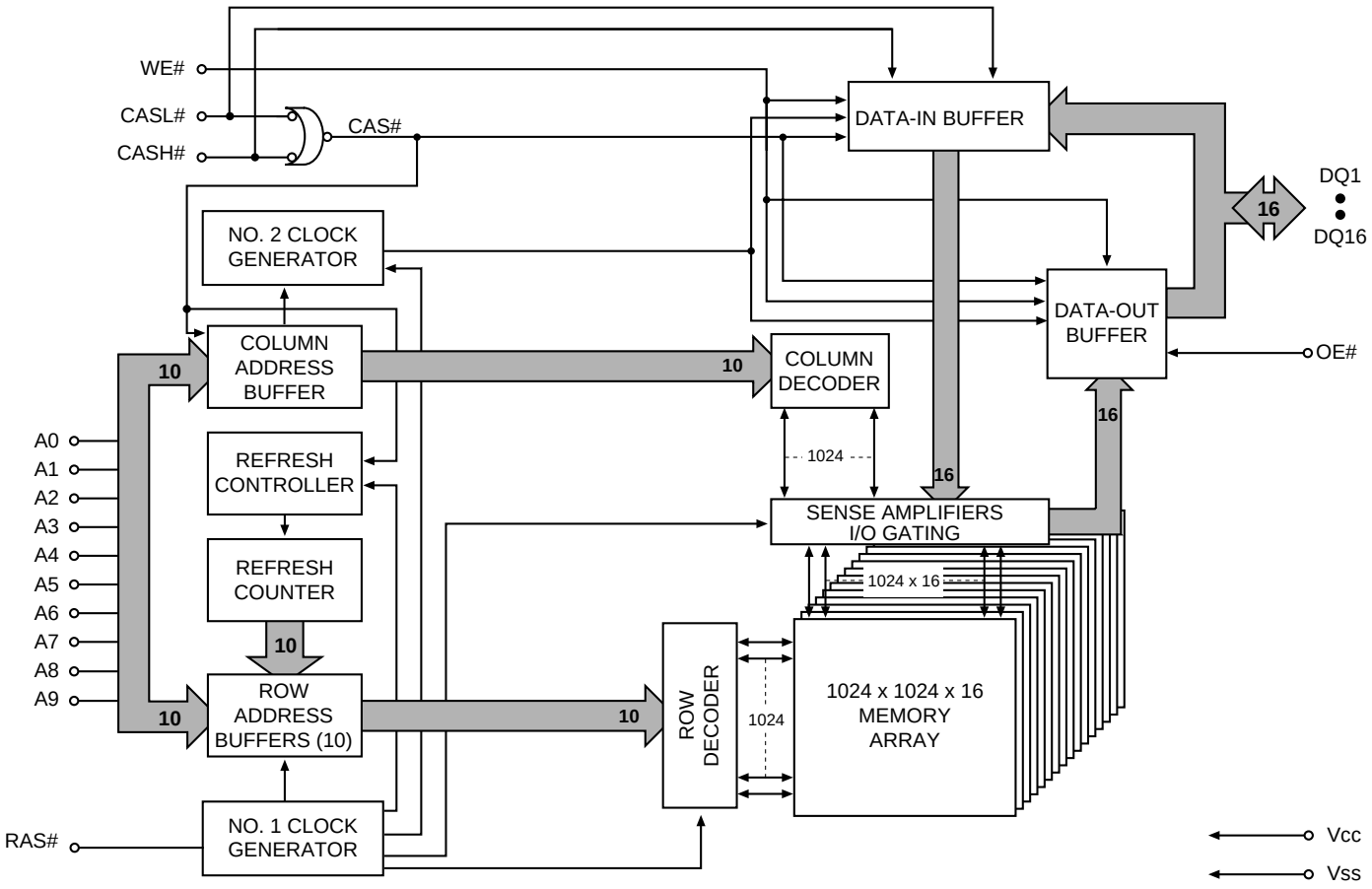
The optional Self Refresh mode is available on the "S" version. The "S" option allows the user a dynamic refresh, data retention mode at the extended refresh period of 128ms, i.e. 125µs per row when using distributed CBR refreshes. The "S" option also allows the user the choice of a fully static low-power data retention mode. The optional Self Refresh feature is initiated by performing a CBR Refresh cycle and holding RAS# LOW for the specified $^{t}$RASS.

The Self Refresh mode is terminated by driving RAS# HIGH for a minimum time of $^{t}$RPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS# LOW-to-HIGH transition. If the DRAM controller uses a distributed refresh sequence, a burst refresh is not required upon exiting Self Refresh. However, if the DRAM controller utilizes RAS#-ONLY or burst refresh sequence, all 1,024 rows must be refreshed within the average internal refresh rate prior to the resumption of normal operation.

## STANDBY

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is preconditioned for the next cycle during the RAS# HIGH time.

## FUNCTIONAL BLOCK DIAGRAM



## TRUTH TABLE

| FUNCTION | | RAS# | CASL# | CASH# | WE# | OE# | ADDRESSES $^tR$ | ADDRESSES $^tC$ | DQs | NOTES |
|---|---|---|---|---|---|---|---|---|---|---|
| Standby | | H | H→X | H→X | X | X | X | X | High-Z | |
| READ: WORD | | L | L | L | H | L | ROW | COL | Data-Out | |
| READ: LOWER BYTE | | L | L | H | H | L | ROW | COL | Lower Byte, Data-Out<br>Upper Byte, Data-Out | |
| READ: UPPER BYTE | | L | H | L | H | L | ROW | COL | Lower Byte, Data-Out<br>Upper Byte, Data-Out | |
| WRITE: WORD (EARLY WRITE) | | L | L | L | L | X | ROW | COL | Data-In | |
| WRITE: LOWER BYTE (EARLY) | | L | L | H | L | X | ROW | COL | Lower Byte, Data-In<br>Upper Byte, High-Z | |
| WRITE: UPPER BYTE (EARLY) | | L | H | L | L | X | ROW | COL | Lower Byte, High-Z<br>Upper Byte, Data-In | |
| READ WRITE | | L | L | L | H→L | L→H | ROW | COL | Data-Out, Data-In | 1 |
| PAGE-MODE | 1st Cycle | L | H→L | H→L | H | L | ROW | COL | Data-Out | |
| READ | 2nd Cycle | L | H→L | H→L | H | L | n/a | COL | Data-Out | |
| PAGE-MODE | 1st Cycle | L | H→L | H→L | L | X | ROW | COL | Data-In | 1 |
| WRITE | 2nd Cycle | L | H→L | H→L | L | X | n/a | COL | Data-In | 1 |
| PAGE-MODE | 1st Cycle | L | H→L | H→L | H→L | L→H | ROW | COL | Data-Out, Data-In | 1 |
| READ-WRITE | 2nd Cycle | L | H→L | H→L | H→L | L→H | n/a | COL | Data-Out, Data-In | 1 |
| HIDDEN | READ | L→H→L | L | L | H | L | ROW | COL | Data-Out | |
| REFRESH | WRITE | L→H→L | L | L | L | X | ROW | COL | Data-In | 1, 2 |
| RAS#-ONLY REFRESH | | L | H | H | X | X | ROW | n/a | High-Z | |
| CBR REFRESH | | H→L | L | L | H | X | X | X | High-Z | 3 |
| SELF REFRESH | | H→L | L | L | H | X | X | X | High-Z | 3 |

**NOTE:** 1. These WRITE cycles may also be BYTE WRITE cycles (either CASL# or CASH# active).
2. EARLY WRITE only.
3. Only one CAS# must be active (CASL# or CASH#).

## ABSOLUTE MAXIMUM RATINGS*

Voltage on $V_{CC}$ pin Relative to $V_{SS}$:
- 3.3V ..... -1V to +4.6V
- 5V ..... -1V to +7V

Voltage on NC, Inputs or I/O pins Relative to $V_{SS}$:
- 3.3V ..... -1V to +5.5V
- 5V ..... -1V to +7V

Operating Temperature, $T_A$ (ambient) ..... 0°C to +70°C
Storage Temperature (plastic)..... -55°C to +150°C
Power Dissipation ..... 1W
Short Circuit Output Current ..... 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1, 2, 3)

| PARAMETER/CONDITION | SYMBOL | 3.3V | | 5V | | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | | |
| Supply Voltage | $V_{CC}$ | 3.0 | 3.6 | 4.5 | 5.5 | V | |
| Input High Voltage:<br>Valid Logic 1; all inputs, I/Os and any NC | $V_{IH}$ | 2.0 | 5.5 | 2.4 | $V_{CC}$ +1 | V | |
| Input Low Voltage:<br>Valid Logic 0; all inputs, I/Os and any NC | $V_{IL}$ | -1.0 | 0.8 | -0.5 | 0.8 | V | |
| Input Leakage Current:<br>Any input at $V_{IN}$ ($0V \le V_{IN} \le V_{IH_{MAX}}$);<br>all other pins not under test = 0V | $I_I$ | -2 | 2 | -2 | 2 | µA | |
| Output High Voltage:<br>$I_{OUT}$ = -2mA (3.3V), -5mA (5.0V) | $V_{OH}$ | 2.4 | - | 2.4 | - | V | |
| Output Low Voltage:<br>$I_{OUT}$ = 2mA (3.3V), 4.2mA (5.0V) | $V_{OL}$ | - | 0.4 | - | 0.4 | V | |
| Output Leakage Current:<br>Any output at $V_{OUT}$ ($0V \le V_{OUT} \le 5.5V$);<br>DQ is disabled and in High-Z state | $I_{OZ}$ | -5 | 5 | -5 | 5 | µA | |

## $I_{CC}$ OPERATING CONDITIONS AND MAXIMUM LIMITS

(Notes: 1, 2, 3) ($V_{CC_{MIN}} \le V_{CC} \le V_{CC_{MAX}}$)

| PARAMETER/CONDITION | SYM | SPEED | 3.3V | 5V | UNITS | NOTES |
|---|---|---|---|---|---|---|
| STANDBY CURRENT: TTL<br>(RAS# = CAS# = $V_{IH}$) | $I_{CC1}$ | ALL | 1 | 2 | mA | |
| STANDBY CURRENT: CMOS (non-S version only)<br>(RAS# = CAS# = other inputs = $V_{CC}$ -0.2V) | $I_{CC2}$ | ALL | 500 | 500 | µA | 22 |
| STANDBY CURRENT: CMOS (S version only)<br>(RAS# = CAS# = other inputs = $V_{CC}$ -0.2V) | $I_{CC2}$ | ALL | 150 | 150 | µA | 22 |
| OPERATING CURRENT: Random READ/WRITE<br>Average power supply current<br>(RAS#, CAS#, address cycling: $^tRC$ = $^tRC$ [MIN]) | $I_{CC3}$ | -6 | 170 | 180 | mA | 3, 23 |
| | | -7 | 160 | – | | |
| OPERATING CURRENT: FAST PAGE MODE<br>Average power supply current<br>(RAS# = $V_{IL}$, CAS#, address cycling: $^tPC$ = $^tPC$ [MIN]) | $I_{CC4}$ | -6 | 90 | 110 | mA | 3, 23 |
| | | -7 | 80 | – | | |
| REFRESH CURRENT: RAS#-ONLY<br>Average power supply current<br>(RAS# cycling, CAS# = $V_{IH}$: $^tRC$ = $^tRC$ [MIN]) | $I_{CC5}$ | -6 | 170 | 180 | mA | 3 |
| | | -7 | 160 | – | | |
| REFRESH CURRENT: CBR<br>Average power supply current<br>(RAS#, CAS#, address cycling: $^tRC$ = $^tRC$ [MIN]) | $I_{CC6}$ | -6 | 170 | 180 | mA | 3, 4 |
| | | -7 | 160 | – | | |
| REFRESH CURRENT: Extended (S version only)<br>Average power supply current: CAS# = 0.2V or CBR cycling;<br>RAS# = $^tRAS$ (MIN); WE# = $V_{CC}$ -0.2V; A0-A11, OE# and<br>$D_{IN}$ = $V_{CC}$ -0.2V or 0.2V ($D_{IN}$ may be left open) | $I_{CC7}$ | ALL | 300 | 300 | µA | 3, 4 |
| REFRESH CURRENT: Self (S version only)<br>Average power supply current: CBR with RAS# ≥ $^tRASS$ (MIN) and<br>CAS# held LOW; WE# = $V_{CC}$ -0.2V; A0-A11,<br>OE# and $D_{IN}$ = $V_{CC}$ -0.2V or 0.2V ($D_{IN}$ may be left open) | $I_{CC8}$ | ALL | 300 | 300 | µA | 3, 4 |

## CAPACITANCE

| PARAMETER | SYMBOL | MAX | UNITS | NOTES |
|---|---|---|---|---|
| Input Capacitance: Addresses | $C_{I1}$ | 5 | pF | 2 |
| Input Capacitance: RAS#, CASL#, CASH#, WE#, OE# | $C_{I2}$ | 7 | pF | 2 |
| Input/Output Capacitance: DQ | $C_{IO}$ | 7 | pF | 2 |

## AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) ($V_{CC_{MIN}} \le V_{CC} \le V_{CC_{MAX}}$)

| AC CHARACTERISTICS | | -6 | | -7* | | | |
|---|---|---|---|---|---|---|---|
| PARAMETER | SYM | MIN | MAX | MIN | MAX | UNITS | NOTES |
| Access time from column address | $^tAA$ | | 30 | | 35 | ns | |
| Column-address hold time (referenced to RAS#) | $^tAR$ | 45 | | 55 | | ns | |
| Column-address setup time | $^tASC$ | 0 | | 0 | | ns | 27 |
| Row-address setup time | $^tASR$ | 0 | | 0 | | ns | |
| Column-address to WE# delay time | $^tAWD$ | 55 | | 60 | | ns | 18 |
| Access time from CAS | $^tCAC$ | | 15 | | 20 | ns | 29 |
| Column-address hold time | $^tCAH$ | 10 | | 12 | | ns | 27 |
| CAS# pulse width | $^tCAS$ | 15 | 10,000 | 20 | 10,000 | ns | 35 |
| CAS# LOW to “don’t care” during Self Refresh | $^tCHD$ | 15 | | 15 | | ns | |
| CAS# hold time (CBR Refresh) | $^tCHR$ | 10 | | 15 | | ns | 4, 28 |
| Last CAS# going LOW to first CAS# to return HIGH | $^tCLCH$ | 10 | | 10 | | ns | 31 |
| CAS# to output in Low-Z | $^tCLZ$ | 3 | | 3 | | ns | 26, 29 |
| CAS# precharge time | $^tCP$ | 10 | | 10 | | ns | 32 |
| Access time from CAS# precharge | $^tCPA$ | | 35 | | 40 | ns | 28 |
| CAS# to RAS# precharge time | $^tCRP$ | 5 | | 5 | | ns | 28 |
| CAS# hold time | $^tCSH$ | 60 | | 70 | | ns | 28 |
| CAS# setup time (CBR Refresh) | $^tCSR$ | 5 | | 5 | | ns | 4, 27 |
| CAS# to WE# delay time | $^tCWD$ | 40 | | 45 | | ns | 18, 27 |
| Write command to CAS# lead time | $^tCWL$ | 15 | | 20 | | ns | 23, 30 |
| Data-in hold time | $^tDH$ | 10 | | 12 | | ns | 19, 29 |
| Data-in setup time | $^tDS$ | 0 | | 0 | | ns | 19, 29 |
| Output disable | $^tOD$ | 3 | 15 | 3 | 20 | ns | 25, 26, 37 |
| Output enable | $^tOE$ | | 15 | | 20 | ns | 30 |
| OE# hold time from WE# during READ-MODIFY-WRITE cycle | $^tOEH$ | 15 | | 20 | | ns | 25 |
| Output buffer turn-off delay | $^tOFF$ | 3 | 15 | 3 | 20 | ns | 17, 26, 29 |
| OE# setup prior to RAS# during HIDDEN Refresh cycle | $^tORD$ | 0 | | 0 | | ns | |
| FAST-PAGE-MODE READ or WRITE cycle time | $^tPC$ | 35 | | 40 | | ns | 31 |
| FAST-PAGE-MODE READ-WRITE cycle time | $^tPRWC$ | 85 | | 95 | | ns | 31 |

*3.3V only

## AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) ($V_{CC_{MIN}} \leq V_{CC} \leq V_{CC_{MAX}}$)

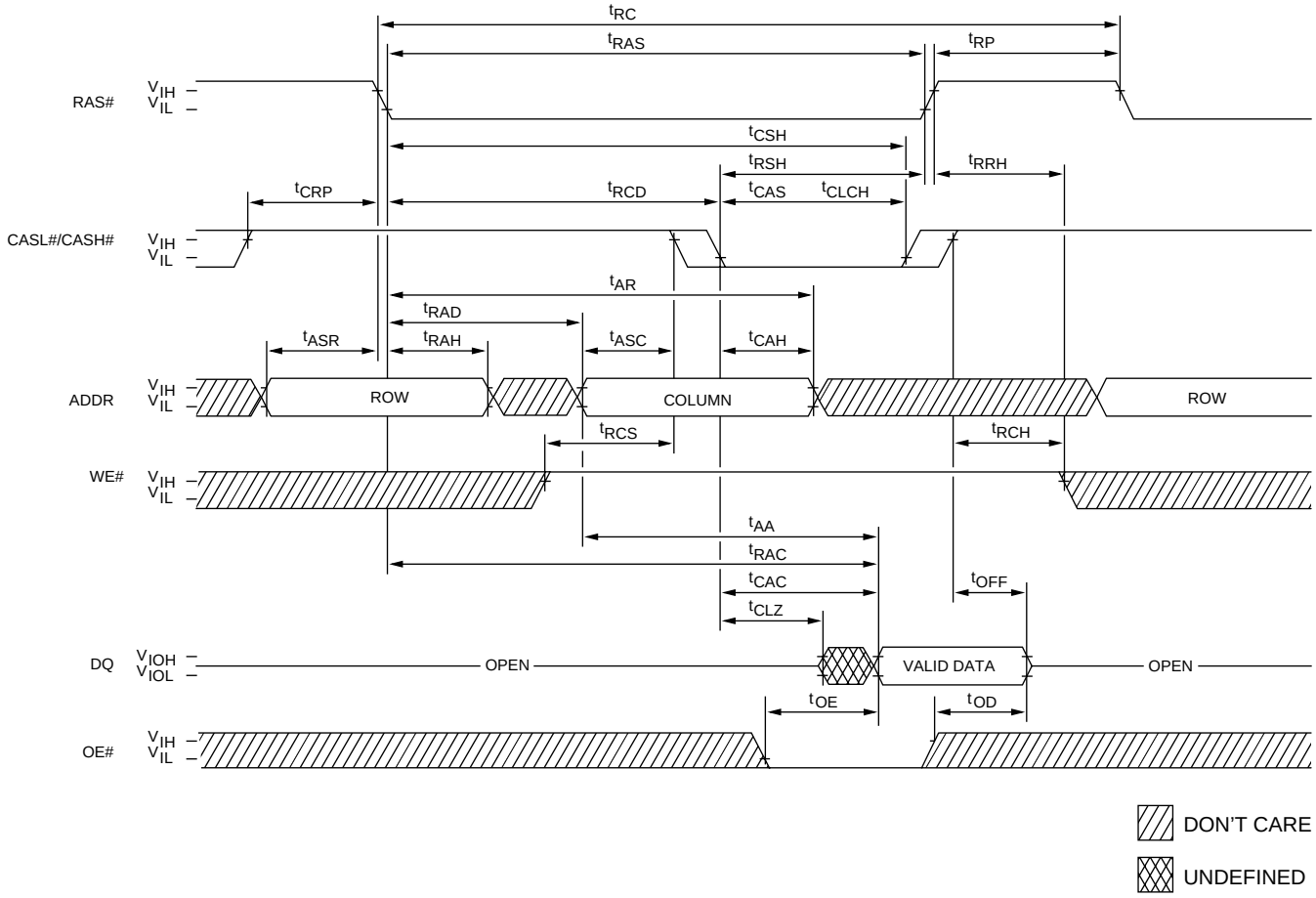
| AC CHARACTERISTICS | | -6 | | -7* | | | |
|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYM** | **MIN** | **MAX** | **MIN** | **MAX** | **UNITS** | **NOTES** |
| Access time from RAS# | tRAC | | 60 | | 70 | ns | |
| RAS# to column-address delay time | tRAD | 15 | | 15 | | ns | 15 |
| Row-address hold time | tRAH | 10 | | 10 | | ns | |
| RAS# pulse width | tRAS | 60 | 10,000 | 70 | 10,000 | ns | |
| RAS# pulse width (FAST PAGE MODE) | tRASP | 60 | 125,000 | 70 | 125,000 | ns | |
| RAS# pulse width (Self Refresh) | tRASS | 100 | | 100 | | µs | |
| Random READ or WRITE cycle time | tRC | 110 | | 130 | | ns | |
| RAS# to CAS# delay time | tRCD | 20 | | 20 | | ns | 14, 27 |
| Read command hold time (referenced to CAS) | tRCH | 0 | | 0 | | ns | 16, 28 |
| Read command setup time | tRCS | 0 | | 0 | | ns | 27 |
| Refresh period (1,024 cycles) | tREF | | 16 | | 16 | ms | |
| Refresh period (1,024 cycles) S version | tREF | | 128 | | 128 | ms | |
| RAS# precharge time | tRP | 40 | | 50 | | ns | |
| RAS# to CAS# precharge time | tRPC | 0 | | 0 | | ns | |
| RAS# precharge time (Self Refresh) | tRPS | 110 | | 130 | | ns | |
| Read command hold time (referenced to RAS#) | tRRH | 0 | | 0 | | ns | 16 |
| RAS# hold time | tRSH | 15 | | 20 | | ns | 36 |
| READ WRITE cycle time | tRWC | 155 | | 180 | | ns | |
| RAS# to WE# delay time | tRWD | 85 | | 95 | | ns | 18 |
| Write command to RAS# lead time | tRWL | 15 | | 20 | | ns | |
| Transition time (rise or fall) | tT | 2 | 50 | 2 | 50 | ns | |
| Write command hold time | tWCH | 10 | | 12 | | ns | 36 |
| Write command hold time (referenced to RAS#) | tWCR | 45 | | 55 | | ns | |
| WE# command setup time | tWCS | 0 | | 0 | | ns | 18, 27 |
| Write command pulse width | tWP | 10 | | 15 | | ns | |
| WE# hold time (CBR Refresh) | tWRH | 10 | | 10 | | ns | |
| WE# setup time (CBR Refresh) | tWRP | 10 | | 10 | | ns | |

*3.3V only

## NOTES

1. All voltages referenced to $V_{SS}$.
2. This parameter is sampled. $V_{CC}$ = +3V; f = 1 MHz.
3. $I_{CC}$ is dependent on output loading. Specified values are obtained with minimum cycle time and the output open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is ensured.
6. An initial pause of 100µs is required after power-up, followed by eight RAS# refresh cycles (RAS#-ONLY or CBR), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the $^tREF$ refresh requirement is exceeded.
7. AC characteristics assume $^tT$ = 5ns.
8. $V_{IH}$ (MIN) and $V_{IL}$ (MAX) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$).
9. In addition to meeting the transition rate specification, all input signals must transit between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) in a monotonic manner.
10. If CAS# = $V_{IH}$, data output is High-Z.
11. If CAS# = $V_{IL}$, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates, 100pF and $V_{OL}$ = 0.8V and $V_{OH}$ = 2V.
13. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, CAS# must be pulsed HIGH for $^tCP$.
14. The $^tRCD$ (MAX) limit is no longer specified. $^tRCD$ (MAX) was specified as a reference point only. If $^tRCD$ was greater than the specified $^tRCD$ (MAX) limit, then access time was controlled exclusively by $^tCAC$ ($^tRAC$ [MIN] no longer applied). With or without the $^tRCD$ limit, $^tAA$ and $^tCAC$ must always be met.
15. The $^tRAD$ (MAX) limit is no longer specified. $^tRAD$ (MAX) was specified as a reference point only. If $^tRAD$ was greater than the specified $^tRAD$ (MAX) limit, then access time was controlled exclusively by $^tAA$ ($^tRAC$ and $^tCAC$ no longer applied). With or without the $^tRAD$ (MAX) limit, $^tAA$, $^tRAC$ and $^tCAC$ must always be met.
16. Either $^tRCH$ or $^tRRH$ must be satisfied for a READ cycle.
17. $^tOFF$ (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to $V_{OH}$ or $V_{OL}$.
18. $^tWCS$, $^tRWD$, $^tAWD$ and $^tCWD$ are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge ^tWCS$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge ^tRWD$ (MIN), $^tAWD \ge ^tAWD$ (MIN) and $^tCWD \ge ^tCWD$ (MIN), the cycle is a READ WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until CAS# or OE# goes back to $V_{IH}$) is indeterminate. OE# held HIGH and WE# taken LOW after CAS# goes LOW result in a LATE WRITE (OE#-controlled) cycle.
19. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
20. During a READ cycle, if OE# is LOW then taken HIGH before CAS# goes HIGH, Q goes open. If OE# is tied permanently LOW, LATE WRITE and READ-MODIFY-WRITE operations are not permissible and should not be attempted.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# = LOW and OE# = HIGH.
22. All other inputs at 0.2V or $V_{CC}$ -0.2V.
23. Column address changed once each cycle.
24. LATE WRITE and READ-MODIFY-WRITE cycles must have both $^tOD$ and $^tOEH$ met (OE# HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS# remains LOW and OE# is taken back LOW after $^tOEH$ is met. If CAS# goes HIGH prior to OE# going back LOW, the DQs will remain open.
25. The DQs open during READ cycles once $^tOD$ or $^tOFF$ occur.
26. The 3ns minimum is a parameter guaranteed by design.
27. The first CASx edge to transition LOW.
28. The last CASx edge to transition HIGH.
29. Output parameter (DQx) is referenced to corresponding CAS# input; DQ1-DQ8 by CASL# and DQ9-DQ16 by CASH#.
30. Last falling CASx edge to first rising CASx edge.
31. Last rising CASx edge to next cycle's last rising CASx edge.
32. Last rising CASx edge to first falling CASx edge.
33. First DQs controlled by the first CASx to go LOW.
34. Last DQs controlled by the last CASx to go HIGH.
35. Each CASx must meet minimum pulse width.
36. Last CASx to go LOW.
37. All DQs controlled, regardless CASL# and CASH#.

## READ CYCLE

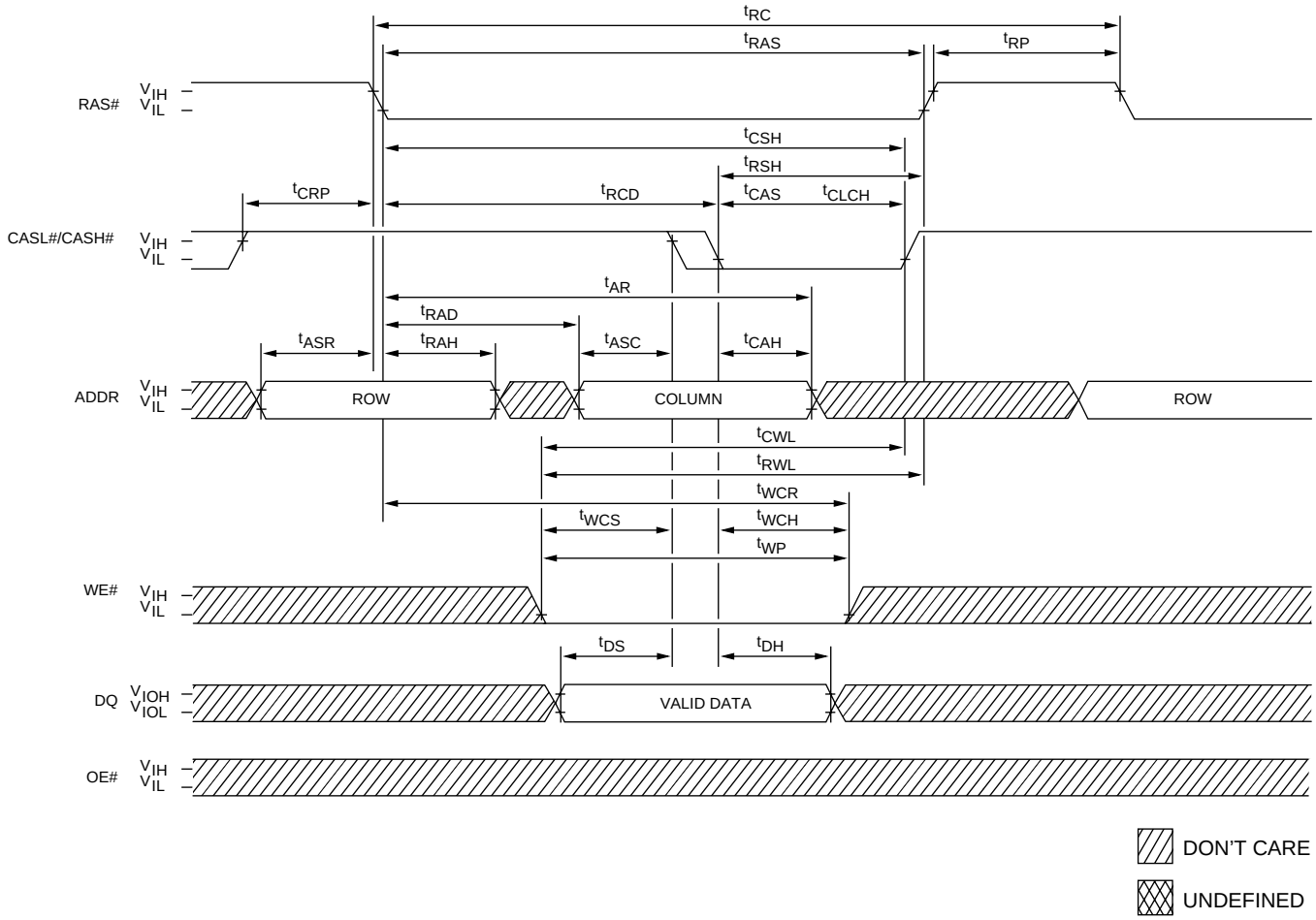



### TIMING PARAMETERS

| SYMBOL | -6 MIN | -6 MAX | -7 MIN | -7 MAX | UNITS |
|---|---|---|---|---|---|
| tAA | | 30 | | 35 | ns |
| tAR | 45 | | 55 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAC | | 15 | | 20 | ns |
| tCAH | 10 | | 12 | | ns |
| tCAS | 15 | 10,000 | 20 | 10,000 | ns |
| tCLCH | 10 | | 10 | | ns |
| tCLZ | 3 | | 3 | | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 60 | | 70 | | ns |
| tOD | 3 | 15 | 3 | 20 | ns |
| tOE | | 15 | | 20 | ns |

| SYMBOL | -6 MIN | -6 MAX | -7 MIN | -7 MAX | UNITS |
|---|---|---|---|---|---|
| tOFF | 3 | 15 | 3 | 20 | ns |
| tRAC | | 60 | | 70 | ns |
| tRAD | 15 | | 15 | | ns |
| tRAH | 10 | | 10 | | ns |
| tRAS | 60 | 10,000 | 70 | 10,000 | ns |
| tRC | 110 | | 130 | | ns |
| tRCD | 20 | | 20 | | ns |
| tRCH | 0 | | 0 | | ns |
| tRCS | 0 | | 0 | | ns |
| tRP | 40 | | 50 | | ns |
| tRRH | 0 | | 0 | | ns |
| tRSH | 15 | | 20 | | ns |

## EARLY WRITE CYCLE

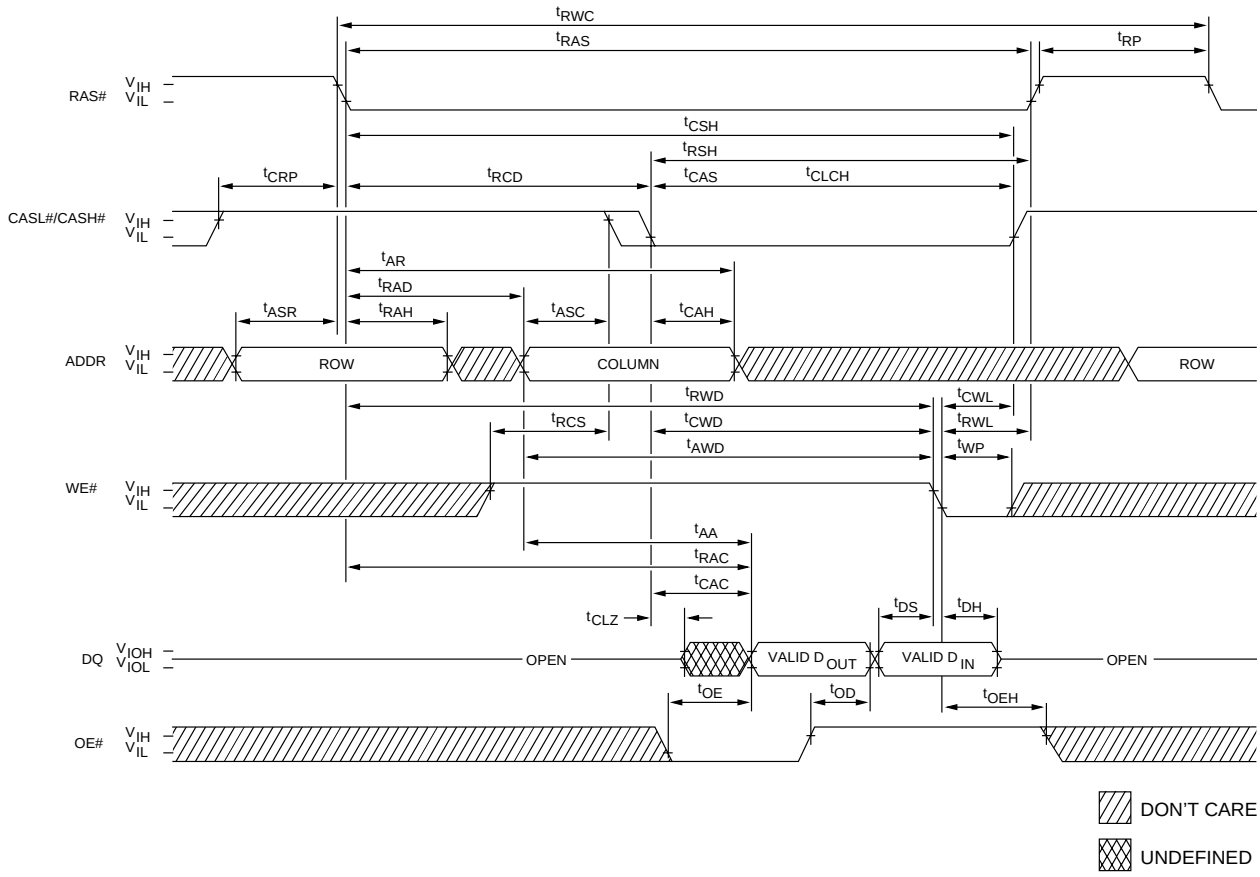



### TIMING PARAMETERS

| SYMBOL | -6 MIN | -6 MAX | -7 MIN | -7 MAX | UNITS |
|---|---|---|---|---|---|
| tAR | 45 | | 55 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAH | 10 | | 12 | | ns |
| tCAS | 15 | 10,000 | 20 | 10,000 | ns |
| tCLCH | 10 | | 10 | | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 60 | | 70 | | ns |
| tCWL | 15 | | 20 | | ns |
| tDH | 10 | | 12 | | ns |
| tDS | 0 | | 0 | | ns |
| tRAD | 15 | | 15 | | ns |

| SYMBOL | -6 MIN | -6 MAX | -7 MIN | -7 MAX | UNITS |
|---|---|---|---|---|---|
| tRAH | 10 | | 10 | | ns |
| tRAS | 60 | 10,000 | 70 | 10,000 | ns |
| tRC | 110 | | 130 | | ns |
| tRCD | 20 | | 20 | | ns |
| tRP | 40 | | 50 | | ns |
| tRSH | 15 | | 20 | | ns |
| tRWL | 15 | | 20 | | ns |
| tWCH | 10 | | 12 | | ns |
| tWCR | 45 | | 55 | | ns |
| tWCS | 0 | | 0 | | ns |
| tWP | 10 | | 15 | | ns |

## READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)

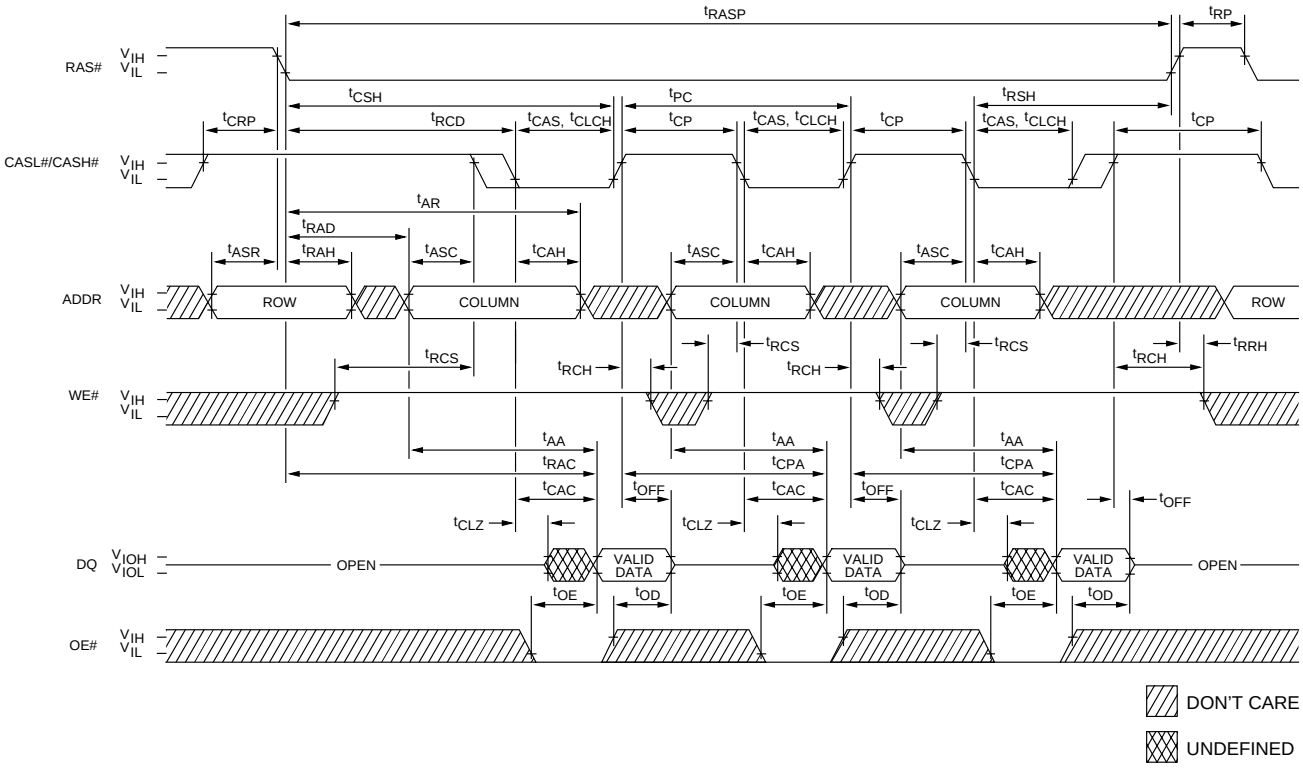



### TIMING PARAMETERS

| SYMBOL | -6 MIN | -6 MAX | -7 MIN | -7 MAX | UNITS |
|---|---|---|---|---|---|
| tAA | | 30 | | 35 | ns |
| tAR | 45 | | 55 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tAWD | 55 | | 60 | | ns |
| tCAC | | 15 | | 20 | ns |
| tCAH | 10 | | 12 | | ns |
| tCAS | 15 | 10,000 | 20 | 10,000 | ns |
| tCLCH | 10 | | 10 | | ns |
| tCLZ | 3 | | 3 | | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 60 | | 70 | | ns |
| tCWD | 40 | | 45 | | ns |
| tCWL | 15 | | 20 | | ns |
| tDH | 10 | | 12 | | ns |
| tDS | 0 | | 0 | | ns |

| SYMBOL | -6 MIN | -6 MAX | -7 MIN | -7 MAX | UNITS |
|---|---|---|---|---|---|
| tOD | 3 | 15 | 3 | 20 | ns |
| tOE | | 15 | | 20 | ns |
| tOEH | 15 | | 20 | | ns |
| tRAC | | 60 | | 70 | ns |
| tRAD | 15 | | 15 | | ns |
| tRAH | 10 | | 10 | | ns |
| tRAS | 60 | 10,000 | 70 | 10,000 | ns |
| tRCD | 20 | | 20 | | ns |
| tRCS | 0 | | 0 | | ns |
| tRP | 40 | | 50 | | ns |
| tRSH | 15 | | 20 | | ns |
| tRWC | 155 | | 180 | | ns |
| tRWD | 85 | | 95 | | ns |
| tRWL | 15 | | 20 | | ns |
| tWP | 10 | | 15 | | ns |

## FAST-PAGE-MODE READ CYCLE

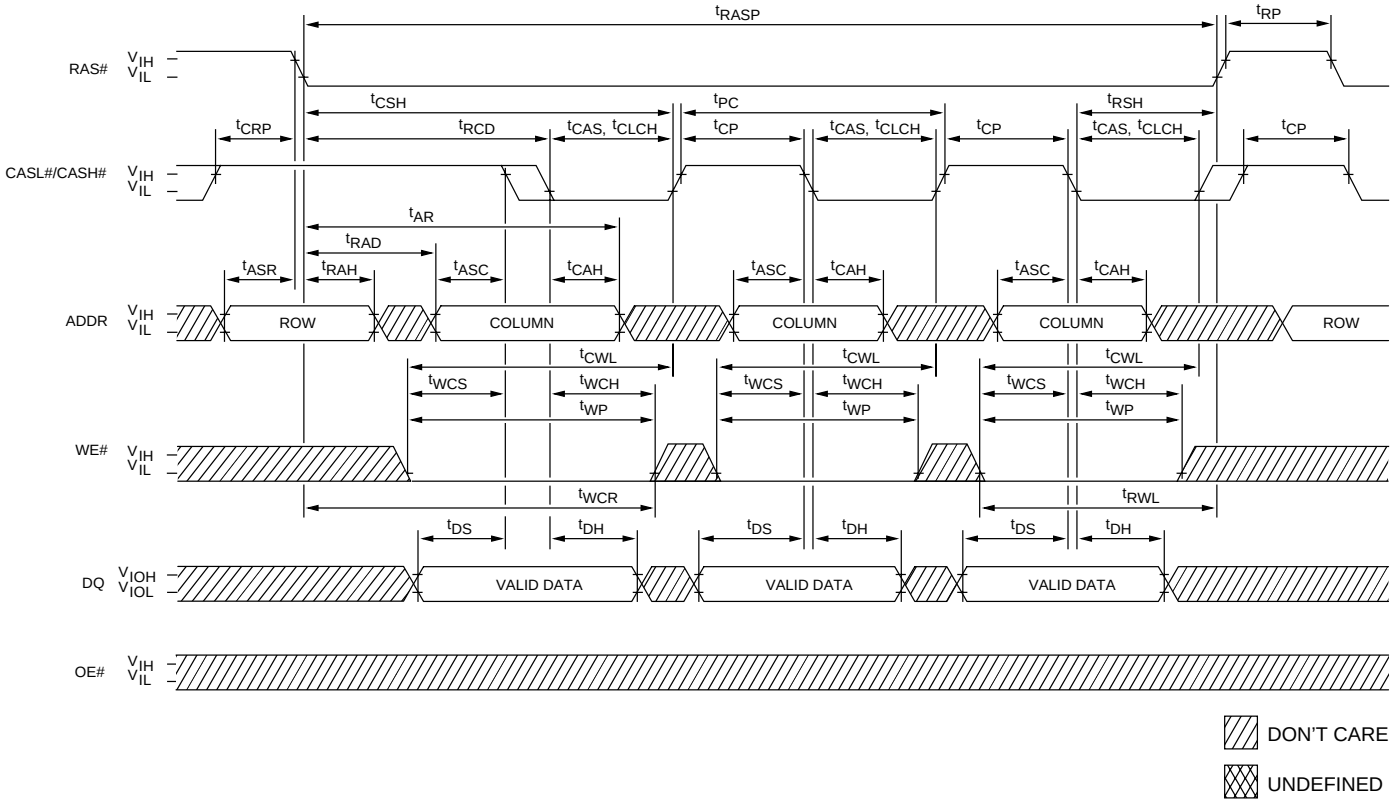



### TIMING PARAMETERS

| SYMBOL | -6 MIN | -6 MAX | -7 MIN | -7 MAX | UNITS |
|---|---|---|---|---|---|
| tAA | | 30 | | 35 | ns |
| tAR | 45 | | 55 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAC | | 15 | | 20 | ns |
| tCAH | 10 | | 12 | | ns |
| tCAS | 15 | 10,000 | 20 | 10,000 | ns |
| tCLCH | 10 | | 10 | | ns |
| tCLZ | 3 | | 3 | | ns |
| tCP | 10 | | 10 | | ns |
| tCPA | | 35 | | 40 | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 60 | | 70 | | ns |
| tOD | 3 | 15 | 3 | 20 | ns |

| SYMBOL | -6 MIN | -6 MAX | -7 MIN | -7 MAX | UNITS |
|---|---|---|---|---|---|
| tOE | | 15 | | 20 | ns |
| tOFF | 3 | 15 | 3 | 20 | ns |
| tPC | 35 | | 40 | | ns |
| tRAC | | 60 | | 70 | ns |
| tRAD | 15 | | 15 | | ns |
| tRAH | 10 | | 10 | | ns |
| tRASP | 60 | 125,000 | 70 | 125,000 | ns |
| tRCD | 20 | | 20 | | ns |
| tRCH | 0 | | 0 | | ns |
| tRCS | 0 | | 0 | | ns |
| tRP | 40 | | 50 | | ns |
| tRRH | 0 | | 0 | | ns |
| tRSH | 15 | | 20 | | ns |

## FAST-PAGE-MODE EARLY-WRITE CYCLE

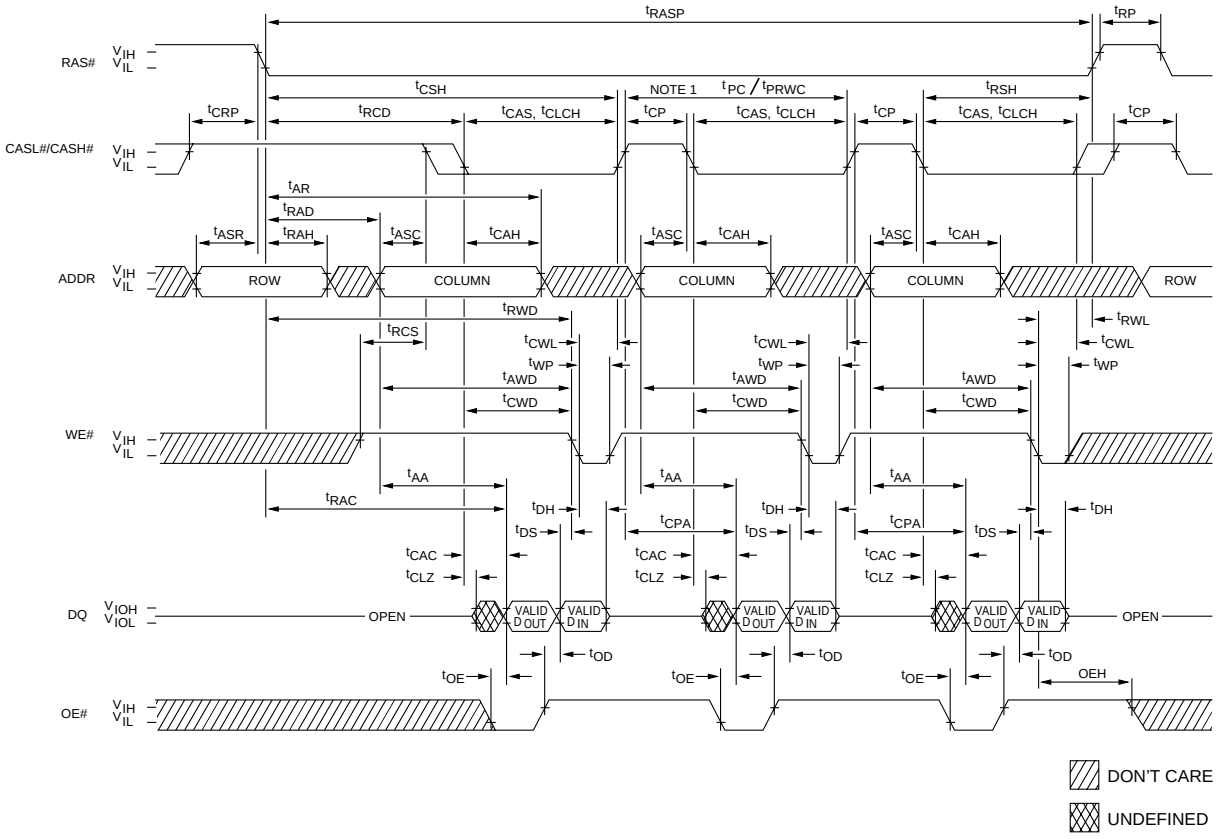



### TIMING PARAMETERS

| SYMBOL | -6 MIN | -6 MAX | -7 MIN | -7 MAX | UNITS |
|---|---|---|---|---|---|
| tAR | 45 | | 55 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAH | 10 | | 12 | | ns |
| tCAS | 15 | 10,000 | 20 | 10,000 | ns |
| tCLCH | 10 | | 10 | | ns |
| tCP | 10 | | 10 | | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 60 | | 70 | | ns |
| tCWL | 15 | | 20 | | ns |
| tDH | 10 | | 12 | | ns |
| tDS | 0 | | 0 | | ns |

| SYMBOL | -6 MIN | -6 MAX | -7 MIN | -7 MAX | UNITS |
|---|---|---|---|---|---|
| tPC | 35 | | 40 | | ns |
| tRAD | 15 | | 15 | | ns |
| tRAH | 10 | | 10 | | ns |
| tRASP | 60 | 125,000 | 70 | 125,000 | ns |
| tRCD | 20 | | 20 | | ns |
| tRP | 40 | | 50 | | ns |
| tRSH | 15 | | 20 | | ns |
| tRWL | 15 | | 20 | | ns |
| tWCH | 10 | | 12 | | ns |
| tWCR | 45 | | 55 | | ns |
| tWCS | 0 | | 0 | | ns |
| tWP | 10 | | 15 | | ns |

## FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



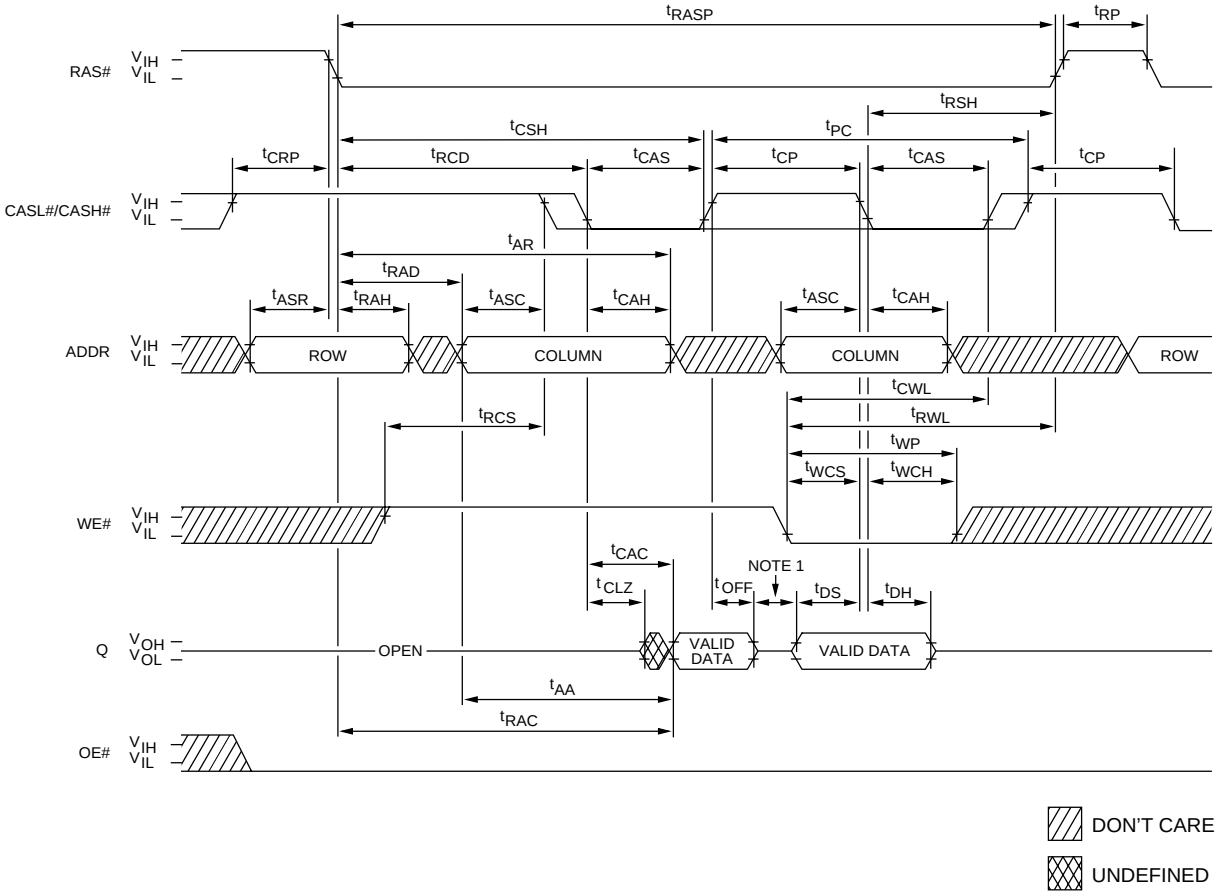

### TIMING PARAMETERS

| SYMBOL | -6 MIN | -6 MAX | -7 MIN | -7 MAX | UNITS |
|---|---|---|---|---|---|
| tAA | | 30 | | 35 | ns |
| tAR | 45 | | 55 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tAWD | 55 | | 60 | | ns |
| tCAC | | 15 | | 20 | ns |
| tCAH | 10 | | 12 | | ns |
| tCAS | 15 | 10,000 | 20 | 10,000 | ns |
| tCLCH | 10 | | 10 | | ns |
| tCLZ | 3 | | 3 | | ns |
| tCP | 10 | | 10 | | ns |
| tCPA | | 35 | | 40 | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 60 | | 70 | | ns |
| tCWD | 40 | | 45 | | ns |
| tCWL | 15 | | 20 | | ns |
| tDH | 10 | | 12 | | ns |

| SYMBOL | -6 MIN | -6 MAX | -7 MIN | -7 MAX | UNITS |
|---|---|---|---|---|---|
| tDS | 0 | | 0 | | ns |
| tOD | 3 | 15 | 3 | 20 | ns |
| tOE | | 15 | | 20 | ns |
| tOEH | 15 | | 20 | | ns |
| tPC | 35 | | 40 | | ns |
| tPRWC | 85 | | 95 | | ns |
| tRAC | | 60 | | 70 | ns |
| tRAD | 15 | | 15 | | ns |
| tRAH | 10 | | 10 | | ns |
| tRASP | 60 | 125,000 | 70 | 125,000 | ns |
| tRCD | 20 | | 20 | | ns |
| tRCS | 0 | | 0 | | ns |
| tRP | 40 | | 50 | | ns |
| tRSH | 15 | | 20 | | ns |
| tRWD | 85 | | 95 | | ns |
| tRWL | 15 | | 20 | | ns |
| tWP | 10 | | 15 | | ns |

**NOTE:** 1. tPC is for LATE WRITE only.

## FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)




### TIMING PARAMETERS

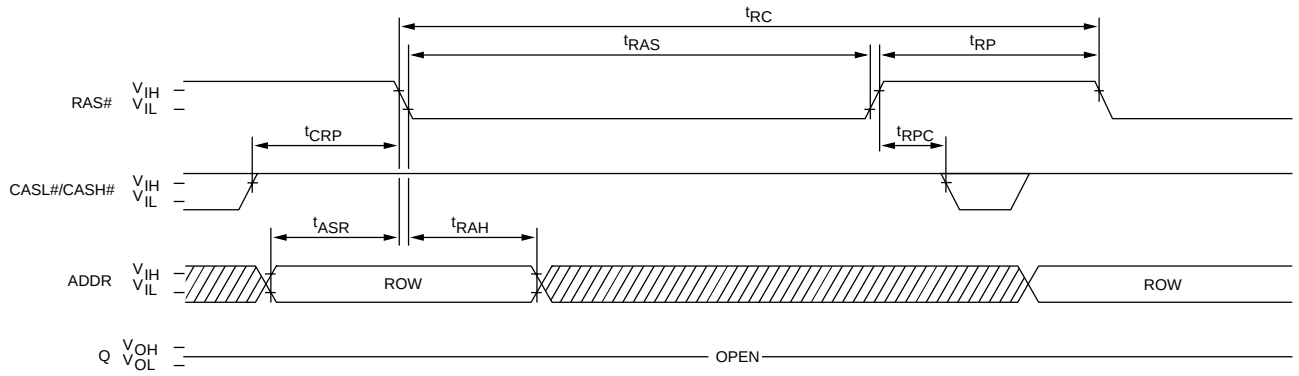
| SYMBOL | -6 MIN | -6 MAX | -7 MIN | -7 MAX | UNITS |
|---|---|---|---|---|---|
| tAA | | 30 | | 35 | ns |
| tAR | 45 | | 55 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAC | | 15 | | 20 | ns |
| tCAH | 10 | | 12 | | ns |
| tCAS | 15 | 10,000 | 20 | 10,000 | ns |
| tCLZ | 3 | | 3 | | ns |
| tCP | 10 | | 10 | | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 60 | | 70 | | ns |
| tCWL | 15 | | 20 | | ns |
| tDH | 10 | | 12 | | ns |
| tDS | 0 | | 0 | | ns |

| SYMBOL | -6 MIN | -6 MAX | -7 MIN | -7 MAX | UNITS |
|---|---|---|---|---|---|
| tOFF | 3 | 15 | 3 | 20 | ns |
| tPC | 35 | | 40 | | ns |
| tRAC | | 60 | | 70 | ns |
| tRAD | 15 | | 15 | | ns |
| tRAH | 10 | | 10 | | ns |
| tRASP | 60 | 125,000 | 70 | 125,000 | ns |
| tRCD | 20 | | 20 | | ns |
| tRCS | 0 | | 0 | | ns |
| tRP | 40 | | 50 | | ns |
| tRSH | 15 | | 20 | | ns |
| tRWL | 15 | | 20 | | ns |
| tWCH | 10 | | 12 | | ns |
| tWCS | 0 | | 0 | | ns |
| tWP | 10 | | 15 | | ns |

**NOTE:** 1. tPC is for LATE WRITE only.

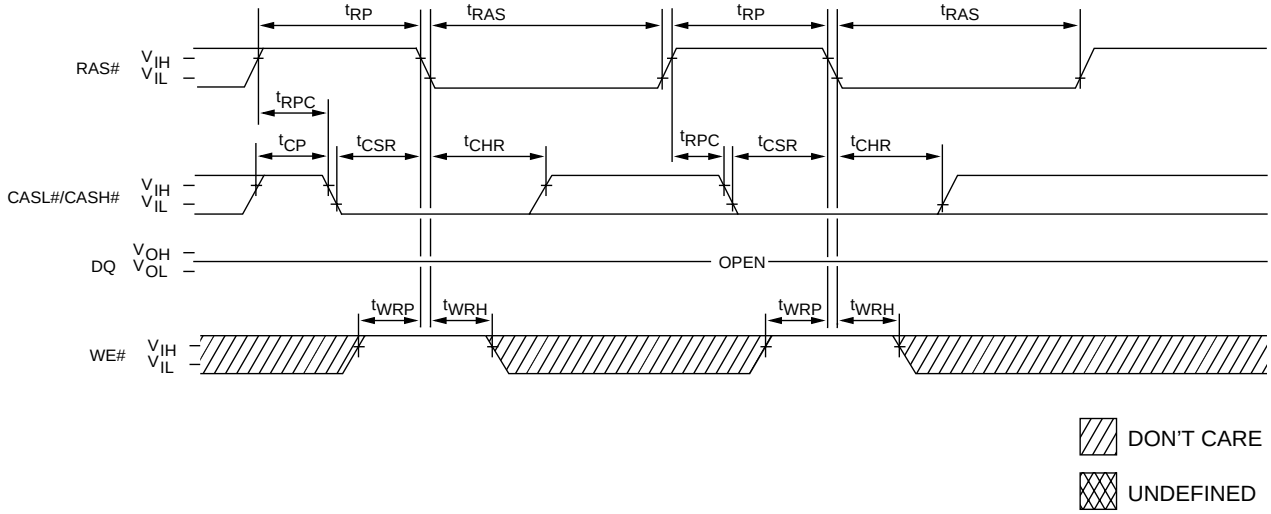
## RAS#-ONLY REFRESH CYCLE

(OE# and WE# = DON'T CARE)




## CBR REFRESH CYCLE

(Addresses and OE# = DON'T CARE)

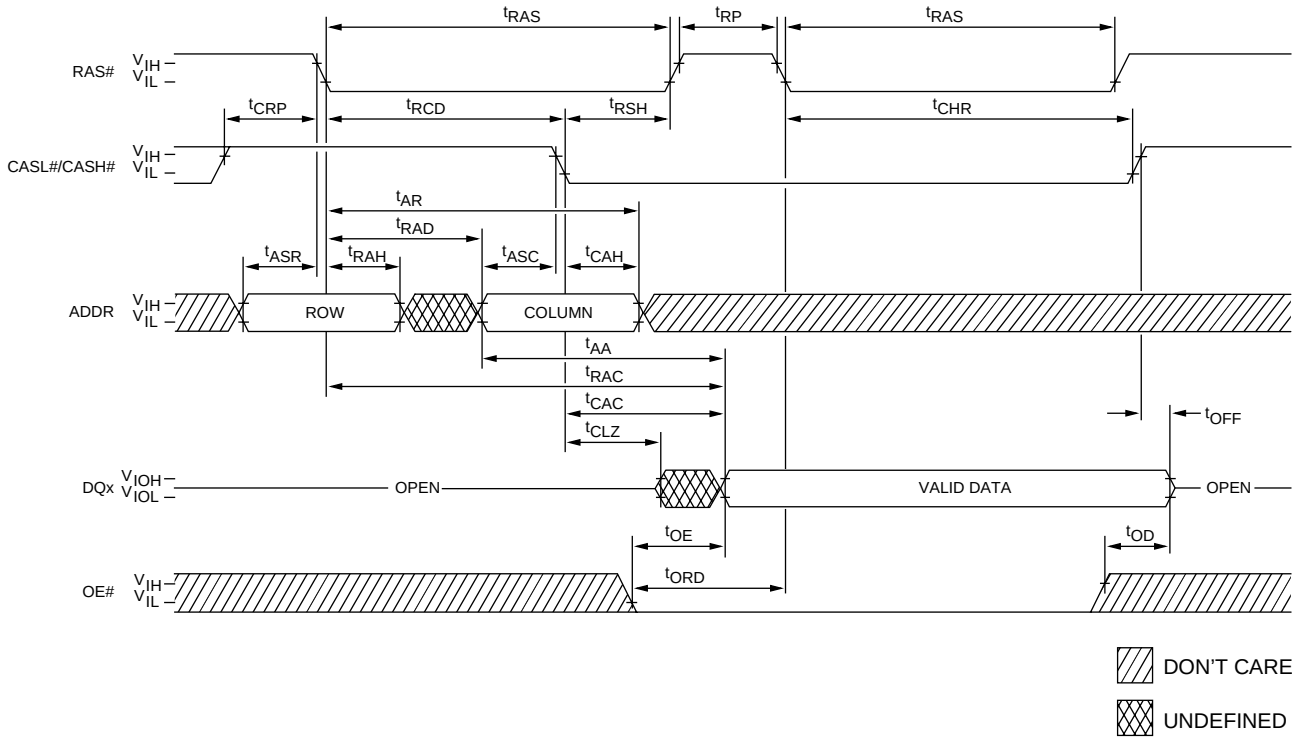



### TIMING PARAMETERS

| SYMBOL | -6 MIN | -6 MAX | -7 MIN | -7 MAX | UNITS |
|---|---|---|---|---|---|
| tASR | 0 | | 0 | | ns |
| tCHR | 10 | | 15 | | ns |
| tCP | 10 | | 10 | | ns |
| tCRP | 5 | | 5 | | ns |
| tCSR | 5 | | 5 | | ns |
| tRAH | 10 | | 10 | | ns |

| SYMBOL | -6 MIN | -6 MAX | -7 MIN | -7 MAX | UNITS |
|---|---|---|---|---|---|
| tRAS | 60 | 10,000 | 70 | 10,000 | ns |
| tRC | 110 | | 130 | | ns |
| tRP | 40 | | 50 | | ns |
| tRPC | 0 | | 0 | | ns |
| tWRH | 10 | | 10 | | ns |
| tWRP | 10 | | 10 | | ns |

## HIDDEN REFRESH CYCLE [21]
(WE# = HIGH; OE# = LOW)

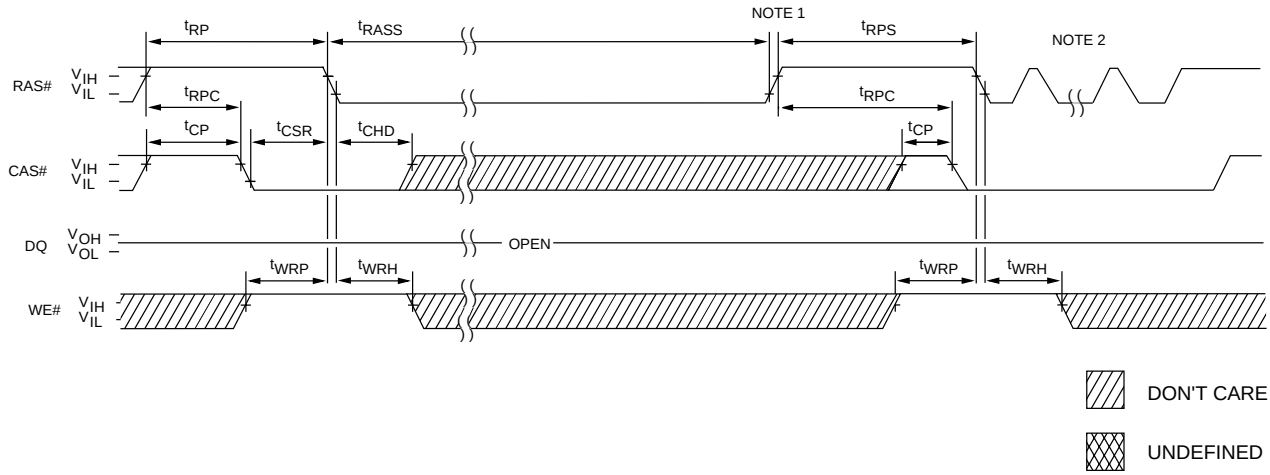



### TIMING PARAMETERS

| SYMBOL | -6 MIN | -6 MAX | -7 MIN | -7 MAX | UNITS |
|---|---|---|---|---|---|
| tAA | | 30 | | 35 | ns |
| tAR | 45 | | 55 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAC | | 15 | | 20 | ns |
| tCAH | 10 | | 12 | | ns |
| tCHR | 10 | | 15 | | ns |
| tCLZ | 3 | | 3 | | ns |
| tCRP | 5 | | 5 | | ns |
| tOD | 3 | 15 | 3 | 20 | ns |

| SYMBOL | -6 MIN | -6 MAX | -7 MIN | -7 MAX | UNITS |
|---|---|---|---|---|---|
| tOE | | 15 | | 20 | ns |
| tOFF | 3 | 15 | 3 | 20 | ns |
| tORD | 0 | | 0 | | ns |
| tRAC | | 60 | | 70 | ns |
| tRAD | 15 | | 15 | | ns |
| tRAH | 10 | | 10 | | ns |
| tRAS | 60 | 10,000 | 70 | 10,000 | ns |
| tRCD | 20 | | 20 | | ns |
| tRP | 40 | | 50 | | ns |
| tRSH | 15 | | 20 | | ns |

## SELF REFRESH CYCLE
(Addresses and OE# = DON'T CARE)




### TIMING PARAMETERS

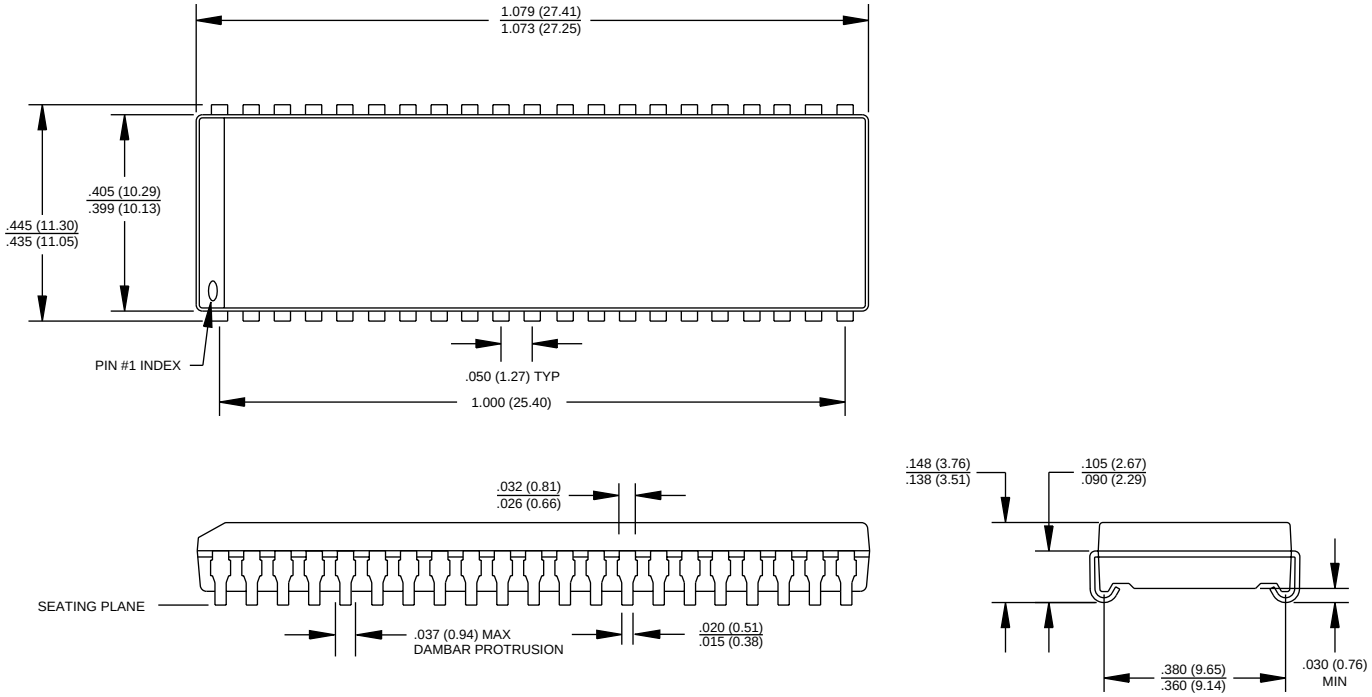
| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | UNITS |
| tCHD | 15 | | 15 | | ns |
| tCLCH | 10 | | 10 | | ns |
| tCP | 10 | | 10 | | ns |
| tCSR | 5 | | 5 | | ns |
| tRASS | 100 | | 100 | | µs |

| | -6 | | -7 | | |
|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | UNITS |
| tRP | 40 | | 50 | | ns |
| tRPC | 0 | | 0 | | ns |
| tRPS | 110 | | 130 | | ns |
| tWRH | 10 | | 10 | | ns |
| tWRP | 10 | | 10 | | ns |

**NOTE:**
1. Once tRASS (MIN) is met and RAS# remains LOW, the DRAM will enter Self Refresh mode.
2. Once tRPS is satisfied, a complete burst of all rows should be executed.

## 42-PIN PLASTIC SOJ (400 mil)

DA-7

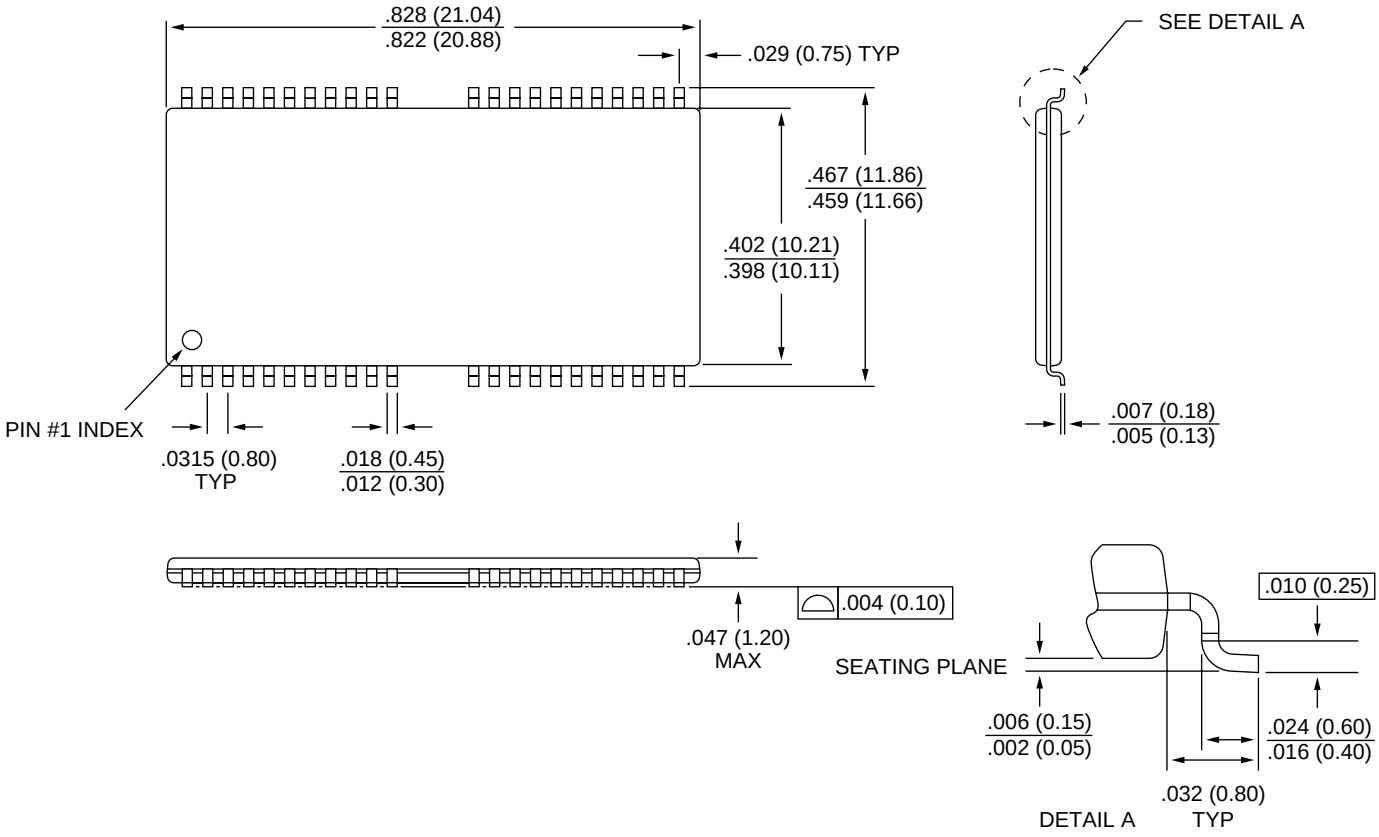



**NOTE:** 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

## 44/50-PIN PLASTIC TSOP (400 mil)

DB-6




**NOTE:** 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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