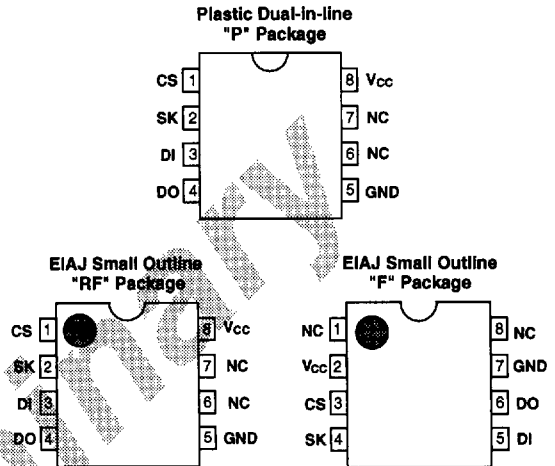


### FEATURES

- 1.8V to 5.5V Operation
- Extended Temperature Range: -40°C to +85°C
- State-of-the-Art Architecture
  - Nonvolatile data storage
  - CMOS compatible inputs and outputs
  - Auto Increment for efficient data dump
- Hardware and Software Write Protection
  - Defaults to write-disabled state at power up
  - Software instructions for write-enable/disable
  - Vcc lockout inadvertent write protection
- Low Power Consumption
  - 3mA active current
  - 3µA standby current
- Advanced Low Voltage CMOS E<sup>2</sup>PROM Technology
- Versatile, Easy-to-Use Interface
  - Self-timed programming cycle
  - Automatic erase-before-write
  - Programming Status Indicator
- Durable and Reliable
  - Minimum of 100,000 write cycles per word
  - Typical 1,000,000 write cycles per word
  - 10-year data retention after 100K write cycles
  - Unlimited read cycles
  - ESD protection (EIAJ and JEDEC standard)

### PIN CONFIGURATIONS



### PIN NAMES

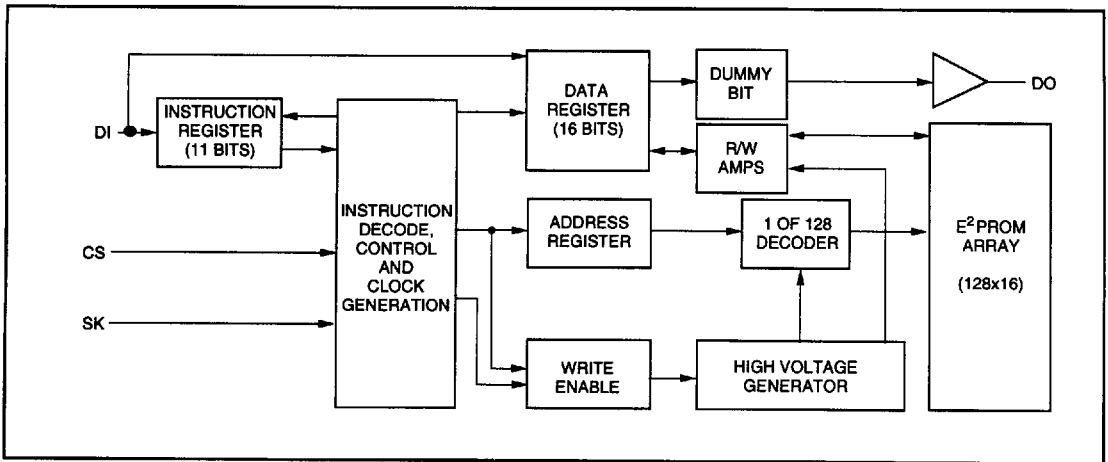
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply
NC	Not Connected

### OVERVIEW

The XL93LL56 is a low voltage 2,048-bit, nonvolatile, serial E<sup>2</sup>PROM. It is fabricated using EXEL's advanced CMOS E<sup>2</sup>PROM technology. The XL93LL56 provides efficient nonvolatile read/write memory arranged as 128 registers of 16 bits each. Four 11-bit instructions control the operation of the device, which include read, write, write disable and write enable functions. The data output pin (DO) indicates the status of the device during the self-timed nonvolatile programming cycle.

The self-timed write cycle includes an automatic erase-before-write capability. To protect against inadvertent writes, the WRITE instruction is accepted only while the chip is in the write enabled state. Data is written in 16 bits per write instruction into the selected register. If Chip Select (CS) is brought HIGH after initiation of the write cycle, the Data Output (DO) pin will indicate the READY/BUSY status of the chip.

### BLOCK DIAGRAM



### APPLICATIONS

The XL93LL56 is ideal for high volume applications requiring low voltage and low density storage. This device uses a cost effective, space saving 8-pin package. Candidate applications include robotics, alarm devices, electronic locks, cameras, pagers, cordless phones and instrumentation settings.

### ENDURANCE AND DATA RETENTION

The XL93LL56 is designed for applications requiring up to 100,000 write cycles per bit. It provides 10 years of secure data retention without power after the execution of 100,000 write cycles for each location.

### DEVICE OPERATION

The XL93LL56 is controlled by four 11-bit instructions. Instructions are clocked in (serially) on the DI pin. Each instruction begins with a logical "1" (the start bit). This is followed by the opcode (2 bits), the address field (8 bits, the most significant bit being "don't care"), and data, if appropriate. The clock signal (SK) may be halted at any time and the XL93LL56 will remain in its last state. This allows full static flexibility and maximum power conservation.

### Read (READ)

The READ instruction is the only instruction that results in serial data on the DO pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into a 16-bit serial shift register. (Please note the dummy "0" bit precedes the actual 16-bit output data string.) The output on DO changes during the LOW-TO-HIGH transitions of SK. (See Figure 2.)

### Auto Increment Read Operations

In order to facilitate memory transfer operations, the XL93LL56 has been designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 16 bits of the addressed word have been clocked out, the data in consecutively higher address locations is output. The address will wrap around continuously with CS HIGH until the Chip Select control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

### Write Enable (WEN)

The write enable (WEN) instruction must be executed before any device programming can be done. When V<sub>CC</sub> is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter the device remains enabled until a WDS instruction is executed or until V<sub>CC</sub> is removed. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction. See Figure 3.)

### Write (WRITE)

The WRITE instruction includes 16 bits of data to be written into the specified register. After the last data bit has been clocked into DI, and before the next rising edge of SK, CS must be brought LOW. The falling edge of CS initiates the self-timed programming cycle.

After a minimum wait of 250ns from the falling edge of CS ( $t_{cs}$ ), if CS is brought HIGH, DO will indicate the READY/BUSY status of the chip: logical "0" means programming is still in progress; logical "1" means the selected register has been written, and the part is ready for another instruction. (See Figure 4.) (NOTE: The combination of CS HIGH, DI HIGH and the rising edge of the SK clock, resets the READY/BUSY flag. Therefore, it is important not to reset the READY/BUSY flag through this combination of control signals, if you want to access it.) Before a WRITE instruction can be executed, the device must be write enabled (see WEN).

### Write Disable (WDS)

The write disable (WDS) instruction disables all programming capabilities. This protects the entire memory array against accidental modification of data until a WEN instruction is executed. (When  $V_{CC}$  is applied, the part powers up in the write disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction. See Figure 5.)

### Vcc Lockout - Inadvertent Write Protection

To ensure against inadvertent write operation, the XL93LL56 has been equipped with an internal  $V_{CC}$  sensor circuit which inhibits data alteration when the supply voltage ( $V_{CC}$ ) falls below  $V_{WL}$ . If the applied  $V_{CC}$  is below 1.45V (typical), the XL93LL56 is inhibited from executing write operations thereby protecting the nonvolatile data from inadvertent write operations.

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**XL93LL56 INSTRUCTION SET**

Instruction	Start Bit	OP Code	Address	Input Data
READ	1	10	X(A6-A0)	
WEN (Write Enable)	1	00	11XXXXXX	
WRITE	1	01	X(A6-A0)	D15-D0
WDS (Write Disable)	1	00	00XXXXXX	

## Preliminary Information

### ABSOLUTE MAXIMUM RATINGS

Temperature under bias .....	-40°C to +85°C
Storage Temperature .....	-65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) .....	300°C
Supply Voltage .....	0 to 7.0V
Voltage on Any Pin .....	-0.3 to $V_{CC} + 0.3V$
ESD Rating .....	2000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may adversely affect device reliability.

### DC ELECTRICAL CHARACTERISTICS

$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 1.8$  to  $5.5V$

Symbol	Parameter	Conditions	Min	Typ.	Max	Units
$V_{CC1}$	Supply Voltage		1.8	5.0	5.5	V
$V_{CC2}$	Supply Voltage		2.5	5.0	5.5	V
$V_{CC3}$	Supply Voltage		4.5	5.0	5.5	V
$I_{CC}$	Supply Current	$V_{CC} = 5.0V$	READ at 1.0MHz		2	mA
			WRITE at 1.0MHz		3	mA
$I_{SB1}$	Standby Current	$V_{CC} = 1.8V$ CS = 0			2	$\mu A$
$I_{SB2}$	Standby Current	$V_{CC} = 2.5V$ CS = 0			2	$\mu A$
$I_{SB3}$	Standby Current	$V_{CC} = 5.0V$ CS = 0			3	$\mu A$
$I_{IL}$	Input Leakage	$V_{IN} = 0V$ TO $V_{CC}$	-1	0.1	1	$\mu A$
$I_{OL}$	Output Leakage	$V_{IN} = 0V$ TO $V_{CC}$	-1	0.1	1	$\mu A$
$V_{IL}$	Input Low Voltage	$1.8V \leq V_{CC} \leq 5.5V$	-0.3		$0.2V_{CC}$ $V_{CC} + 0.3$	V
$V_{IH}$	Input High Voltage		$0.8 V_{CC}$			
$V_{OL}$	Output Low Voltage	$1.8V \leq V_{CC} \leq 5.5V$ $I_{OL} = 1mA, I_{OH} = -10\mu A$	$V_{CC} - 0.3$		0.3	V
$V_{OH}$	Output High Voltage					

### AC ELECTRICAL CHARACTERISTICS

$T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 1.8\text{V}$  to  $5.5\text{V}$

Symbol	Parameter	Conditions	Min	Typ.	Max	Units
$f_{SK}$	SK Clock Frequency	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	0 0 0		1 0.5 0.25	MHz
$t_{SKH}$	SK High Time	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	400 800 1000			ns
$t_{SKL}$	SK Low Time	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	250 500 1000			ns
$t_{CS}$	Minimum CS Low Time	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	250 500 1000			ns
$t_{CSS}$	CS Setup Time	Relative to SK $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	50 100 200			ns
$t_{DIS}$	DI Setup Time	Relative to SK $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	100 200 400			ns
$t_{CSH}$	CS Hold Time	Relative to SK	0			ns
$t_{DIH}$	DI Hold Time	Relative to SK $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	100 200 400			ns
$t_{PD1}$	Output Delay to "1"	AC Test $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$			250 500 2000	ns
$t_{PD0}$	Output Delay to "0"	AC Test $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$			250 500 2000	ns
$t_{SV}$	CS to Status Valid	AC Test $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$			250 500 2000	ns
$t_{DF}$	Impedance	$CS = V_{IL}$ $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$			100 200 400	ns
$t_{WP}$	Write Cycle Time	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$			10 10 10	ms

### CAPACITANCE

$T_A = 25^\circ\text{C}$ ,  $f = 250\text{KHz}$

Symbol	Parameter	Max	Units
$C_{IN}$	Input Capacitance	5	pF
$C_{OUT}$	Output Capacitance	5	pF

