

MOSFET – N-Channel, UniFET™ II

600 V, 17 A, 340 mΩ

FDPF17N60NT

Description

UniFET II MOSFET is onsemi's high voltage MOSFET family based on advanced planar stripe and DMOS technology. This advanced MOSFET family has the smallest on-state resistance among the planar MOSFET, and also provides superior switching performance and higher avalanche energy strength. In addition, internal gate-source ESD diode allows UniFET II MOSFET to withstand over 2 kV HBM surge stress. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

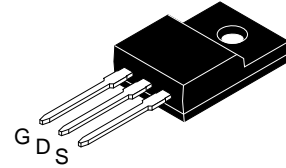
Features

- $R_{DS(on)} = 290 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 8.5 \text{ A}$
- Low Gate Charge (Typ. 48 nC)
- Low C_{rss} (Typ. 23 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- RoHS Compliant

Applications

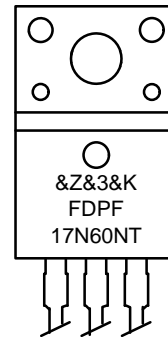
- LCD/LED/PDP TV
- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply

V_{DSS}	$R_{DS(on)}$ MAX	I_D MAX
600 V	340 mΩ @ 10 V	17 A



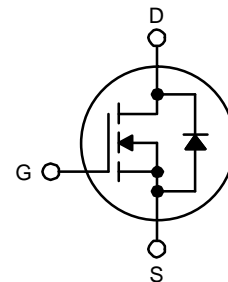
TO-220 Fullpack, 3-Lead / TO-220F-3SG
 CASE 221AT

MARKING DIAGRAM



- &Z = Assembly Plant Code
- &3 = 3-Digit Date Code
- &K = 2-Digits Lot Run Code
- FDPF17N60NT = Specific Device Code

N-CHANNEL MOSFET



ORDERING INFORMATION

Part Number	Package	Shipping
FDPF17N60NT	TO-220F	50 Units / Tube

FDPF17N60NT

MOSFET MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted*)

Symbol	Parameter	FDPF17N60NT	Unit
V_{DSS}	Drain to Source Voltage	600	V
V_{GSS}	Gate to Source Voltage	± 30	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	17*
		- Continuous ($T_C = 100^\circ\text{C}$)	10.2*
I_{DM}	Drain Current	- Pulsed (Note 1)	68*
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	838	mJ
I_{AR}	Avalanche Current (Note 1)	17	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	24.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	10	V/ns
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	62.5
		- Derate Above 25°C	0.5
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $L = 5.8\text{ mH}$, $I_{AS} = 17\text{ A}$, $V_{DD} = 50\text{ V}$, $R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 17\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.

THERMAL CHARACTERISTICS

Symbol	Parameter	FDPF17N60NT	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	2.0	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V, T _C = 25°C	600	–	–	V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	–	0.8	–	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 600 V, V _{GS} = 0 V	–	–	1	μA
		V _{DS} = 480 V, V _{GS} = 0 V, T _C = 150°C	–	–	10	
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±30 V, V _{DS} = 0 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	3.0	–	5.0	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 8.5 A	–	0.29	0.34	Ω
g _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 8.5 A	–	21	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz	–	2285	3040	pF
C _{oss}	Output Capacitance		–	310	410	pF
C _{rss}	Reverse Transfer Capacitance		–	23	35	pF
Q _{g(tot)}	Total Gate Charge at 10 V	V _{DS} = 480 V, I _D = 17 A, V _{GS} = 10 V (Note 4)	–	48	65	nC
Q _{gs}	Gate to Source Gate Charge		–	13	–	nC
Q _{gd}	Gate to Drain "Miller" Charge		–	20	–	nC

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 300 V, I _D = 17 A, V _{GS} = 10 V, R _G = 25 Ω (Note 4)	–	48	106	ns
t _r	Turn-On Rise Time		–	79	168	ns
t _{d(off)}	Turn-Off Delay Time		–	128	266	ns
t _f	Turn-Off Fall Time		–	62	134	ns

DRAIN-SOURCE DIODE CHARACTERISTICS

I _S	Maximum Continuous Drain to Source Diode Forward Current	–	–	74	A	
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current	–	–	68	A	
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 17 A	–	–	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 17 A, dI _F /dt = 100 A/μs	–	575	–	ns
Q _{rr}	Reverse Recovery Charge		–	7.2	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

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TYPICAL PERFORMANCE CHARACTERISTICS

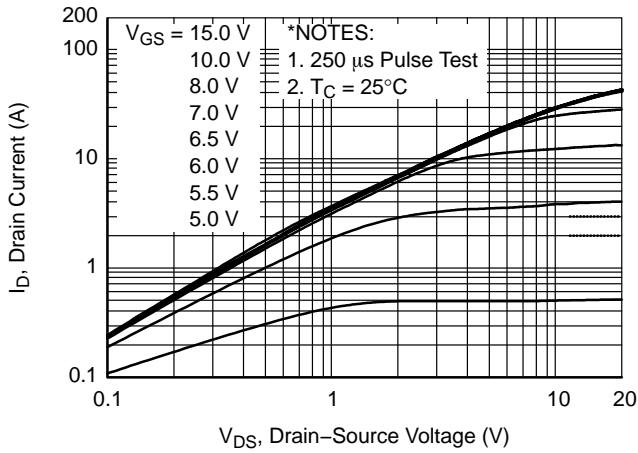


Figure 1. On-Region Characteristics

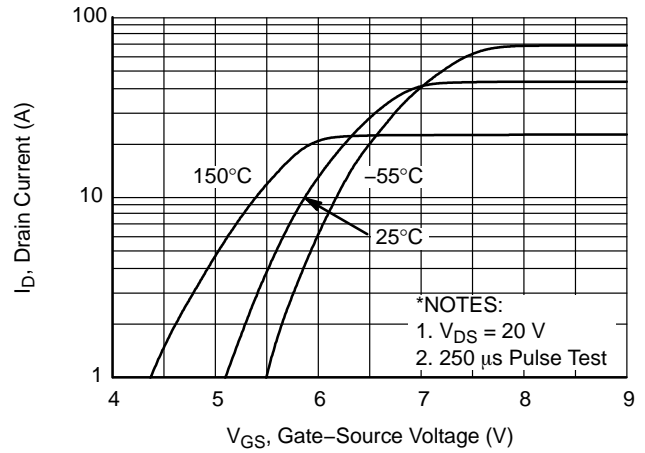


Figure 2. Transfer Characteristics

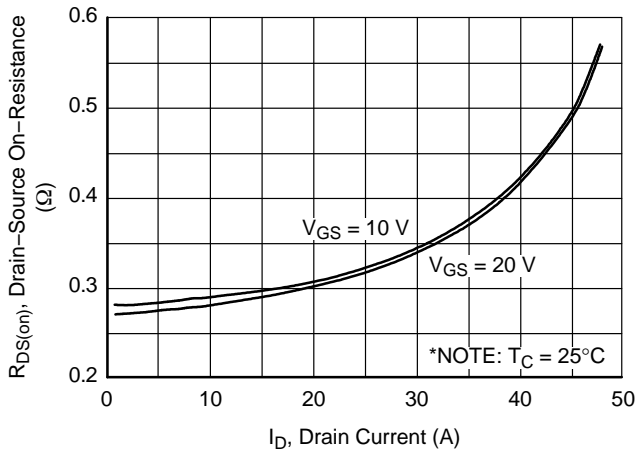


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

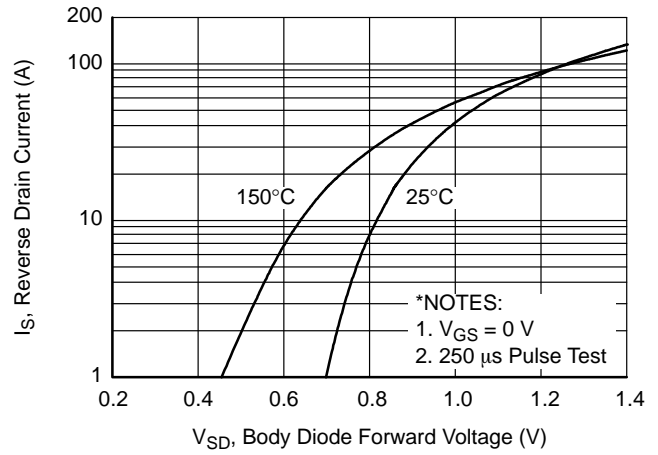


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

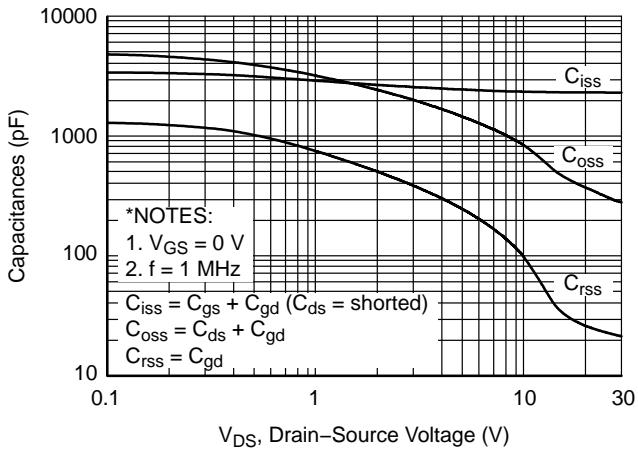


Figure 5. Capacitance Characteristics

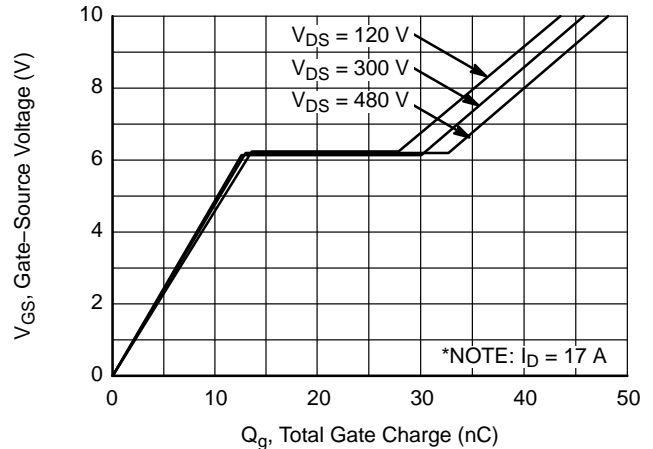


Figure 6. Gate Charge Characteristics

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TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

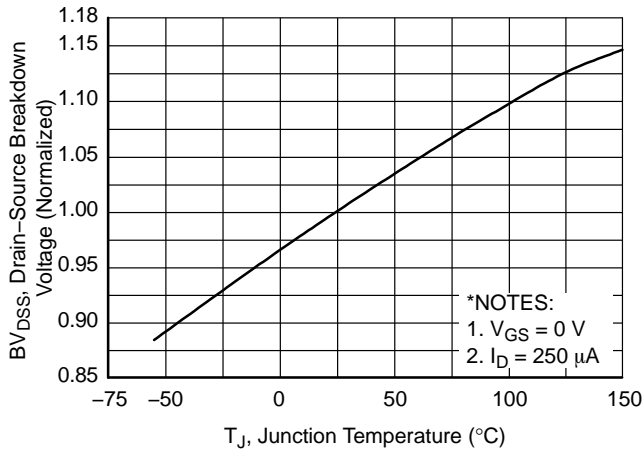


Figure 7. Breakdown Voltage Variation vs. Temperature

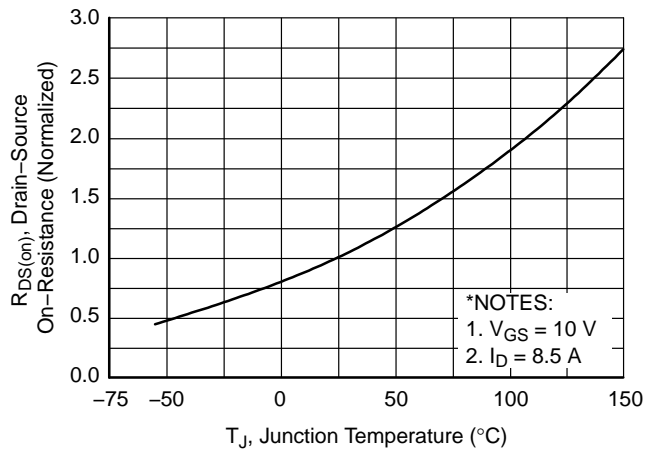


Figure 8. On-Resistance Variation vs. Temperature

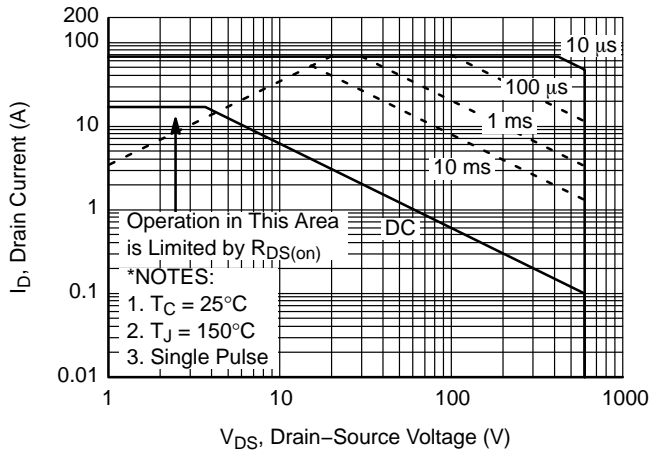


Figure 9. Maximum Safe Operating Area

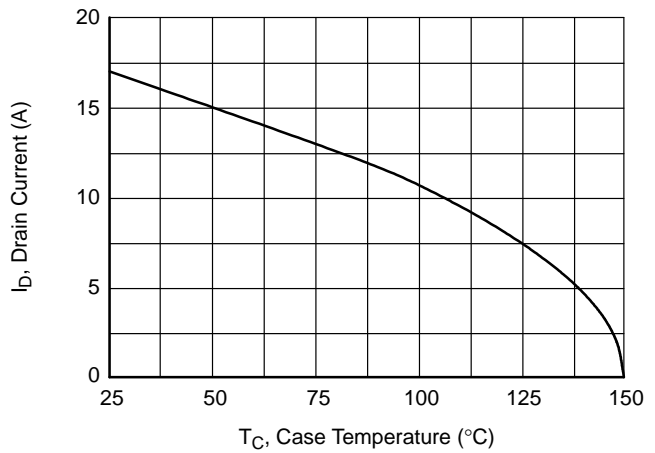


Figure 10. Maximum Drain Current vs. Case Temperature

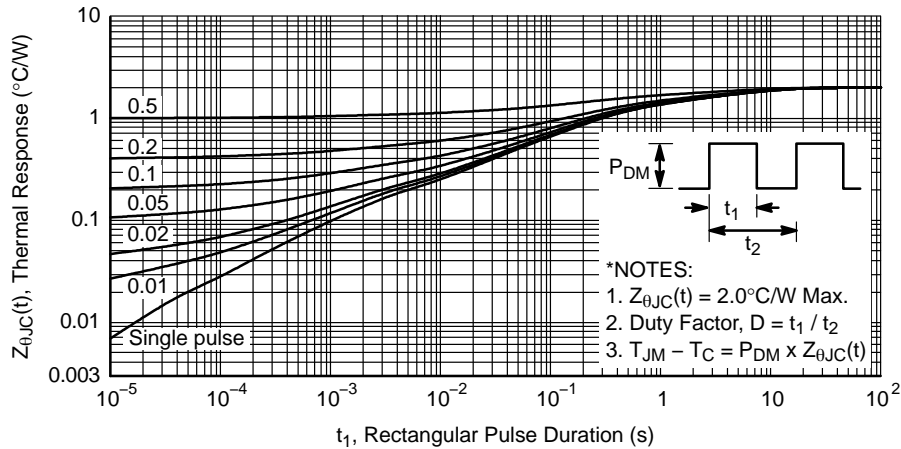


Figure 11. Transient Thermal Response Curve

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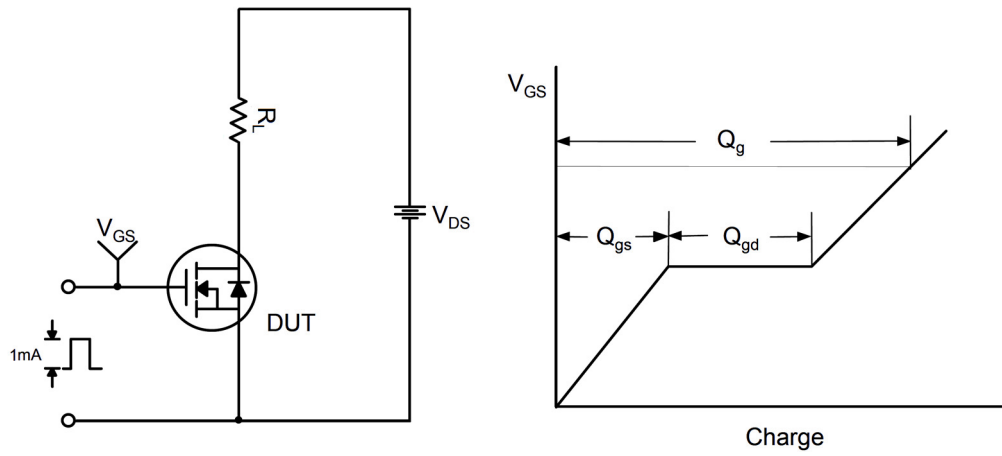


Figure 12. Gate Charge Test Circuit & Waveform

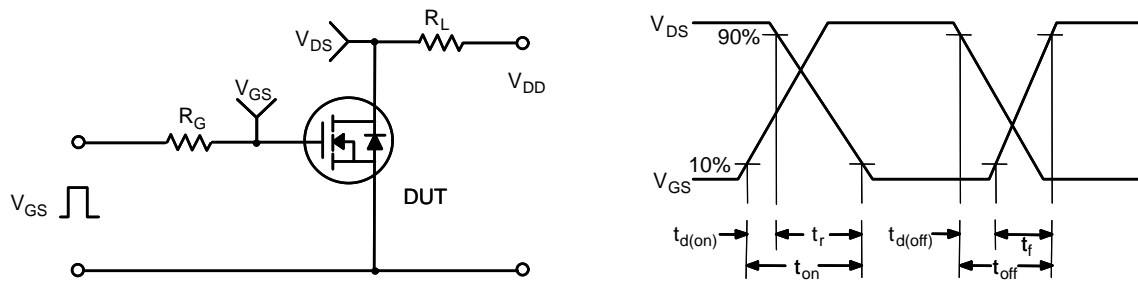


Figure 13. Resistive Switching Test Circuit & Waveforms

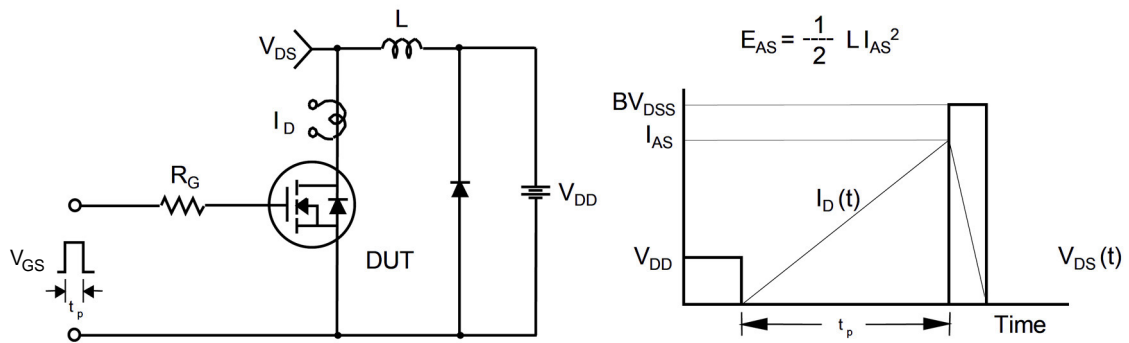


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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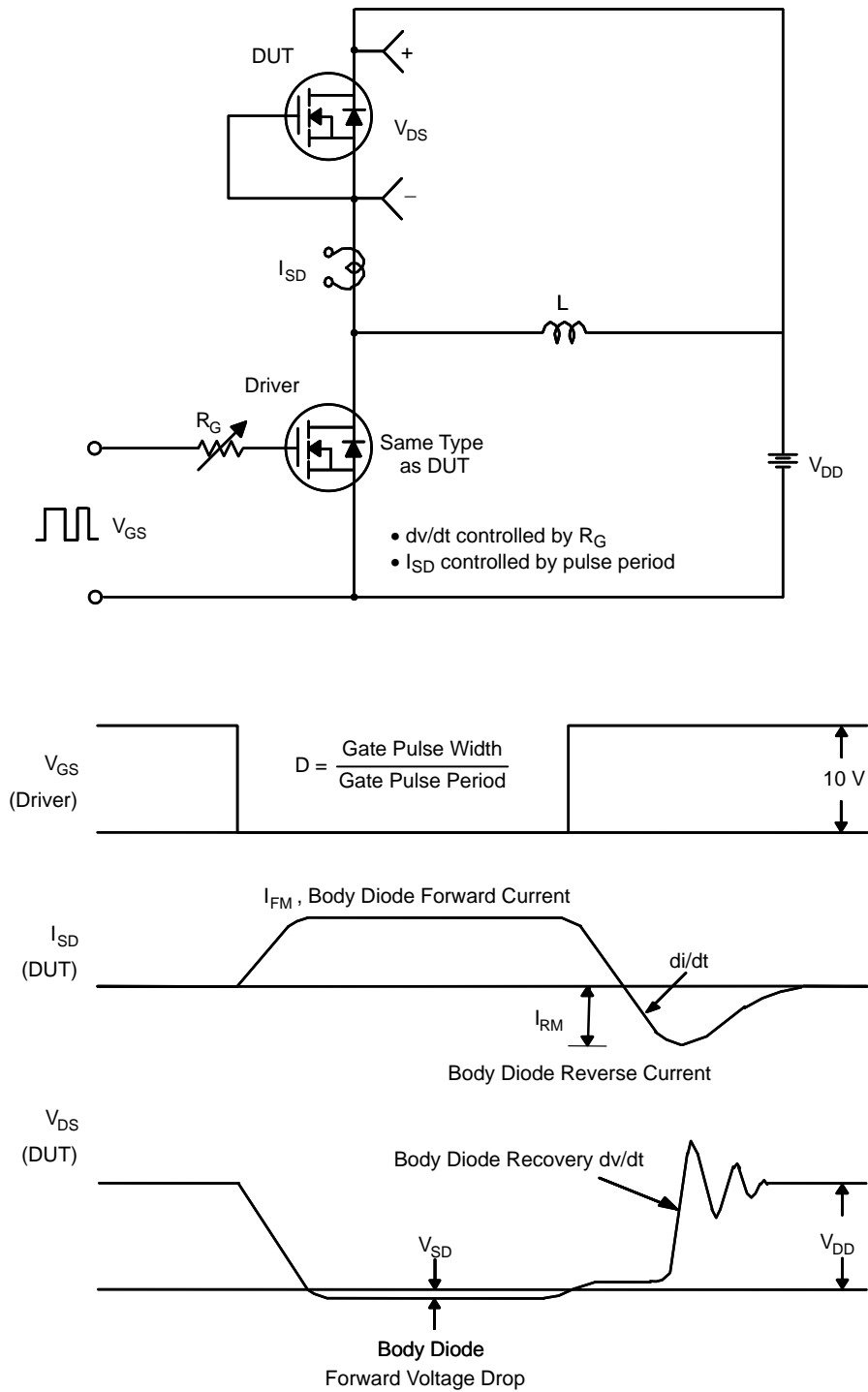


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

MECHANICAL CASE OUTLINE

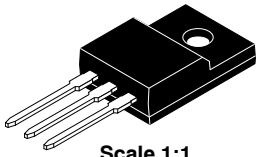
PACKAGE DIMENSIONS

ON Semiconductor®

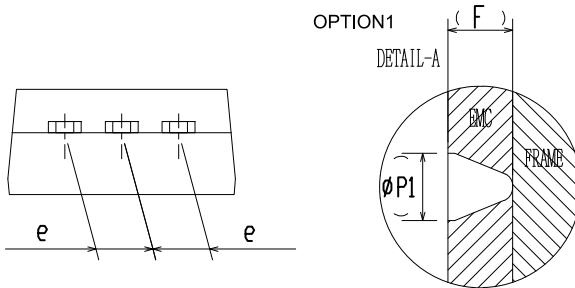
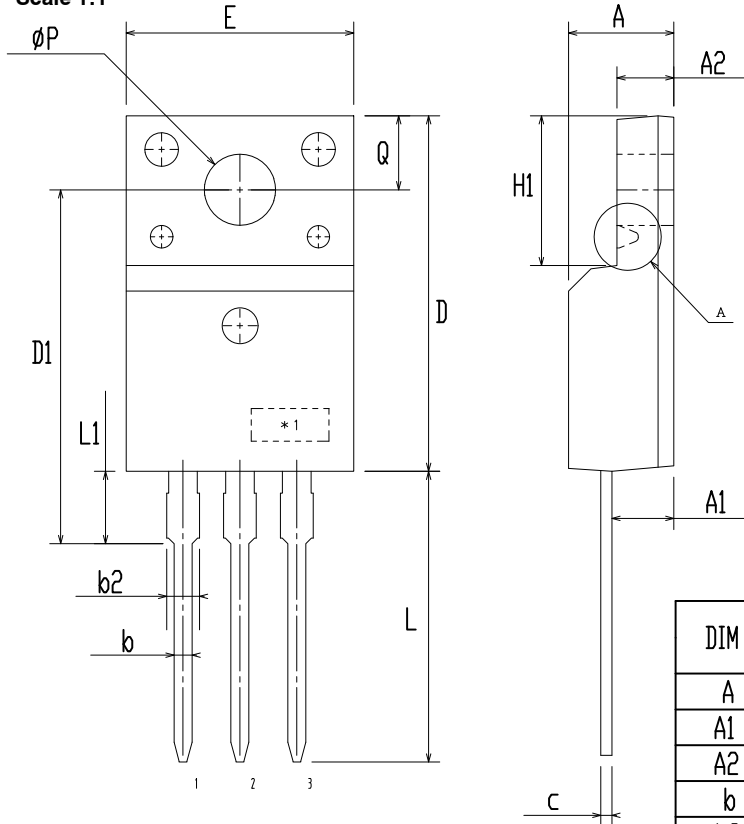


TO-220 Fullpack, 3-Lead / TO-220F-3SG CASE 221AT ISSUE B

DATE 19 JAN 2021



Scale 1:1



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.50	4.70	4.90
A1	2.56	2.76	2.96
A2	2.34	2.54	2.74
b	0.70	0.80	0.90
b2	~	~	1.47
c	0.45	0.50	0.60
D	15.67	15.87	16.07
D1	15.60	15.80	16.00
E	9.96	10.16	10.36
e	2.34	2.54	2.74
F	~	0.84	~
H1	6.48	6.68	6.88
L	12.78	12.98	13.18
L1	3.03	3.23	3.43
∅ P	2.98	3.18	3.38
∅ P1	~	1.00	~
Q	3.20	3.30	3.40

NOTES:

- A. DIMENSION AND TOLERANCE AS ASME Y14.5-2009
- B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUCTIONS.
- C. OPTION 1 - WITH SUPPORT PIN HOLE
OPTION 2 - NO SUPPORT PIN HOLE

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