

NTD23N03R

Power MOSFET

23 A, 25 V, N-Channel DPAK



ON Semiconductor®

<http://onsemi.com>

Features

- Planar HD3e Process for Fast Switching Performance
- Low $R_{DS(on)}$ to Minimize Conduction Loss
- Low C_{iss} to Minimize Driver Loss
- Low Gate Charge
- Optimized for High Side Switching Requirements in High-Efficiency DC-DC Converters
- Pb-Free Packages are Available

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

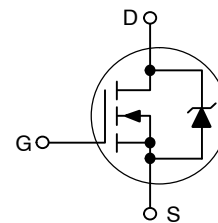
Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	25	Vdc
Gate-to-Source Voltage – Continuous	V_{GS}	± 20	Vdc
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	5.6	$^\circ\text{C/W}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	22.3	W
Drain Current	I_D	23	A
– Continuous @ $T_C = 25^\circ\text{C}$, Chip	I_D	17.1	A
– Continuous @ $T_C = 25^\circ\text{C}$, Limited by Package	I_{DM}	40	A
– Single Pulse			
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	76	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.64	W
Drain Current – Continuous @ $T_A = 25^\circ\text{C}$	I_D	4.5	A
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	110	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.14	W
Drain Current – Continuous @ $T_A = 25^\circ\text{C}$	I_D	3.8	A
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

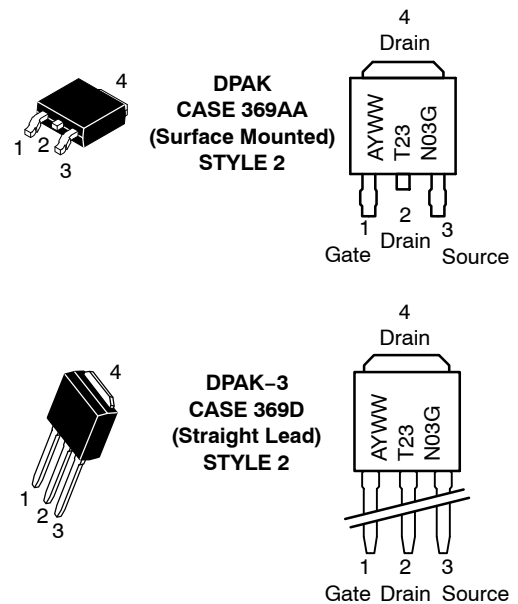
1. When surface mounted to an FR4 board using 0.5 sq in pad size.
2. When surface mounted to an FR4 board using minimum recommended pad size.

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
25 V	32 m Ω	23 A

N-CHANNEL



MARKING DIAGRAMS



T23N03 = Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NTD23N03R

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) ($V_{GS} = 0\text{ Vdc}$, $I_D = 250\ \mu\text{Adc}$) Temperature Coefficient (Positive)	$V_{(br)DSS}$	25 –	28 –	– –	Vdc mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current ($V_{DS} = 20\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$) ($V_{DS} = 20\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$, $T_J = 150^\circ\text{C}$)	I_{DSS}	– –	– –	1.0 10	μAdc
Gate-Body Leakage Current ($V_{GS} = \pm 20\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	–	–	± 100	nAdc

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) ($V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{Adc}$) Threshold Temperature Coefficient (Negative)	$V_{GS(th)}$	1.0 –	1.8 –	2.0 –	Vdc mV/ $^\circ\text{C}$
Static Drain-to-Source On-Resistance (Note 3) ($V_{GS} = 4.5\text{ Vdc}$, $I_D = 6\text{ Adc}$) ($V_{GS} = 10\text{ Vdc}$, $I_D = 6\text{ Adc}$)	$R_{DS(on)}$	– –	50.3 32.3	60 45	m Ω
Forward Transconductance (Note 3) ($V_{DS} = 10\text{ Vdc}$, $I_D = 6\text{ Adc}$)	g_{FS}	–	13	–	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = 20\text{ Vdc}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$)	C_{iss}	–	225	–	pF
Output Capacitance		C_{oss}	–	108	–	
Transfer Capacitance		C_{rss}	–	48	–	

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$(V_{GS} = 10\text{ Vdc}$, $V_{DD} = 10\text{ Vdc}$, $I_D = 6\text{ Adc}$, $R_G = 3\ \Omega$)	$t_{d(on)}$	–	2.0	–	ns
Rise Time		t_r	–	14.9	–	
Turn-Off Delay Time		$t_{d(off)}$	–	9.9	–	
Fall Time		t_f	–	2.0	–	
Gate Charge	$(V_{GS} = 4.5\text{ Vdc}$, $I_D = 6\text{ Adc}$, $V_{DS} = 10\text{ Vdc}$) (Note 3)	Q_T	–	3.76	–	nC
		Q_1	–	1.7	–	
		Q_2	–	1.6	–	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	$(I_S = 6\text{ Adc}$, $V_{GS} = 0\text{ Vdc}$) (Note 3) $(I_S = 6\text{ Adc}$, $V_{GS} = 0\text{ Vdc}$, $T_J = 125^\circ\text{C}$)	V_{SD}	– –	0.87 0.74	1.2 –	Vdc
Reverse Recovery Time	$(I_S = 6\text{ Adc}$, $V_{GS} = 0\text{ Vdc}$, $di_S/dt = 100\text{ A}/\mu\text{s}$) (Note 3)	t_{rr}	–	8.7	–	ns
		t_a	–	5.2	–	
		t_b	–	3.5	–	
Reverse Recovery Stored Charge		Q_{RR}	–	0.003	–	μC

3. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

4. Switching characteristics are independent of operating junction temperatures.

NTD23N03R

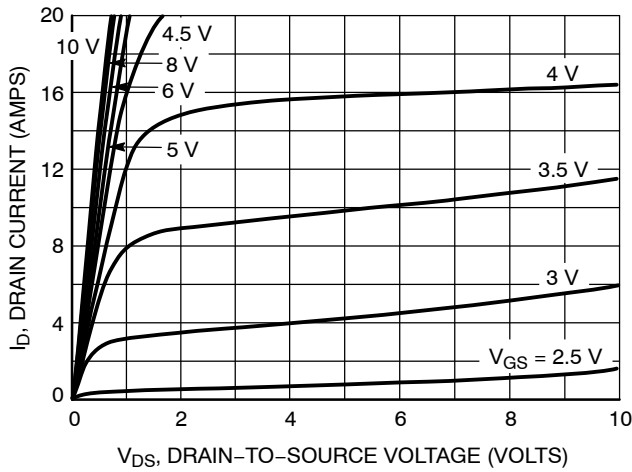


Figure 1. On-Region Characteristics

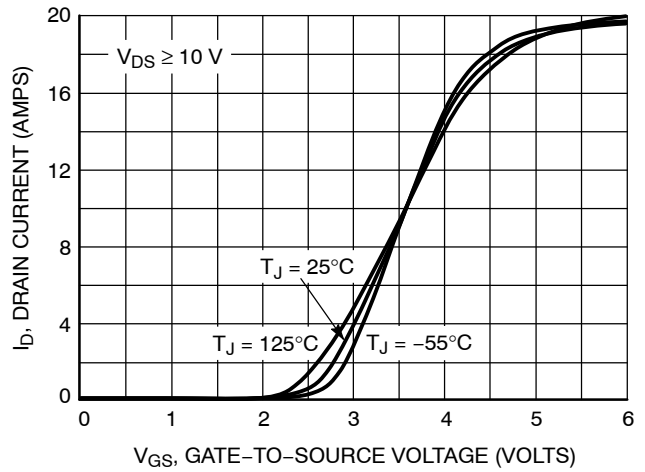


Figure 2. Transfer Characteristics

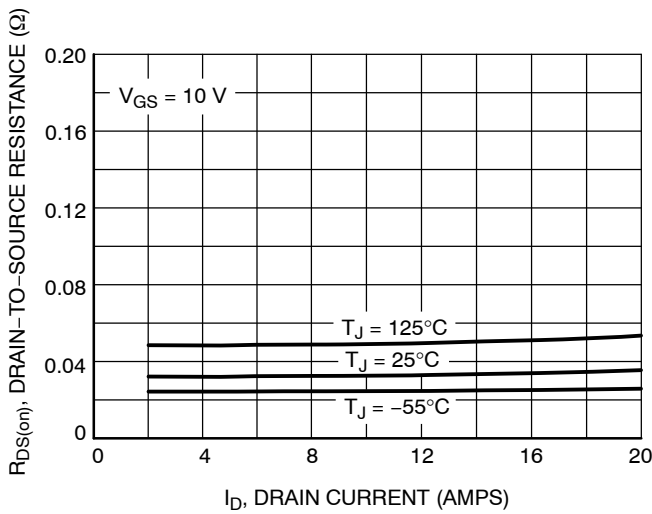


Figure 3. On-Resistance versus Drain Current and Temperature

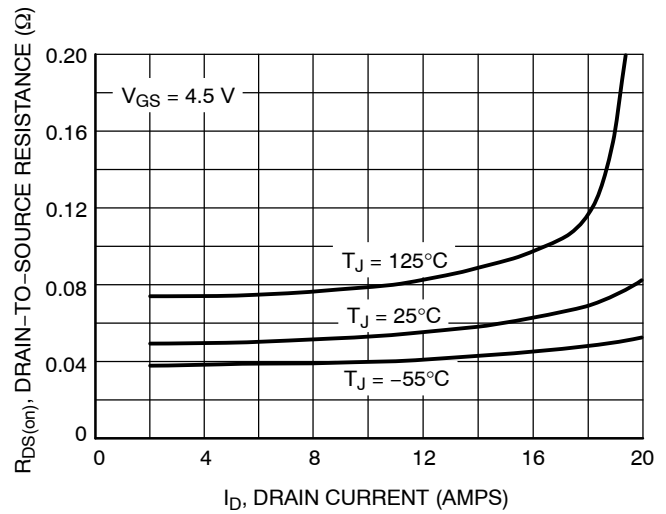


Figure 4. On-Resistance versus Drain Current and Temperature

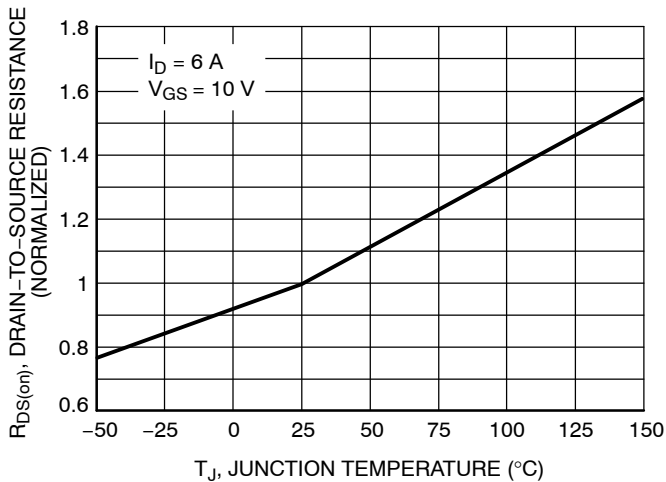


Figure 5. On-Resistance Variation with Temperature

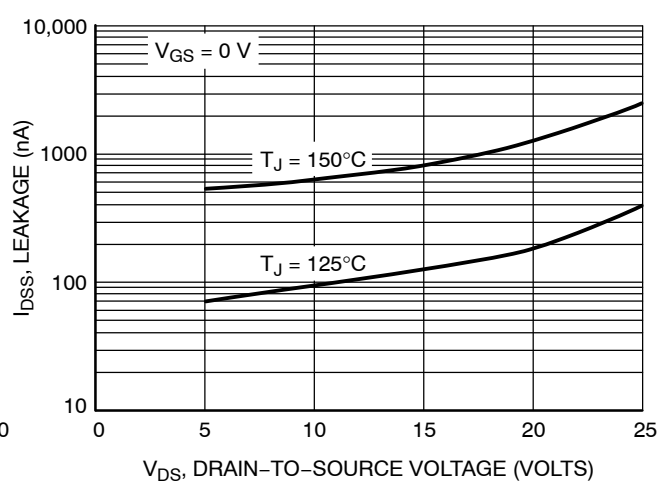


Figure 6. Drain-to-Source Leakage Current versus Voltage

NTD23N03R

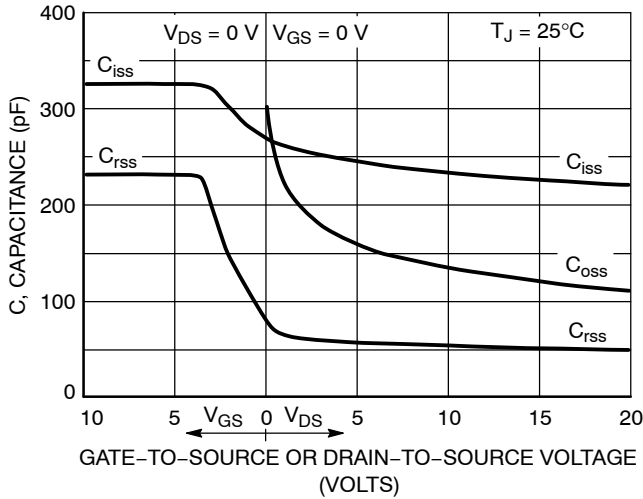


Figure 7. Capacitance Variation

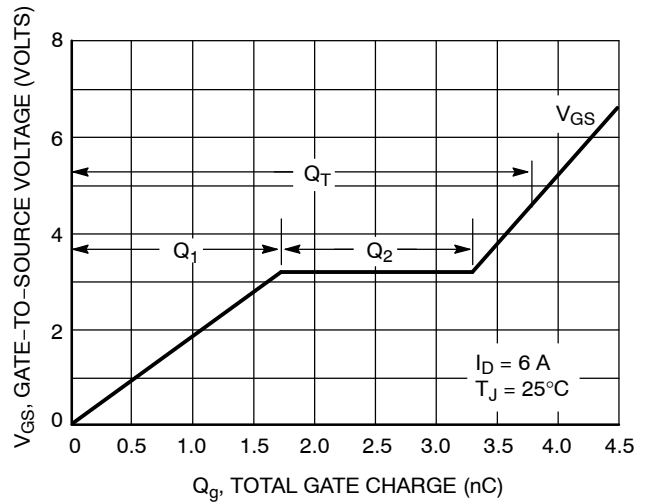


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

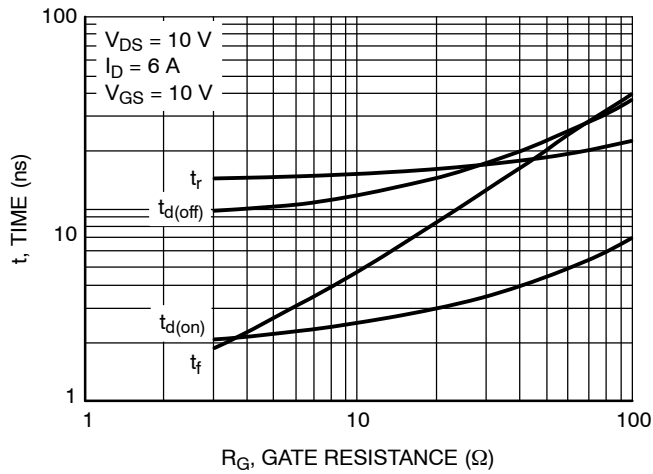


Figure 9. Resistive Switching Time Variation versus Gate Resistance

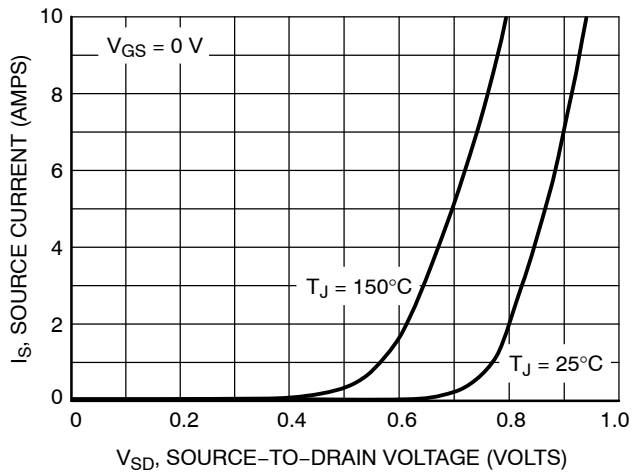


Figure 10. Diode Forward Voltage versus Current

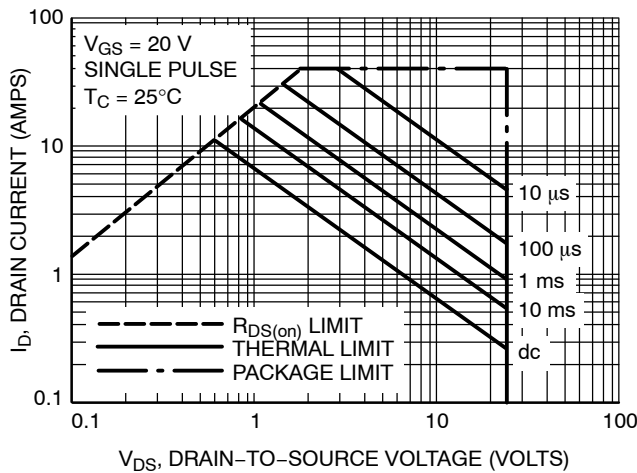


Figure 11. Maximum Rated Forward Biased Safe Operating Area

NTD23N03R

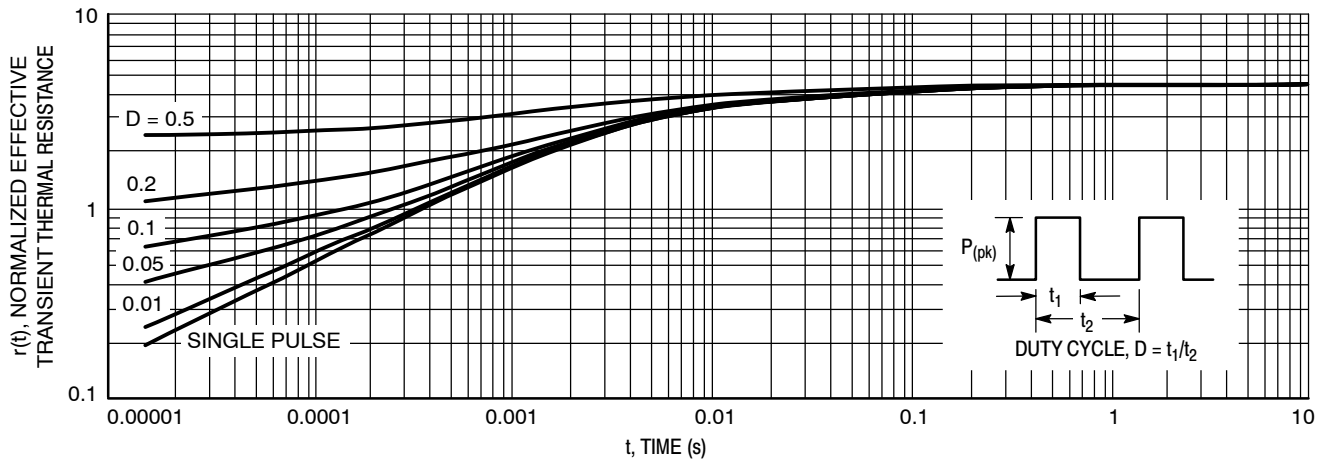


Figure 12. Thermal Response

ORDERING INFORMATION

Device	Package	Shipping†
NTD23N03RG	DPAK (Pb-Free)	75 Units/Rail
NTD23N03R-1G	DPAK-3 (Pb-Free)	75 Units/Rail
NTD23N03RT4	DPAK	2500 Tape & Reel
NTD23N03RT4G	DPAK (Pb-Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



IPAK CASE 369D-01 ISSUE C

DATE 15 DEC 2010

SCALE 1:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

MARKING DIAGRAMS

- STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR
- STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN
- STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE
- STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE
- STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE
- STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2
- STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR



- xxxxxxxxx = Device Code
- A = Assembly Location
- IL = Wafer Lot
- Y = Year
- WW = Work Week

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

DPAK (SINGLE GAUGE)

CASE 369AA-01

ISSUE B

DATE 03 JUN 2010



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

- STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR
- STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN
- STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE
- STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE
- STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE
- STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2
- STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

GENERIC MARKING DIAGRAM*

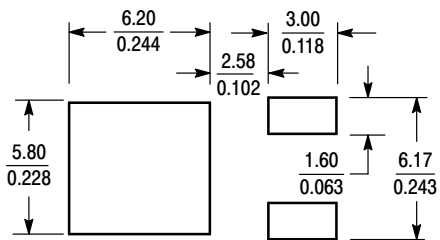


IC Discrete

- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

SOLDERING FOOTPRINT*



SCALE 3:1 (mm/inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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