74HC1G66-Q100; 74HCT1G66-Q100

Single-pole single-throw analog switch

Rev. 3 — 5 December 2023 Product data sheet

1. General description

The 74HC1G66-Q100; 74HCT1G66-Q100 is a single-pole, single-throw analog switch with two input/output terminals (nY and nZ) and a digital enable input (nE). When nE is LOW, the analog switch is turned off. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

The HCT device features control inputs with reduced input threshold levels to allow interfacing to TTL logic levels.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 2.0 V to 10.0 V
- Very low ON resistance:
  - 45 Ω (typ.) at V_{CC} = 4.5 V
  - 30 Ω (typ.) at V_{CC} = 6.0 V
  - 25 Ω (typ.) at V_{CC} = 9.0 V
- High noise immunity
- CMOS low power dissipation
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC1G66GW-Q100	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74HCT1G66GW-Q100				
74HC1G66GV-Q100	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753
74HCT1G66GV-Q100				

4. Marking

Table 2. Marking codes

Type number	Marking
74HC1G66GW-Q100	HL
74HCT1G66GW-Q100	TL
74HC1G66GV-Q100	H66
74HCT1G66GV-Q100	T66

5. Functional diagram

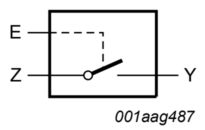


Fig. 1. Logic symbol

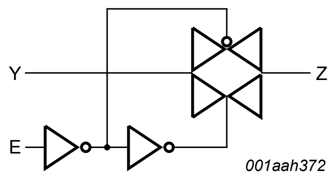


Fig. 2. Logic diagram

6. Pinning information

6.1. Pinning

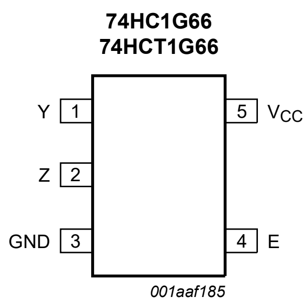


Fig. 3. Pin configuration SOT353-1 (TSSOP5) and SOT753 (SC-74A)

6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
Y	1	independent input or output
Z	2	independent input or output
GND	3	ground (0 V)
E	4	enable input (active HIGH)
V_{CC}	5	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input E	Switch
L	OFF
H	ON

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+11.0	V
I_{IK}	input clamping current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V	[1]	-	±20	mA
I_{SK}	switch clamping current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V	[1]	-	±20	mA
I_{SW}	switch current	V_{SW} > -0.5 V or V_{SW} < V_{CC} + 0.5 V		-	±25	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			-50	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT353-1 (TSSOP5) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.
For SOT753 (SC-74A) package: P_{tot} derates linearly with 3.8 mW/K above 85 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		74HC1G66-Q100			74HCT1G66-Q100			Unit
				Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage			2.0	5.0	10.0	4.5	5.0	5.5	V
V_I	input voltage			0	-	V_{CC}	0	-	V_{CC}	V
V_{SW}	switch voltage		[1]	0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature			-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.0 V		-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V		-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V		-	-	83	-	-	-	ns/V
		V_{CC} = 10.0 V		-	-	35	-	-	-	ns/V

[1] To avoid drawing V_{CC} current out of pin Z, when switch current flows in pin Y, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into pin Z, no V_{CC} current will flow out of terminal Y. In this case there is no limit for the voltage drop across the switch, but the voltage at pins Y and Z may not exceed V_{CC} or GND.

10. Static characteristics

Table 7. Static characteristics

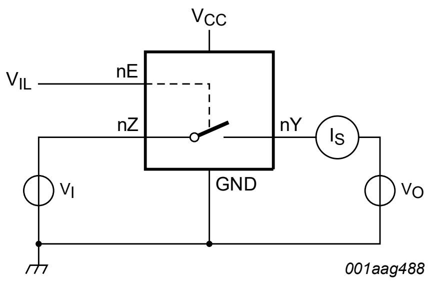
Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74HC1G66-Q100								
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	V
		V_{CC} = 9.0 V	6.3	4.7	-	6.3	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	V
		V_{CC} = 9.0 V	-	4.3	2.7	-	2.7	V
I_I	input leakage current	E; V_I = V_{CC} or GND						
		V_{CC} = 6.0 V	-	0.1	1.0	-	1.0	μA
		V_{CC} = 10.0 V	-	0.2	2.0	-	2.0	μA
$I_{S(OFF)}$	OFF-state leakage current	Y or Z; V_{CC} = 10 V; see Fig. 4	-	0.1	1.0	-	1.0	μA
$I_{S(ON)}$	ON-state leakage current	Y or Z; V_{CC} = 10 V; see Fig. 5	-	0.1	1.0	-	1.0	μA
I_{CC}	supply current	E, Y or Z; V_I = V_{CC} or GND; V_{SW} = GND or V_{CC}						
		V_{CC} = 6.0 V	-	1.0	10	-	20	μA
		V_{CC} = 10.0 V	-	2.0	20	-	40	μA
C_I	input capacitance		-	1.5	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance		-	8	-	-	-	pF

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74HCT1G66-Q100								
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	0.1	1.2	0.8	-	0.8	V
I_I	input leakage current	E; V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	0.1	1.0	-	1.0	μA
$I_{S(OFF)}$	OFF-state leakage current	Y or Z; V_{CC} = 5.5 V; see Fig. 4	-	0.1	1.0	-	1.0	μA
$I_{S(ON)}$	ON-state leakage current	Y or Z; V_{CC} = 5.5 V; see Fig. 5	-	0.1	1.0	-	1.0	μA
I_{CC}	supply current	E, Y or Z; V_I = V_{CC} or GND; V_{SW} = GND or V_{CC}; V_{CC} = 4.5 V to 5.5 V	-	1	10	-	20	μA
ΔI_{CC}	additional supply current	V_I = V_{CC} - 2.1 V; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A	-	-	500	-	850	μA
C_I	input capacitance		-	1.5	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance		-	8	-	-	-	pF

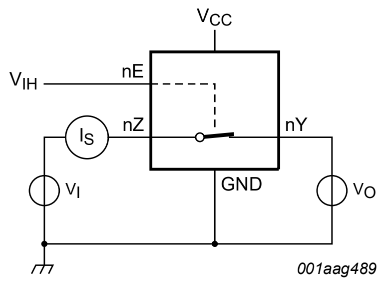
[1] Typical values are measured at T_{amb} = 25 °C.

10.1. Test circuits



V_I = V_{CC} or GND and V_O = GND or V_{CC}

Fig. 4. Test circuit for measuring OFF-state leakage current



V_I = V_{CC} or GND and V_O = open circuit

Fig. 5. Test circuit for measuring ON-state leakage current

10.2. ON resistance

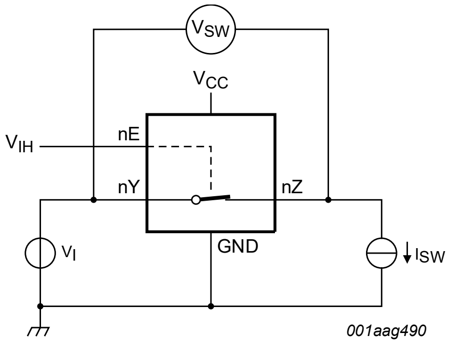
Table 8. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground 0 V); for graph see Fig. 7.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74HC1G66-Q100 [2]								
$R_{ON(peak)}$	ON resistance (peak)	V_I = GND to V_{CC}; see Fig. 6						
		I_{SW} = 0.1 mA; V_{CC} = 2.0 V	-	-	-	-	-	Ω
		I_{SW} = 1 mA; V_{CC} = 4.5 V	-	42	118	-	142	Ω
		I_{SW} = 1 mA; V_{CC} = 6.0 V	-	31	105	-	126	Ω
		I_{SW} = 1 mA; V_{CC} = 9.0 V	-	23	88	-	105	Ω
$R_{ON(rail)}$	ON resistance (rail)	V_I = GND; see Fig. 6						
		I_{SW} = 0.1 mA; V_{CC} = 2.0 V	-	75	-	-	-	Ω
		I_{SW} = 1 mA; V_{CC} = 4.5 V	-	29	95	-	115	Ω
		I_{SW} = 1 mA; V_{CC} = 6.0 V	-	23	82	-	100	Ω
		I_{SW} = 1 mA; V_{CC} = 9.0 V	-	18	70	-	80	Ω
		V_I = V_{CC}; see Fig. 6						
		I_{SW} = 0.1 mA; V_{CC} = 2.0 V	-	75	-	-	-	Ω
		I_{SW} = 1 mA; V_{CC} = 4.5 V	-	35	106	-	128	Ω
		I_{SW} = 1 mA; V_{CC} = 6.0 V	-	27	94	-	113	Ω
		I_{SW} = 1 mA; V_{CC} = 9.0 V	-	21	78	-	95	Ω
74HCT1G66-Q100								
$R_{ON(peak)}$	ON resistance (peak)	V_I = GND to V_{CC}; see Fig. 6						
		I_{SW} = 1 mA; V_{CC} = 4.5 V	-	42	118	-	142	Ω
$R_{ON(rail)}$	ON resistance (rail)	V_I = GND; see Fig. 6						
		I_{SW} = 1 mA; V_{CC} = 4.5 V	-	29	95	-	115	Ω
		V_I = V_{CC}; see Fig. 6						
		I_{SW} = 1 mA; V_{CC} = 4.5 V	-	35	106	-	128	Ω

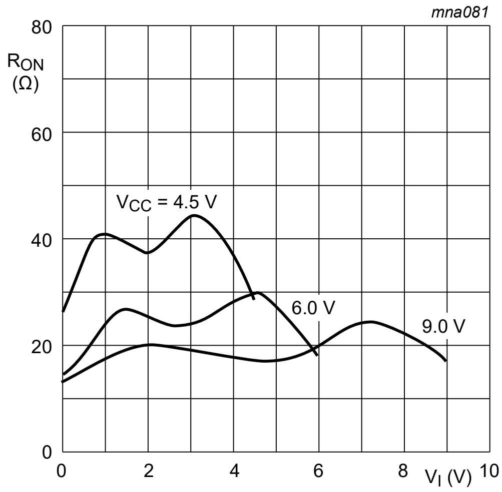
[1] Typical values are measured at T_{amb} = 25 °C.
[2] At supply voltages approaching 2 V, the ON resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using this supply voltage.

10.3. ON resistance test circuit and graphs



$R_{ON} = V_{SW} / I_{SW}$

Fig. 6. Test circuit for measuring ON resistance



T_{amb} = 25 °C

Fig. 7. Typical ON resistance as a function of input voltage

11. Dynamic characteristics

Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF; R_L = 1 kΩ, unless otherwise specified.
For test circuit see Fig. 10.

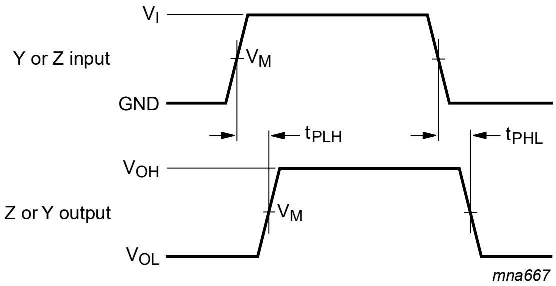
Symbol	Parameter	Conditions		-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74HC1G66-Q100								
t_{pd}	propagation delay	Y to Z or Z to Y; R_L = ∞ Ω; see Fig. 8 [2]						
		V_{CC} = 2.0 V	-	8	75	-	90	ns
		V_{CC} = 4.5 V	-	3	15	-	18	ns
		V_{CC} = 6.0 V	-	2	13	-	15	ns
		V_{CC} = 9.0 V	-	1	10	-	12	ns
t_{en}	enable time	E to Y or Z; see Fig. 9 [2]						
		V_{CC} = 2.0 V	-	50	125	-	150	ns
		V_{CC} = 4.5 V	-	16	25	-	30	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	11	-	-	-	ns
		V_{CC} = 6.0 V	-	13	21	-	26	ns
		V_{CC} = 9.0 V	-	9	16	-	20	ns
t_{dis}	disable time	E to Y or Z; see Fig. 9 [2]						
		V_{CC} = 2.0 V	-	27	190	-	225	ns
		V_{CC} = 4.5 V	-	16	38	-	45	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	11	-	-	-	ns
		V_{CC} = 6.0 V	-	14	33	-	38	ns
		V_{CC} = 9.0 V	-	12	16	-	20	ns
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} [3]	-	9	-	-	-	pF
74HCT1G66-Q100								
t_{pd}	propagation delay	Y to Z or Z to Y; R_L = ∞ Ω; see Fig. 8 [2]						
		V_{CC} = 4.5 V	-	3	15	-	18	ns
t_{en}	enable time	E to Y or Z; see Fig. 9 [2]						
		V_{CC} = 4.5 V	-	15	30	-	36	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	12	-	-	-	ns
t_{dis}	disable time	E to Y or Z; see Fig. 9 [2]						
		V_{CC} = 4.5 V	-	13	44	-	53	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	12	-	-	-	ns
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} - 1.5 V [3]	-	9	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.
[2] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{en} is the same as t_{PZL} and t_{PZH}.; t_{dis} is the same as t_{PLZ} and t_{PHZ}.
[3] C_{PD} is used to determine the dynamic power dissipation P_D (μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma((C_L \times C_{SW}) \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz;
C_L = output load capacitance in pF; C_{SW} = maximum switch capacitance in pF (see Table 7);
V_{CC} = supply voltage in Volt;
$\Sigma((C_L \times C_{SW}) \times V_{CC}^2 \times f_o)$ = sum of outputs.

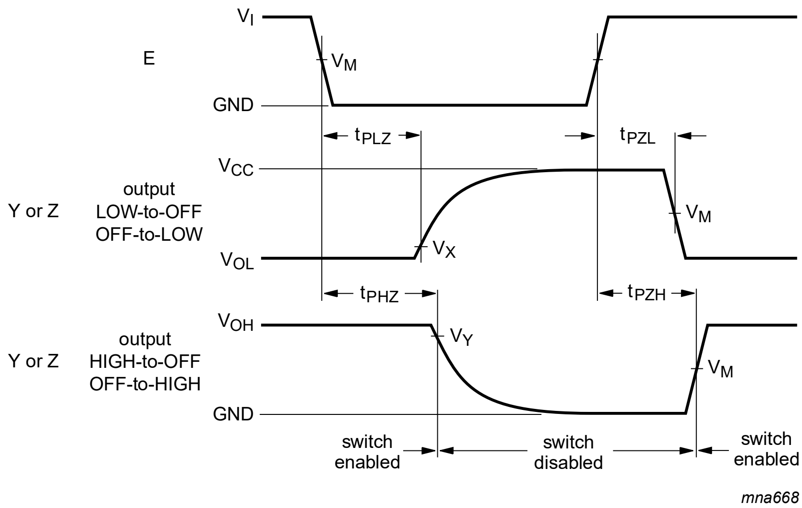
11.1. Waveforms and test circuit



Measurement points are given in Table 10.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 8. Input (Y or Z) to output (Z or Y) propagation delays



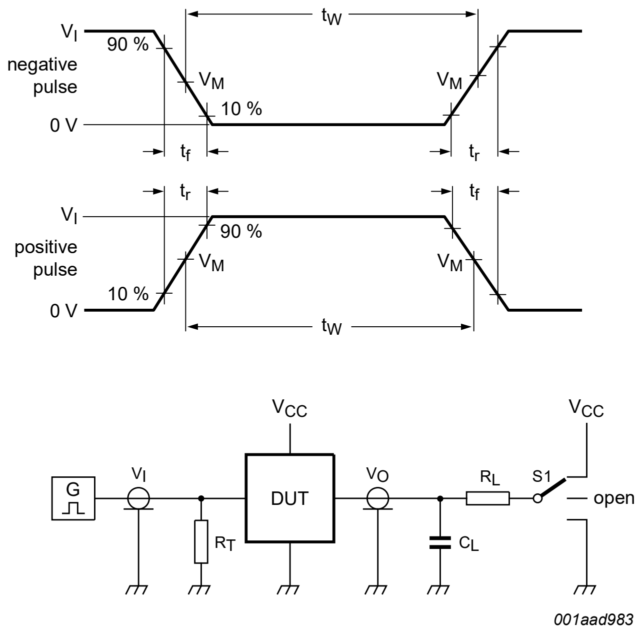
Measurement points are given in Table 10.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 9. Enable and disable times

Table 10. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC1G66-Q100	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 10%	V_{OH} - 10%
74HCT1G66-Q100	1.3 V	1.3 V	V_{OL} + 10%	V_{OH} - 10%



Test data is given in Table 11.

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator
C_L = Load capacitance including jig and probe capacitance
R_L = Load resistance
S1 = Test selection switch

Fig. 10. Test circuit for measuring switching times

Table 11. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f [1]	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC1G66-Q100	GND to V_{CC}	6 ns	50 pF, 15 pF	1 kΩ, ∞ Ω	open	GND	V_{CC}
74HCT1G66-Q100	GND to 3 V	6 ns	50 pF, 15 pF	1 kΩ, ∞ Ω	open	GND	V_{CC}

[1] There is no constraint on t_r, t_f with a 50% duty factor when measuring f_{max}.

11.2. Additional dynamic characteristics

Table 12. Additional dynamic characteristics for 74HC1G66 and 74HCT1G66

GND = 0 V; t_r = t_f = 6.0 ns; C_L = 50 pF; unless otherwise specified. All typical values are measured at T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	f_i = 1 kHz; R_L = 10 kΩ; see Fig. 11				%
		V_{CC} = 4.5 V; V_I = 4.0 V (p-p)	-	0.04	-	%
		V_{CC} = 9.0 V; V_I = 8.0 V (p-p)	-	0.02	-	%
		f_i = 10 kHz; R_L = 10 kΩ; see Fig. 11				
		V_{CC} = 4.5 V; V_I = 4.0 V (p-p)	-	0.12	-	%
		V_{CC} = 9.0 V; V_I = 8.0 V (p-p)	-	0.06	-	%
$f_{(-3dB)}$	-3 dB frequency response	R_L = 50 Ω; C_L = 10 pF; see Fig. 12 and Fig. 13				
		V_{CC} = 4.5 V	-	180	-	MHz
		V_{CC} = 9.0 V	-	200	-	MHz
α_{iso}	isolation (OFF-state)	R_L = 600 Ω; f_i = 1 MHz; see Fig. 14 and Fig. 15				
		V_{CC} = 4.5 V	-	-50	-	dB
		V_{CC} = 9.0 V	-	-50	-	dB

11.3. Test circuits and graphs

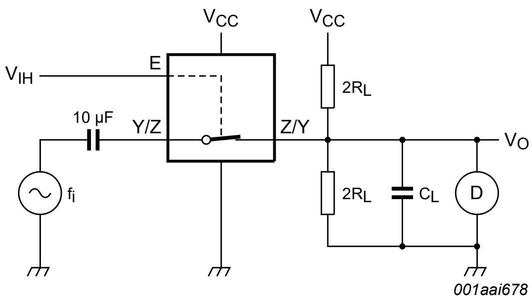
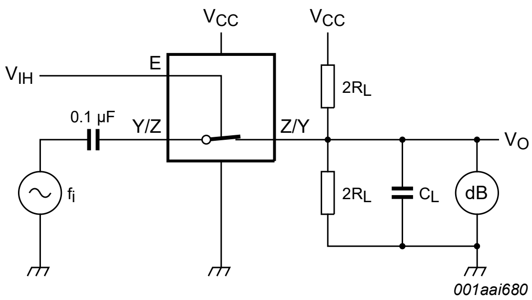
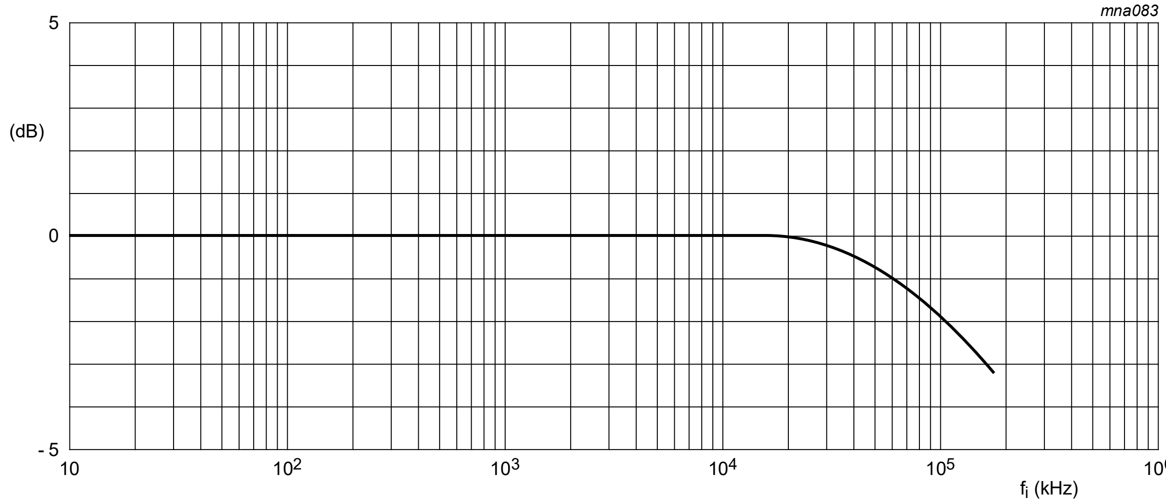


Fig. 11. Test circuit for measuring total harmonic distortion



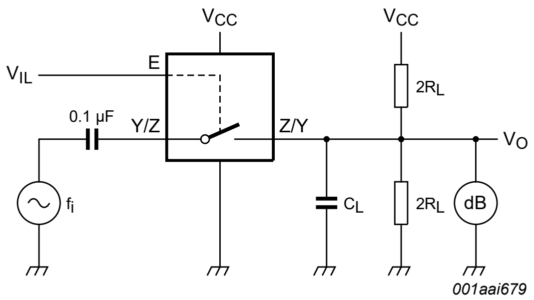
With f_i = 1 MHz adjust the switch input voltage for a 0 dBm level at the switch output, (0 dBm = 1 mW into 50 Ω). Then increase the input frequency until the dB meter reads -3 dB

Fig. 12. Test circuit for measuring the -3 dB frequency response



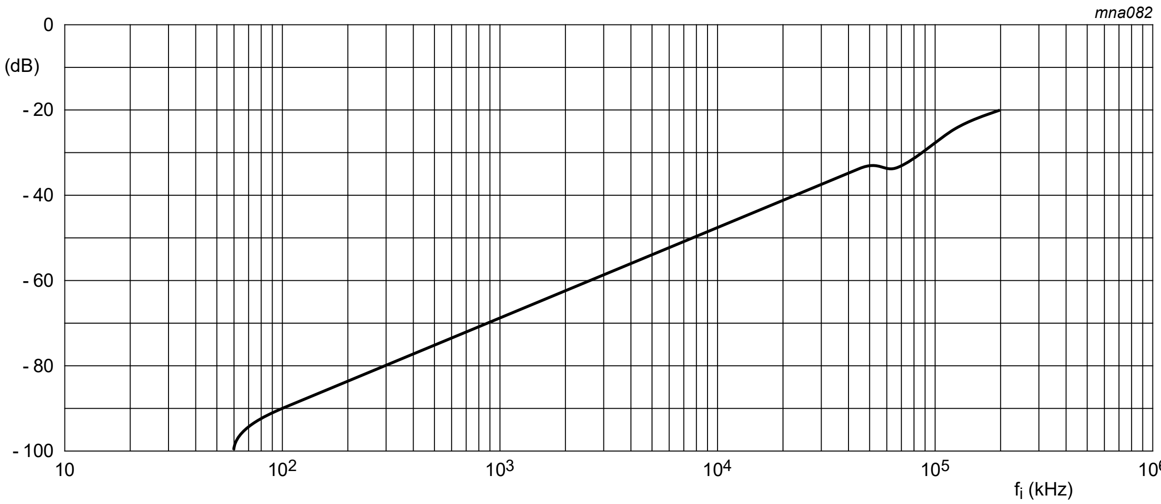
Test conditions: V_{CC} = 4.5 V; GND = 0 V; R_L = 50 Ω; R_{SOURCE} = 1 kΩ

Fig. 13. Typical -3 dB frequency response



Adjust the switch input voltage for a 0 dBm level (0 dBm = 1 mW into 600 Ω).

Fig. 14. Test circuit for measuring isolation (OFF-state)

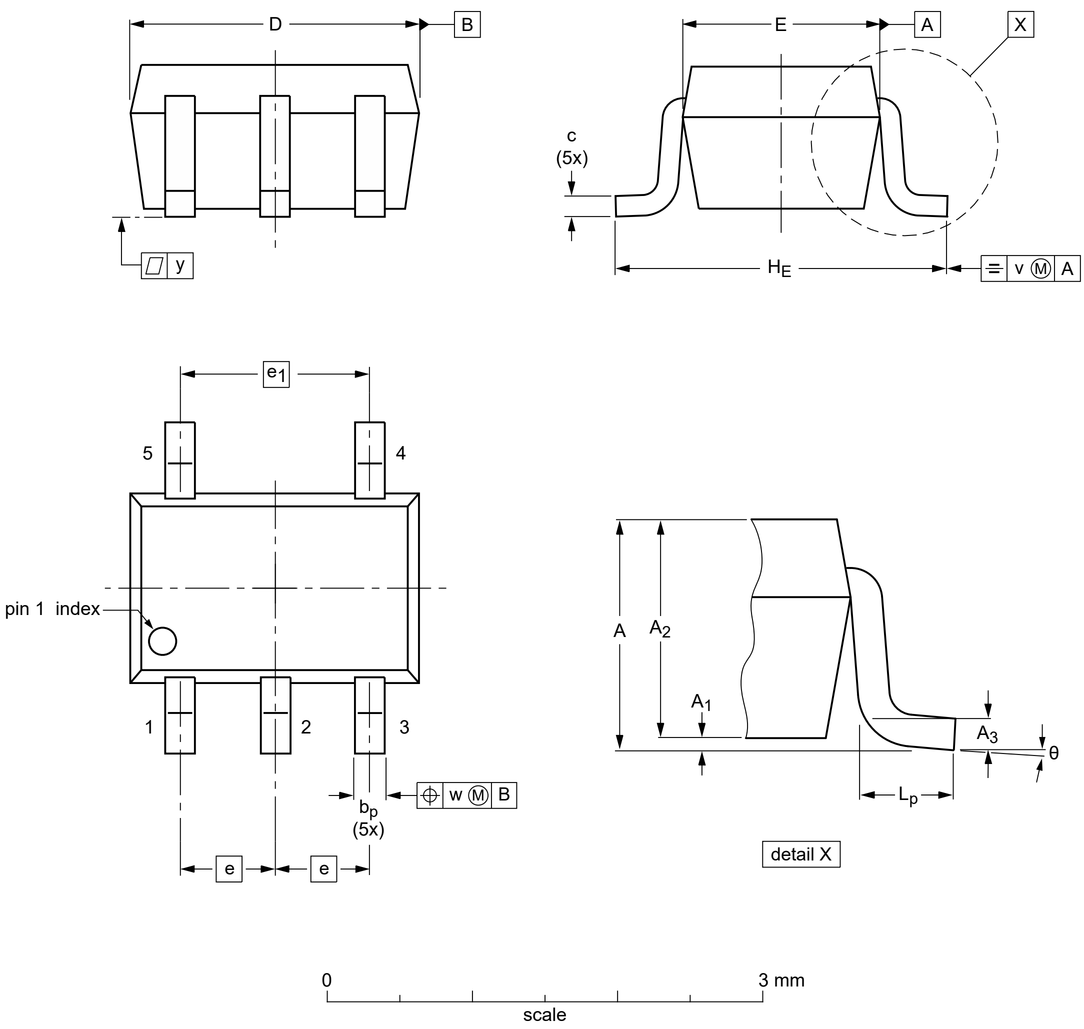


Test conditions: V_{CC} = 4.5 V; GND = 0 V; R_L = 50 Ω; R_{SOURCE} = 1 kΩ

Fig. 15. Typical isolation (OFF-state) as a function of frequency

12. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm **SOT353-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	e_1	H_E	L_p	v	w	y	θ
mm	max	1.1	0.1	1.0	0.15	0.30	0.25	2.2	1.35	0.65	1.3	2.4	0.46	0.3	0.1	0.1	8°
	min	0.8	0	0.8		0.15	0.08	1.8	1.15			1.8	0.26				0°

Note

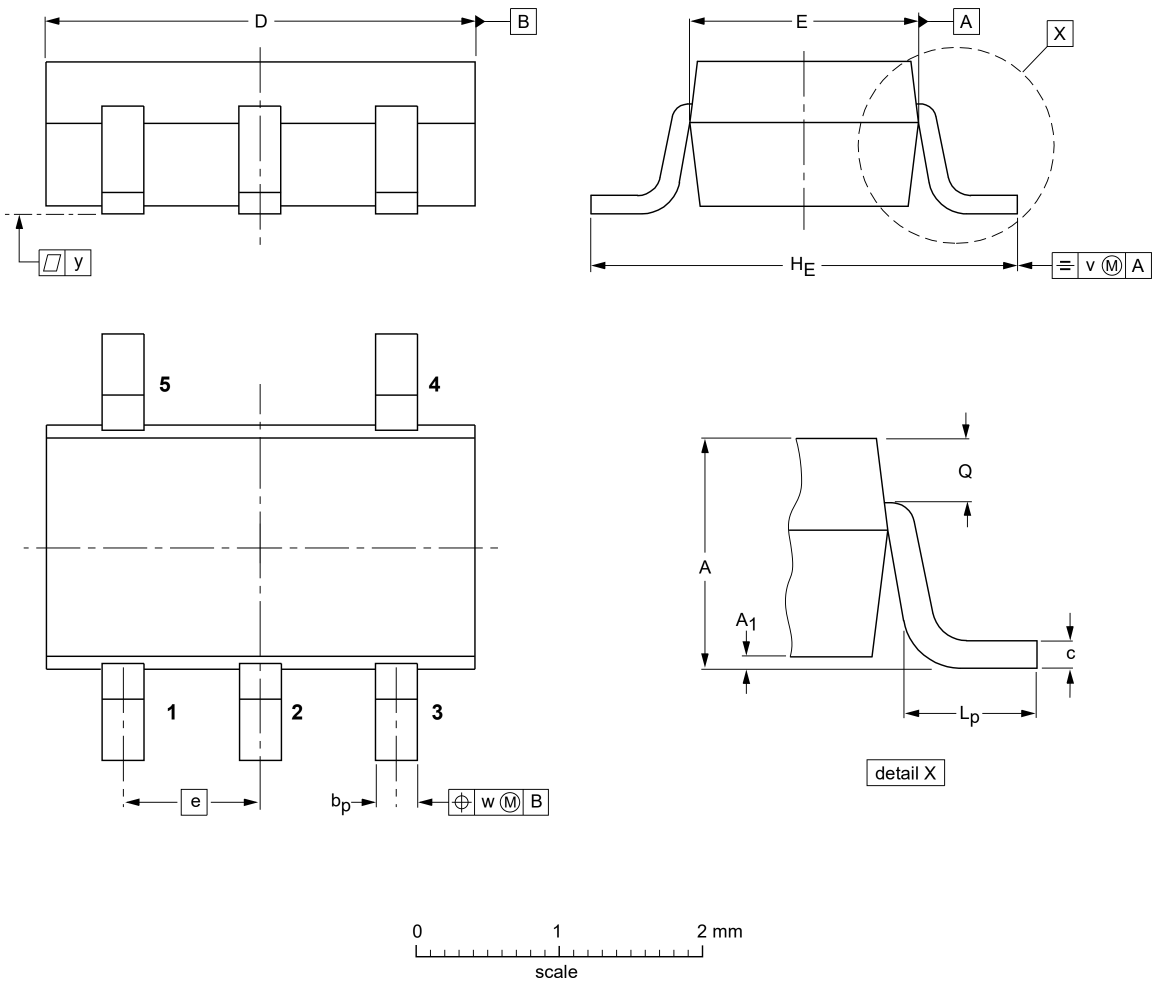
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

sot353-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT353-1		MO-203	SC-88A			~~21-12-15~~ 21-12-16

Fig. 16. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads **SOT753**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.100 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT753			SC-74A			~~02-04-16~~ 06-03-16

Fig. 17. Package outline SOT753 (SC-74A)

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic
DUT	Device Under Test

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT1G66_Q100 v.3	20231205	Product data sheet	-	74HC_HCT1G66_Q100 v.2
Modifications	• Section 2: ESD specification updated according to the latest JEDEC standard.			
74HC_HCT1G66_Q100 v.2	20220127	Product data sheet	-	74HC_HCT1G66_Q100 v.1
Modifications	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 2 updated. • Table 5: Derating values for P_{tot} total power dissipation updated. • Fig. 16: Package outline drawing for SOT353-1 (TSSOP5) has changed			
74HC_HCT1G66_Q100 v.1	20130916	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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