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TinyLogic ULP-A Dual Inverter

NC7WV04

The NC7WV04 is a dual inverter in tiny footprint packages. The device is designed to operate for V_{CC} = 0.9 V to 3.6 V.

Features

- Designed for 0.9 V to 3.6 V V_{CC} Operation
- 1.6 ns t_{PD} at 3.3 V (Typ)
- Inputs/Outputs Over−Voltage Tolerant up to 3.6 V
- I_{OFF} Supports Partial Power Down Protection
- Source/Sink 24 mA at 3.3 V
- Available in SC−88A and MicroPak™ Packages
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant
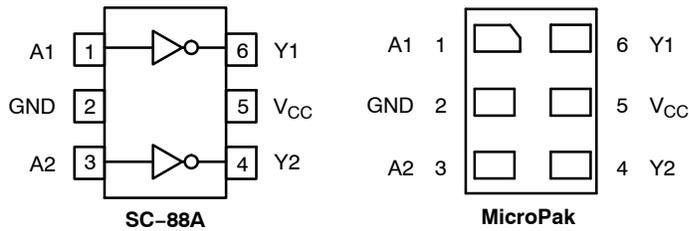
Figure 1. Pinout Diagrams (Top Views)
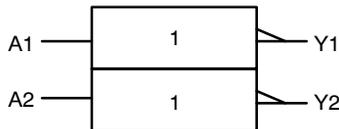
Figure 2. Logic Symbol

PIN ASSIGNMENT

Pin	Function
1	A1
2	GND
3	A2
4	Y2
5	V_{CC}
6	Y1

ON Semiconductor®

MARKING DIAGRAMS

SIP6 1.45X1.0
MicroPak
CASE 127EB

CCKK
XYZ

Pin 1
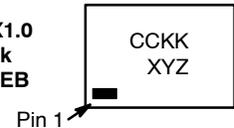
CC = Specific Device Code
KK = 2−Digit Lot Run Traceability Code
XY = 2−Digit Date Code
Z = Assembly Plant Code
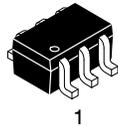
SC−88
DF SUFFIX
CASE 419B−02
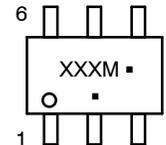
XXXM ▪

XXX = Specific Devic Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

FUNCTION TABLE

A Input	Y Output
L	H
H	L

MAXIMUM RATINGS

Symbol	Characteristics		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +4.3	V
V_{IN}	DC Input Voltage		−0.5 to +4.3	V
V_{OUT}	DC Output Voltage	Active−Mode (High or Low State) Tri−State Mode (Note 1) Power−Down Mode (V_{CC} = 0 V)	−0.5 to V_{CC} + 0.5 −0.5 to +4.3 −0.5 to +4.3	V
I_{IK}	DC Input Diode Current	V_{IN} < GND	−50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < GND	−50	mA
I_{OUT}	DC Output Source/Sink Current		±50	mA
I_{CC} or I_{GND}	DC Supply Current per Supply Pin or Ground Pin		±50	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)	SC−88A MicroPak	377 154	°C/W
P_D	Power Dissipation in Still Air	SC−88A MicroPak	332 812	mW
MSL	Moisture Sensitivity		Level 1	–
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	–
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	2000 1000	V
$I_{Latchup}$	Latchup Performance (Note 4)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Applicable to devices with outputs that may be tri−stated.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2 ounce copper trace no air flow per JESD51−7.
3. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.
4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage		0.9	3.6	V
V_{IN}	DC Input Voltage		0	3.6	V
V_{OUT}	DC Output Voltage	Active–Mode (High or Low State) Tri–State Mode (Note 1) Power–Down Mode (V_{CC} = 0 V)	0 0 0	V_{CC} 3.6 3.6	
T_A	Operating Temperature Range		−40	+85	°C
t_r , t_f	Input Transition Rise and Fall Time	V_{CC} = 3.3 V ± 0.3 V	0	10	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			T_A = −40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High–Level Input Voltage		0.9	–	0.5	–	–	–	V
			1.1 to 1.3	0.65 x V_{CC}	–	–	0.65 x V_{CC}	–	
			1.4 to 1.6	0.65 x V_{CC}	–	–	0.65 x V_{CC}	–	
			1.65 to 1.95	0.65 x V_{CC}	–	–	0.65 x V_{CC}	–	
			2.3 to <2.7	1.6	–	–	1.6	–	
			2.7 to 3.6	2.0	–	–	2.0	–	
V_{IL}	Low–Level Input Voltage		0.9	–	0.5	–	–	–	V
			1.1 to 1.3	–	–	0.35 x V_{CC}	–	0.35 x V_{CC}	
			1.4 to 1.6	–	–	0.35 x V_{CC}	–	0.35 x V_{CC}	
			1.65 to 1.95	–	–	0.35 x V_{CC}	–	0.35 x V_{CC}	
			2.3 to <2.7	–	–	0.7	–	0.7	
			2.7 to 3.6	–	–	0.8	–	0.8	
V_{OH}	High–Level Output Voltage	V_{IN} = V_{IH} or V_{IL}							V
		I_{OH} = −100 μA	0.9	–	V_{CC} − 0.1	–	–	–	
			1.1 to 1.3	V_{CC} − 0.1	–	–	V_{CC} − 0.1	–	
			1.4 to 1.6	V_{CC} − 0.1	–	–	V_{CC} − 0.1	–	
			1.65 to 1.95	V_{CC} − 0.2	–	–	V_{CC} − 0.2	–	
			2.3 to <2.7	V_{CC} − 0.2	–	–	V_{CC} − 0.2	–	
			2.7 to 3.6	V_{CC} − 0.2	–	–	V_{CC} − 0.2	–	
		I_{OH} = −2 mA	1.1 o 1.3	0.75 x V_{CC}	–	–	0.75 x V_{CC}	–	
		I_{OH} = −4 mA	1.4 to 1.6	0.75 x V_{CC}	–	–	0.75 x V_{CC}	–	
		I_{OH} = −6 mA	1.65 to 1.95	1.25	–	–	1.25	–	
			2.3 to <2.7	2.0	–	–	2.0	–	
		I_{OH} = −12 mA	2.3 to <2.7	1.8	–	–	1.8	–	
			2.7 to 3.6	2.2	–	–	2.2	–	
		I_{OH} = −18 mA	2.3 to <2.7	1.7	–	–	1.7	–	
			2.7 to 3.6	2.4	–	–	2.4	–	
		I_{OH} = −24 mA	2.7 to 3.6	2.2	–	–	2.2	–	

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Condition	V_{CC} (V)	$T_A = 25°C$			$T_A = -40°C$ to $+85°C$		Unit
				Min	Typ	Max	Min	Max	
V_{OL}	Low-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}							V
		$I_{OL} = 100$ μA	0.9	–	0.1	–	–	–	
			1.1 to 1.3	–	–	0.1	–	0.1	
			1.4 to 1.6	–	–	0.1	–	0.1	
			1.65 to 1.95	–	–	0.2	–	0.2	
			2.3 to < 2.7	–	–	0.2	–	0.2	
			2.7 to 3.6	–	–	0.2	–	0.2	
		$I_{OL} = 2$ mA	1.1 o 1.3	–	–	0.25 x V_{CC}	–	0.25 x V_{CC}	
		$I_{OL} = 4$ mA	1.4 to 1.6	–	–	0.25 x V_{CC}	–	0.25 x V_{CC}	
		$I_{OL} = 6$ mA	1.65 to 1.95	–	–	0.3	–	0.3	
		$I_{OL} = 12$ mA	2.3 to <2.7	–	–	0.4	–	0.4	
			2.7 to 3.6	–	–	0.4	–	0.4	
		$I_{OL} = 18$ mA	2.3 to <2.7	–	–	0.6	–	0.6	
			2.7 to 3.6	–	–	0.4	–	0.4	
		$I_{OL} = 24$ mA	2.7 to 3.6	–	–	0.55	–	0.55	
I_{IN}	Input Leakage Current	$V_{IN} = 0$ V to 3.6 V	0.9 to 3.6	–	–	±0.1	–	±0.5	μA
I_{OFF}	Power Off Leakage Current	$V_{IN} = 0$ V to 3.6 V or $V_{OUT} = 0$ V to 3.6 V	0	–	–	0.5	–	0.5	μA
I_{CC}	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	0.9 to 3.6	–	–	0.9	–	0.9	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
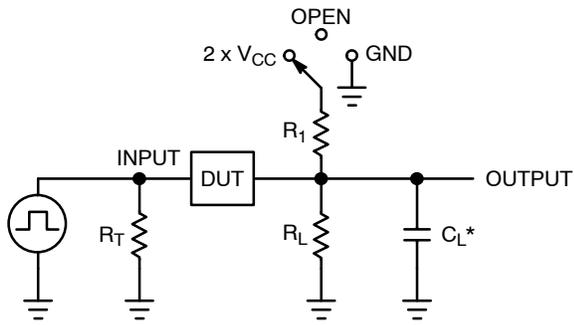
AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	$T_A = 25°C$			$T_A = -40°C$ to $+85°C$		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay, A to Y (Figures 3 and 4)	$R_L = 1$ MΩ, $C_L = 15$ pF	0.9	–	17.4	–	–	–	ns
		$R_L = 2$ kΩ, $C_L = 15$ pF	1.1 to 1.3	–	4.5	12.1	–	14.9	
			1.4 to 1.6	–	2.9	5.4	–	6.0	
		$R_L = 500$ Ω, $C_L = 30$ pF	1.65 to 1.95	–	2.5	4.6	–	5.2	
			2.3 to 2.7	–	1.9	3.6	–	3.8	
			2.7 to 3.6	–	1.6	3.0	–	3.3	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition	Typical ($T_A = 25°C$)	Unit
C_{IN}	Input Capacitance	$V_{CC} = 0$ V	2.0	pF
C_{OUT}	Output Capacitance	$V_{CC} = 0$ V	4.5	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	f = 10 MHz, $V_{CC} = 0.9$ to 3.6 V, $V_{IN} = 0$ V or V_{CC}	10.0	pF

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NC7WV04

Test	Switch Position
t_{PLH} / t_{PHL}	Open
t_{PLZ} / t_{PZL}	2 x V_{CC}
t_{PHZ} / t_{PZH}	GND

C_L includes probe and jig capacitance
R_T is Z_{OUT} of pulse generator (typically 50 Ω)
f = 1 MHz

Figure 3. Test Circuit
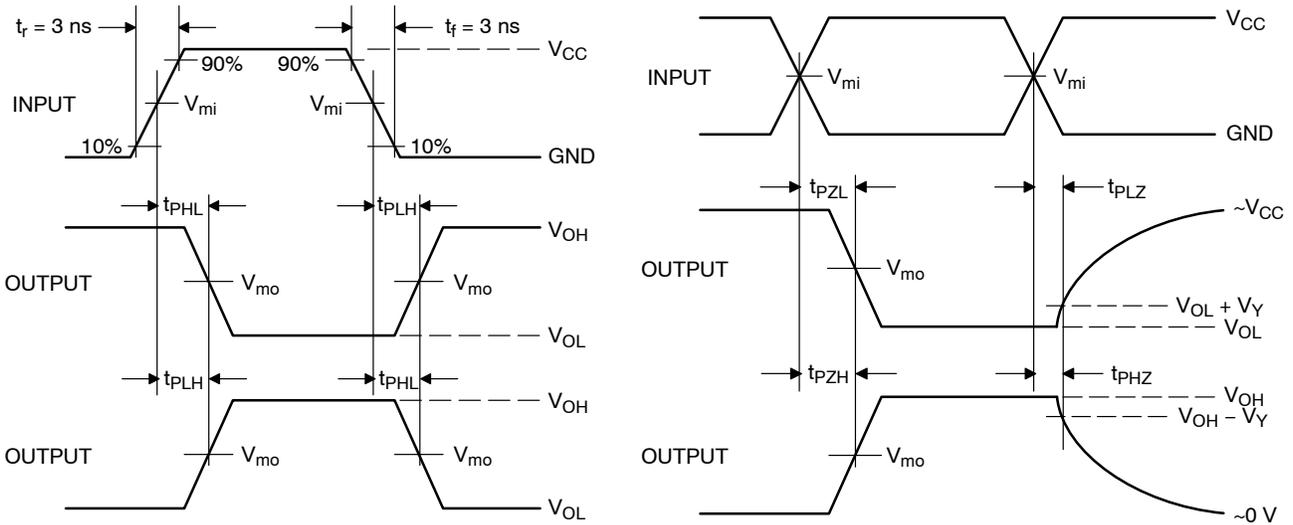
V_{CC}, V	V_{mi}, V	V_{mo}, V	V_Y, V
0.9	V_{CC} / 2	V_{CC} / 2	0.1
1.1 to 1.3	V_{CC} / 2	V_{CC} / 2	0.1
1.4 to 1.6	V_{CC} / 2	V_{CC} / 2	0.1
1.65 to 1.95	V_{CC} / 2	V_{CC} / 2	0.15
2.3 to 2.7	V_{CC} / 2	V_{CC} / 2	0.15
3.0 to 3.6	1.5	1.5	0.3

Figure 4. Switching Waveforms

NC7WV04

Device	Package	Marking	Pin 1 Orientation (See below)	Shipping†
NC7WV04P6X	SC−88	V04	Q4	3000 / Tape & Reel
NC7WV04L6X	MicroPak	BA	Q4	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
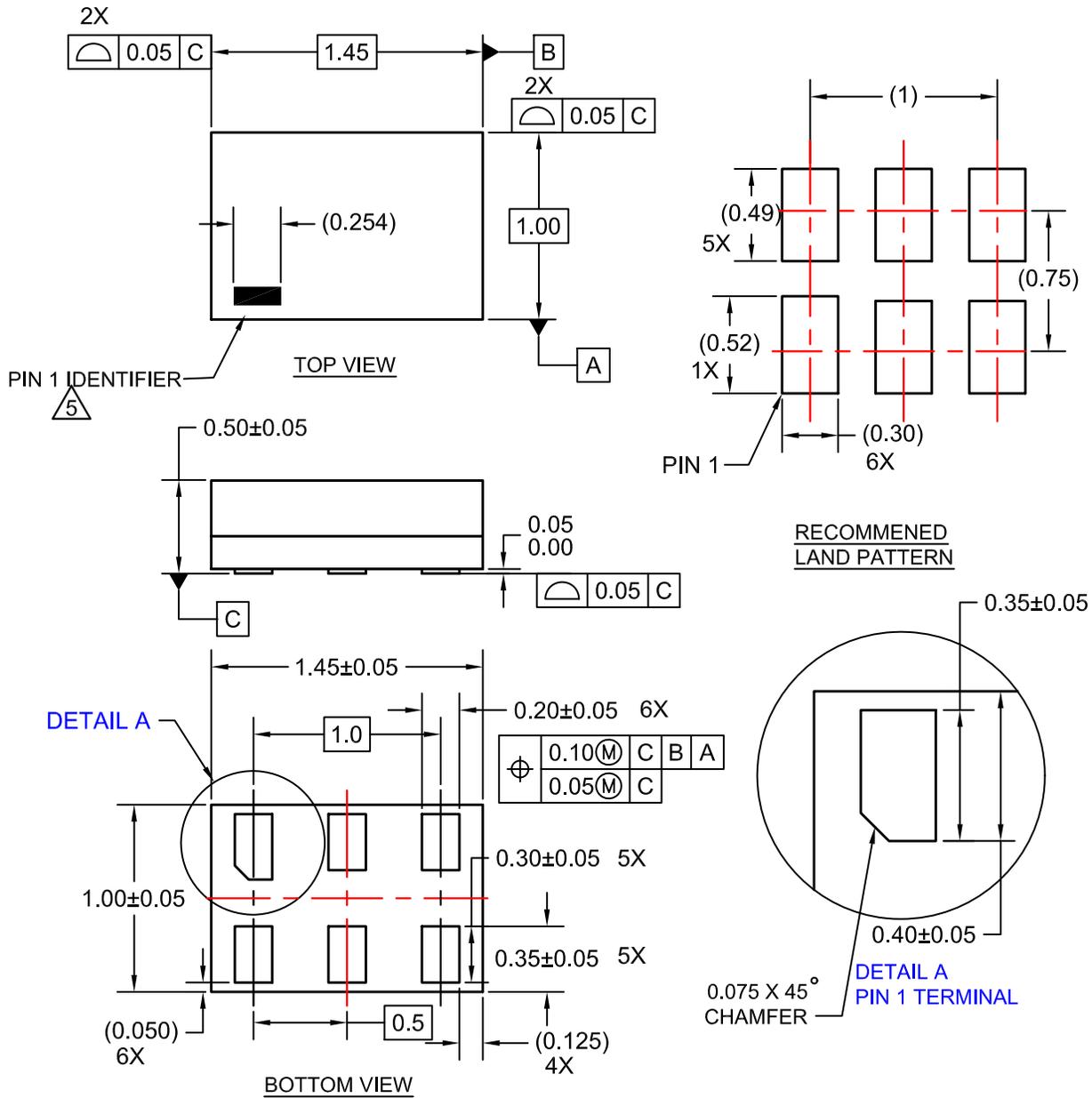
Pin 1 Orientation in Tape and Reel
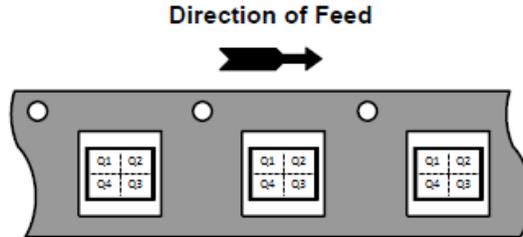
Direction of Feed

PACKAGE DIMENSIONS

SIP6 1.45X1.0
CASE 127EB
ISSUE O

TOP VIEW

PIN 1 IDENTIFIER

2X

0.05 C

1.45

B

2X

0.05 C

1.00

(0.254)

A

0.50±0.05

0.05
0.00

0.05 C

C

RECOMMENED LAND PATTERN

(1)

(0.49)
5X

(0.52)
1X

(0.75)

(0.30)
6X

PIN 1

BOTTOM VIEW

DETAIL A

1.45±0.05

1.0

0.20±0.05   6X

0.10 Ⓜ C B A
0.05 Ⓜ C

1.00±0.05

0.30±0.05   5X

0.35±0.05   5X

(0.050)
6X

0.5

(0.125)
4X

**DETAIL A
PIN 1 TERMINAL**

0.35±0.05

0.40±0.05

0.075 X 45°
CHAMFER

NOTES:
1. CONFORMS TO JEDEC STANDARD MO-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-2009
4. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

1
SCALE 2:1

SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE Y

DATE 11 DEC 2012

TOP VIEW

DETAIL A

GAGE PLANE

2X 3 TIPS

SIDE VIEW

SEATING PLANE

END VIEW

DETAIL A
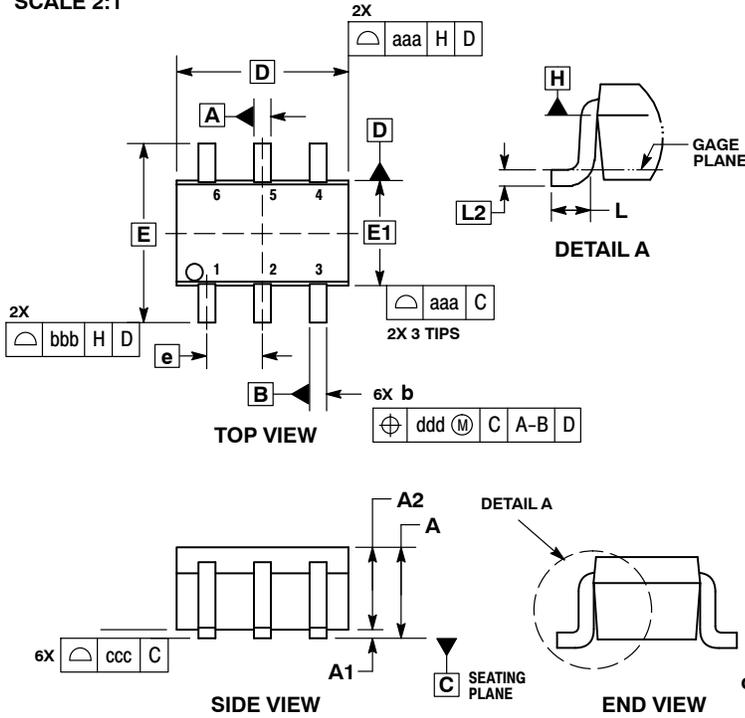
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	–––	–––	1.10	–––	–––	0.043
A1	0.00	–––	0.10	0.000	–––	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

RECOMMENDED SOLDERING FOOTPRINT*

6X 0.30
6X 0.66
2.50
0.65 PITCH

DIMENSIONS: MILLIMETERS
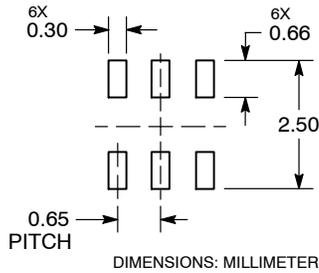
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

6

XXXM▪

1

XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42985B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SC−88/SC70−6/SOT−363		PAGE 1 OF 9

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NC7WV04

SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE Y

DATE 11 DEC 2012

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. COLLECTOR
4. EMITTER
5. BASE
6. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 6:
PIN 1. ANODE 2
2. N/C
3. CATHODE 1
4. ANODE 1
5. N/C
6. CATHODE 2

STYLE 7:
PIN 1. SOURCE 2
2. DRAIN 2
3. GATE 1
4. SOURCE 1
5. DRAIN 1
6. GATE 2

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. EMITTER 2
2. EMITTER 1
3. COLLECTOR 1
4. BASE 1
5. BASE 2
6. COLLECTOR 2

STYLE 10:
PIN 1. SOURCE 2
2. SOURCE 1
3. GATE 1
4. DRAIN 1
5. DRAIN 2
6. GATE 2

STYLE 11:
PIN 1. CATHODE 2
2. CATHODE 2
3. ANODE 1
4. CATHODE 1
5. CATHODE 1
6. ANODE 2

STYLE 12:
PIN 1. ANODE 2
2. ANODE 2
3. CATHODE 1
4. ANODE 1
5. ANODE 1
6. CATHODE 2

STYLE 13:
PIN 1. ANODE
2. N/C
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 14:
PIN 1. VREF
2. GND
3. GND
4. IOUT
5. VEN
6. VCC

STYLE 15:
PIN 1. ANODE 1
2. ANODE 2
3. ANODE 3
4. CATHODE 3
5. CATHODE 2
6. CATHODE 1

STYLE 16:
PIN 1. BASE 1
2. EMITTER 2
3. COLLECTOR 2
4. BASE 2
5. EMITTER 1
6. COLLECTOR 1

STYLE 17:
PIN 1. BASE 1
2. EMITTER 1
3. COLLECTOR 2
4. BASE 2
5. EMITTER 2
6. COLLECTOR 1

STYLE 18:
PIN 1. VIN1
2. VCC
3. VOUT2
4. VIN2
5. GND
6. VOUT1

STYLE 19:
PIN 1. I OUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF

STYLE 20:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 21:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. N/C
6. CATHODE 1

STYLE 22:
PIN 1. D1 (i)
2. GND
3. D2 (i)
4. D2 (c)
5. VBUS
6. D1 (c)

STYLE 23:
PIN 1. Vn
2. CH1
3. Vp
4. N/C
5. CH2
6. N/C

STYLE 24:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 25:
PIN 1. BASE 1
2. CATHODE
3. COLLECTOR 2
4. BASE 2
5. EMITTER
6. COLLECTOR 1

STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 27:
PIN 1. BASE 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. EMITTER 2
6. COLLECTOR 2

STYLE 28:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 29:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE/ANODE
6. CATHODE

STYLE 30:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

◊