

DUAL D-TYPE FLIP FLOP WITH PRESET AND CLEAR

- HIGH SPEED:
 $f_{MAX} = 170 \text{ MHz (TYP.) at } V_{CC} = 5\text{V}$
- LOW POWER DISSIPATION:
 $I_{CC} = 2 \mu\text{A (MAX.) at } T_A = 25^\circ\text{C}$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- POWER DOWN PROTECTION ON INPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 8 \text{ mA (MIN)}$
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC(OPR)} = 2\text{V to } 5.5\text{V}$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 74
- IMPROVED LATCH-UP IMMUNITY

DESCRIPTION

The 74VHC74 is an advanced high-speed CMOS DUAL D-TYPE FLIP FLOP WITH PRESET AND CLEAR fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology. A signal on the D INPUT is transferred to the Q OUTPUTS during the positive going transition of the clock pulse.

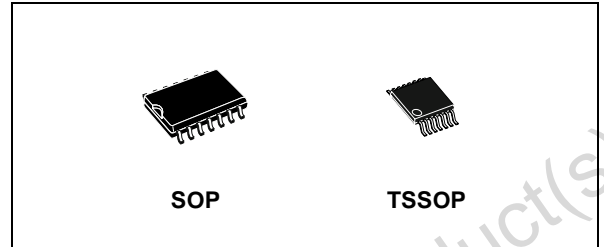


Table 1: Order Codes

PACKAGE	T & R
SOP	74VHC74MTR
TSSOP	74VHC74TTR

$\overline{\text{CLR}}$ and $\overline{\text{PR}}$ are independent of the clock and accomplished by a low setting on the appropriate input.

Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

Figure 1: Pin Connection And IEC Logic Symbols

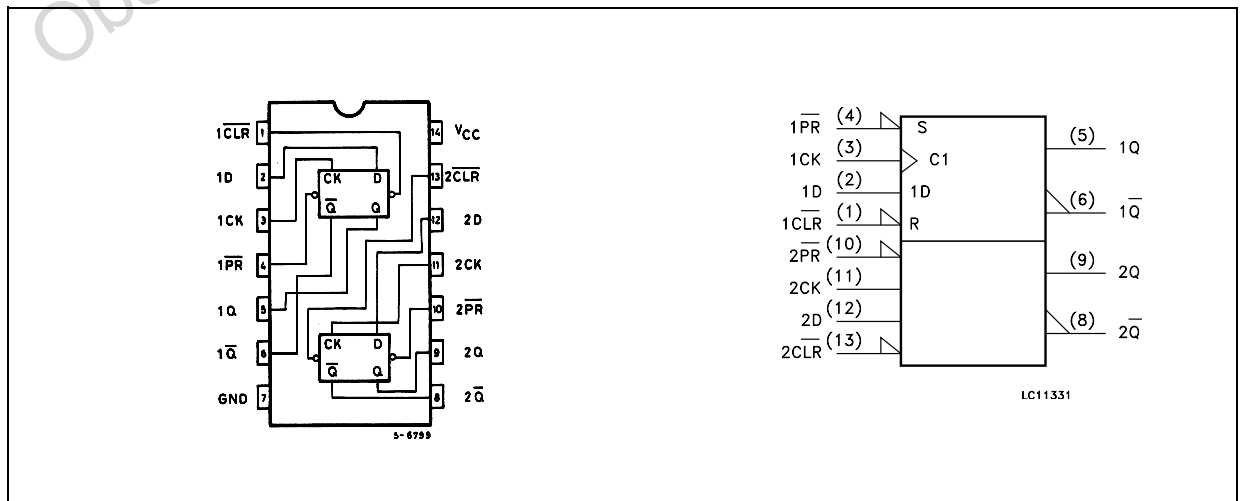


Figure 2: Input Equivalent Circuit

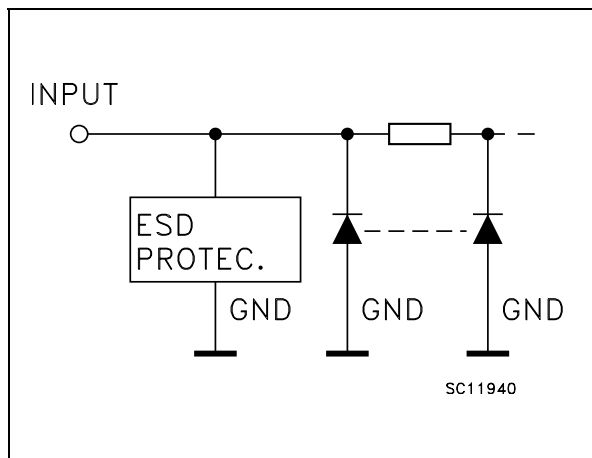


Table 2: Pin Description

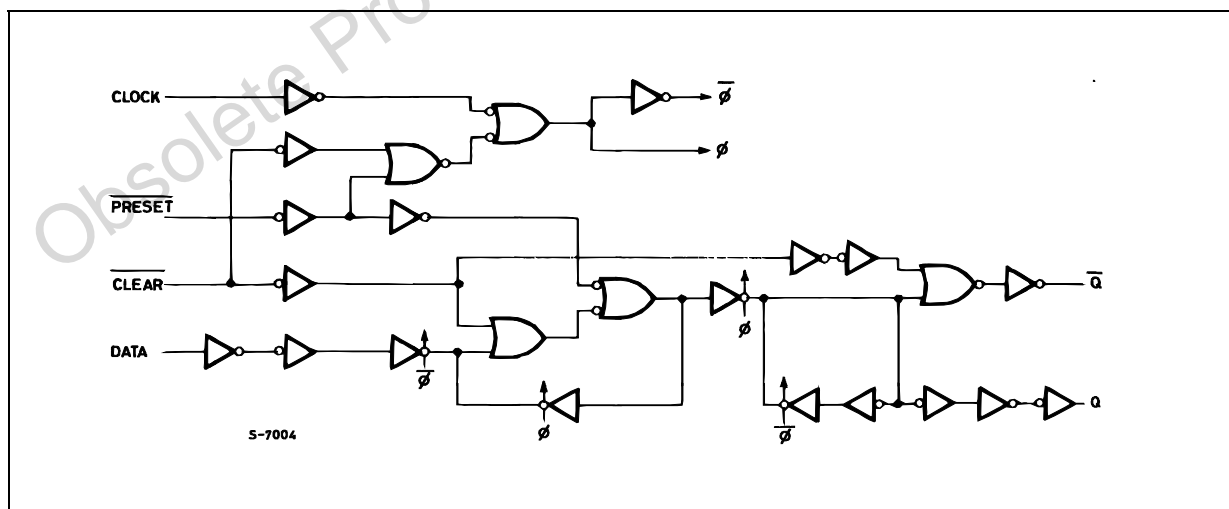
PIN N°	SYMBOL	NAME AND FUNCTION
1, 13	$\overline{1CLR}$, $\overline{2CLR}$	Asynchronous Reset - Direct Input
2, 12	1D, 2D	Data Inputs
3, 11	1CK, 2CK	Clock Input (LOW to HIGH, Edge Triggered)
4, 10	1PR, 2PR	Asynchronous Set - Direct Input
5, 9	1Q, 2Q	True Flip-Flop Outputs
6, 8	1 \overline{Q} , 2 \overline{Q}	Complement Flip-Flop Outputs
7	GND	Ground (0V)
14	V _{CC}	Positive Supply Voltage

Table 3: Truth Table

INPUTS				OUTPUTS		FUNCTION
\overline{CLR}	\overline{PR}	D	CK	Q	\overline{Q}	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	
H	H	L		L	H	
H	H	H		H	L	
H	H	X		Q _n	\overline{Q}_n	NO CHANGE

X : Don't Care

Figure 3: Logic Diagram



This logic diagram has not be used to estimate propagation delays

Table 4: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	-0.5 to +7.0	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	- 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

Table 5: Recommended Operating Conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 5.5	V
V_I	Input Voltage	0 to 5.5	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (note 1) ($V_{CC} = 3.3 \pm 0.3V$) ($V_{CC} = 5.0 \pm 0.5V$)	0 to 100 0 to 20	ns/V

1) V_{IN} from 30% to 70% of V_{CC}

Table 6: DC Specifications

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		3.0 to 5.5		0.7V _{CC}			0.7V _{CC}		0.7V _{CC}		
V _{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		3.0 to 5.5				0.3V _{CC}		0.3V _{CC}		0.3V _{CC}	
V _{OH}	High Level Output Voltage	2.0	I _O =-50 μA	1.9	2.0		1.9		1.9		V
		3.0	I _O =-50 μA	2.9	3.0		2.9		2.9		
		4.5	I _O =-50 μA	4.4	4.5		4.4		4.4		
		3.0	I _O =-4 mA	2.58			2.48		2.4		
		4.5	I _O =-8 mA	3.94			3.8		3.7		
V _{OL}	Low Level Output Voltage	2.0	I _O =50 μA		0.0	0.1		0.1		0.1	V
		3.0	I _O =50 μA		0.0	0.1		0.1		0.1	
		4.5	I _O =50 μA		0.0	0.1		0.1		0.1	
		3.0	I _O =4 mA			0.36		0.44		0.55	
		4.5	I _O =8 mA			0.36		0.44		0.55	
I _I	Input Leakage Current	0 to 5.5	V _I = 5.5V or GND			± 0.1		± 1		± 1	μA
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND			2		20		20	μA

Table 7: AC Electrical Characteristics (Input $t_r = t_f = 3\text{ns}$)

Symbol	Parameter	Test Condition			Value						Unit	
		V_{CC} (V)	C_L (pF)	$T_A = 25^\circ\text{C}$			-40 to 85°C		-55 to 125°C			
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Time CK to Q or \bar{Q}	3.3(*)	15			6.7	11.9	1.0	14.0	1.0	14.0	ns
		3.3(*)	50			9.2	15.4	1.0	17.5	1.0	17.5	
		5.0(**)	15			4.6	7.3	1.0	8.5	1.0	8.5	
		5.0(**)	50			6.1	9.3	1.0	10.5	1.0	10.5	
t_{PLH} t_{PHL}	Propagation Delay Time \bar{PR} or CLR to Q or \bar{Q}	3.3(*)	15			7.6	12.3	1.0	14.5	1.0	14.5	ns
		3.3(*)	50			10.1	15.8	1.0	18.0	1.0	18.0	
		5.0(**)	15			4.8	7.7	1.0	9.0	1.0	9.0	
		5.0(**)	50			6.3	9.7	1.0	11.0	1.0	11.0	
t_W	CK Pulse Width HIGH or LOW	3.3(*)					6.0		7.0		7.0	ns
		5.0(**)						5.0		5.0		
t_W	PR or CLR Pulse Width LOW	3.3(*)					6.0		7.0		7.0	ns
		5.0(**)						5.0		5.0		
t_s	Setup Time D to CK HIGH or LOW	3.3(*)					6.0		7.0		7.0	ns
		5.0(**)						5.0		5.0		
t_h	Hold Time D to CK HIGH or LOW	3.3(*)					0.5		0.5		0.5	ns
		5.0(**)						0.5		0.5		
t_{REM}	Removal Time \bar{PR} or CLR to CK	3.3(*)					5.0		5.0		5.0	ns
		5.0(**)						3.0		3.0		
f_{MAX}	Maximum Clock Frequency	3.3(*)	15		80	125		70		70		MHz
		3.3(*)	50		50	75		45		45		
		5.0(**)	15		130	170		110		110		
		5.0(**)	50		90	115		75		75		

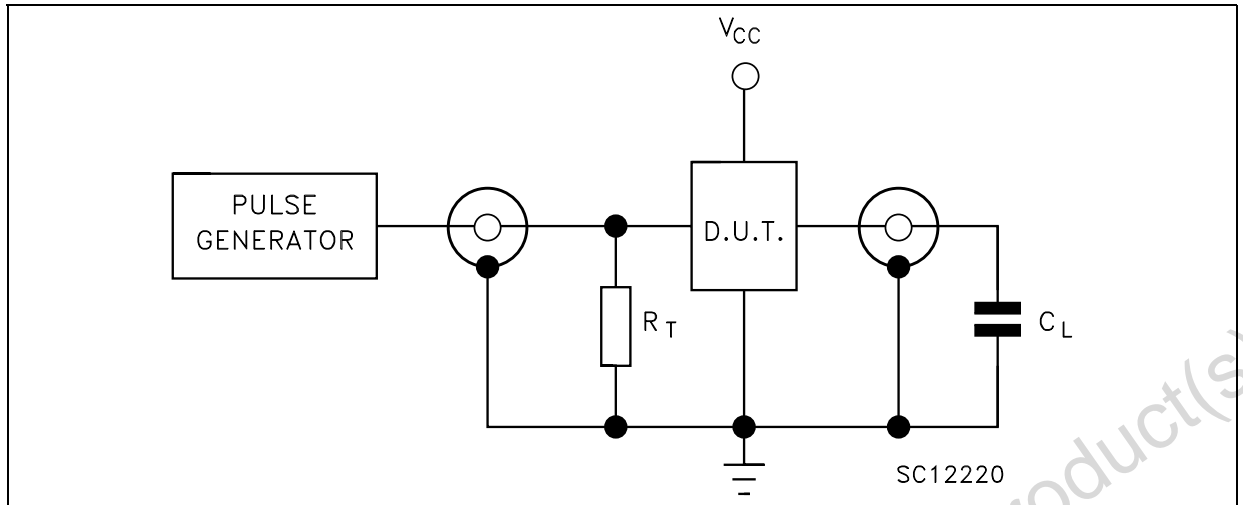
(*) Voltage range is $3.3\text{V} \pm 0.3\text{V}$ (**) Voltage range is $5.0\text{V} \pm 0.5\text{V}$

Table 8: Capacitive Characteristics

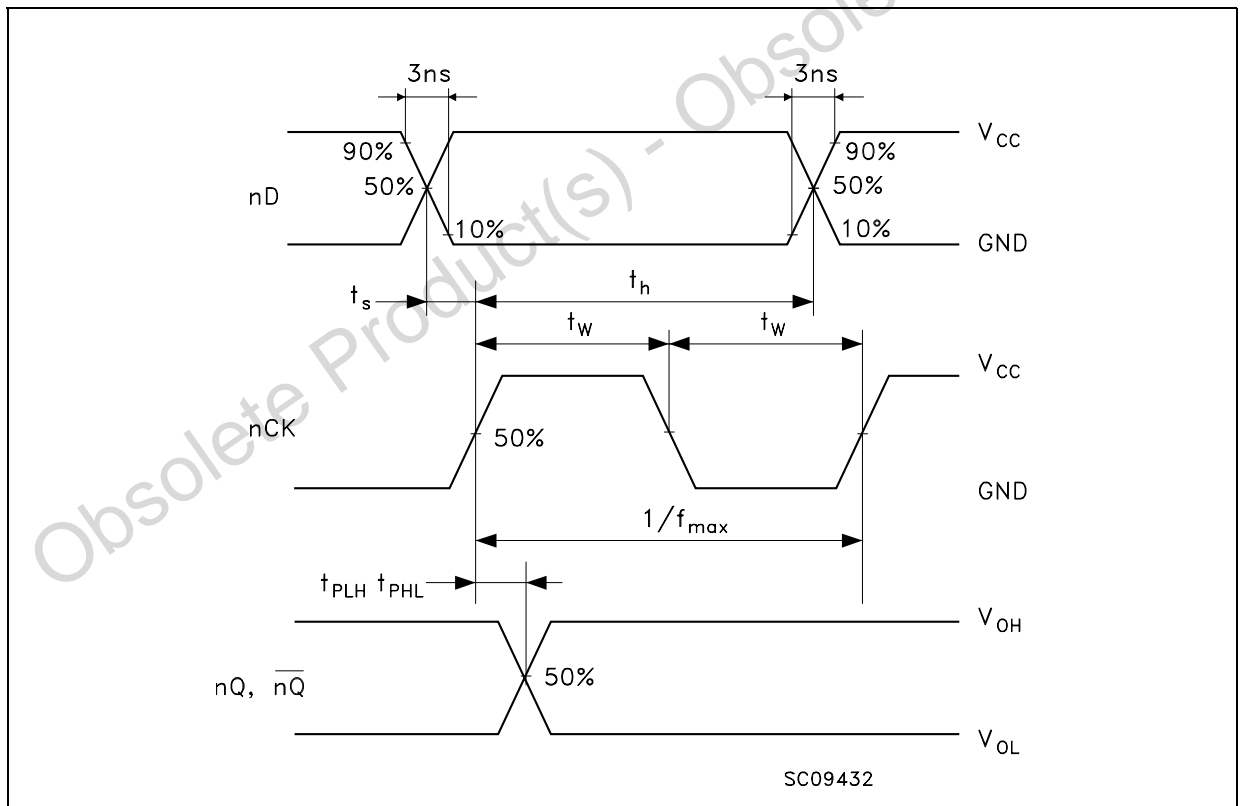
Symbol	Parameter	Test Condition			Value						Unit	
		V_{CC} (V)			$T_A = 25^\circ\text{C}$			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C_{IN}	Input Capacitance	5.0				7	10		10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)	5.0	$f_{IN} = 10\text{MHz}$			25						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/2$ (per flip-flop)

Figure 4: Test Circuit



$C_L = 15/50\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 5: Waveform - Propagation Delays, Setup And Hold Times ($f=1\text{MHz}$; 50% duty cycle)

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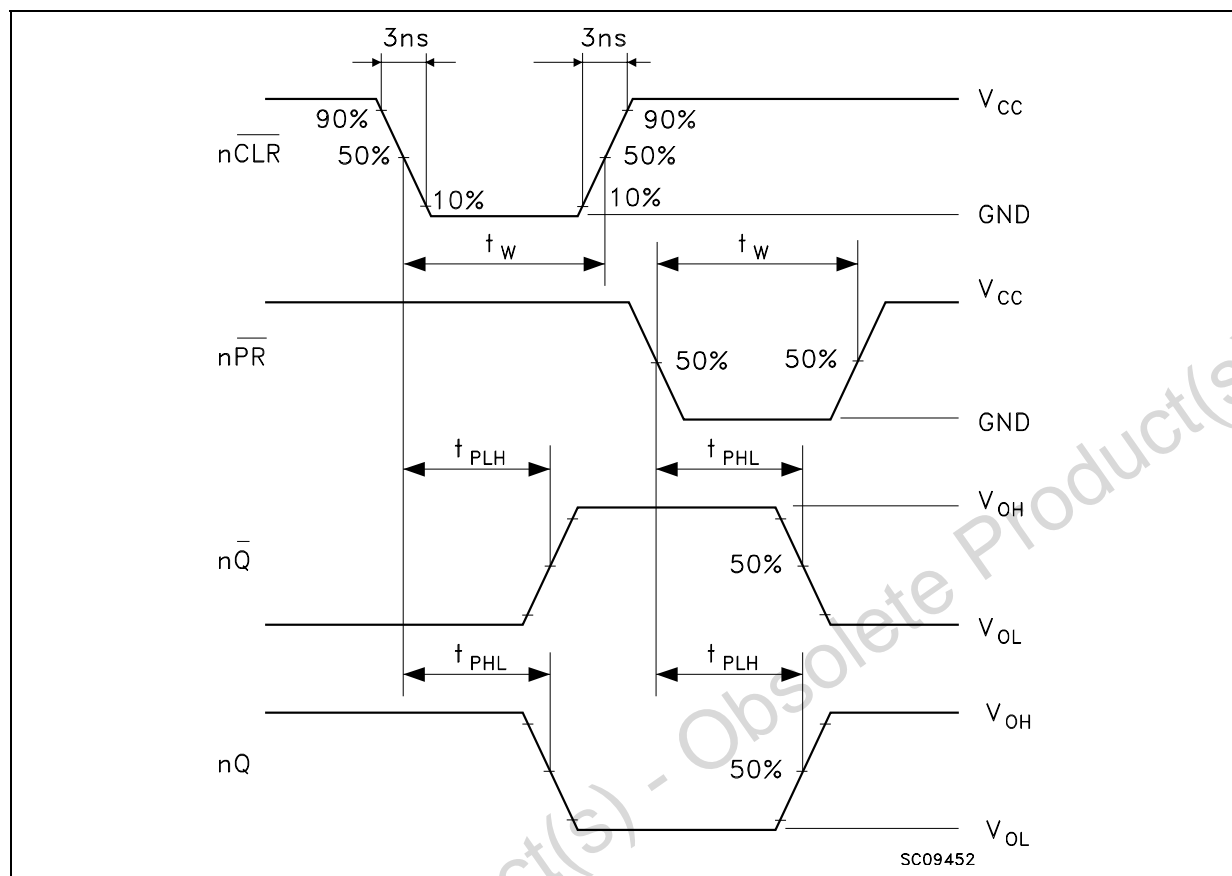
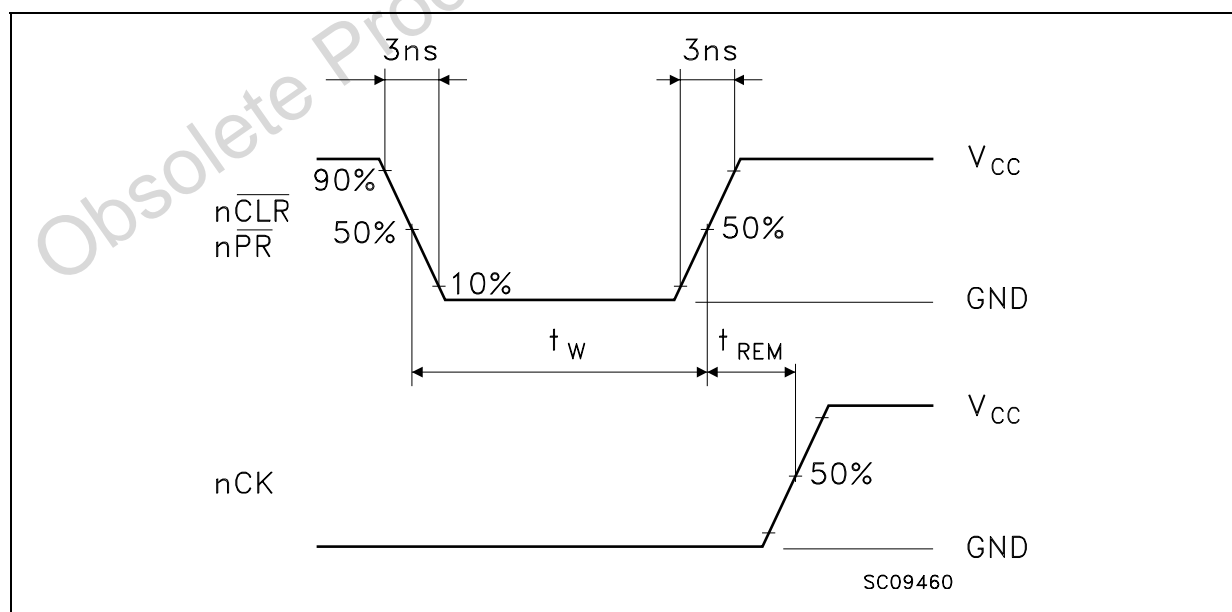
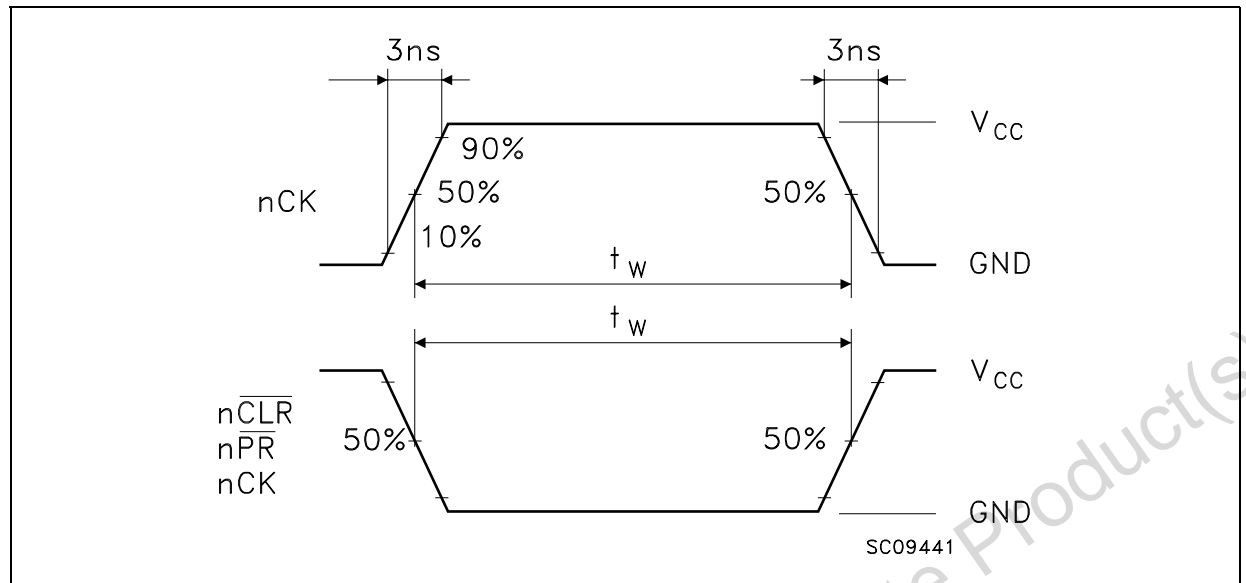
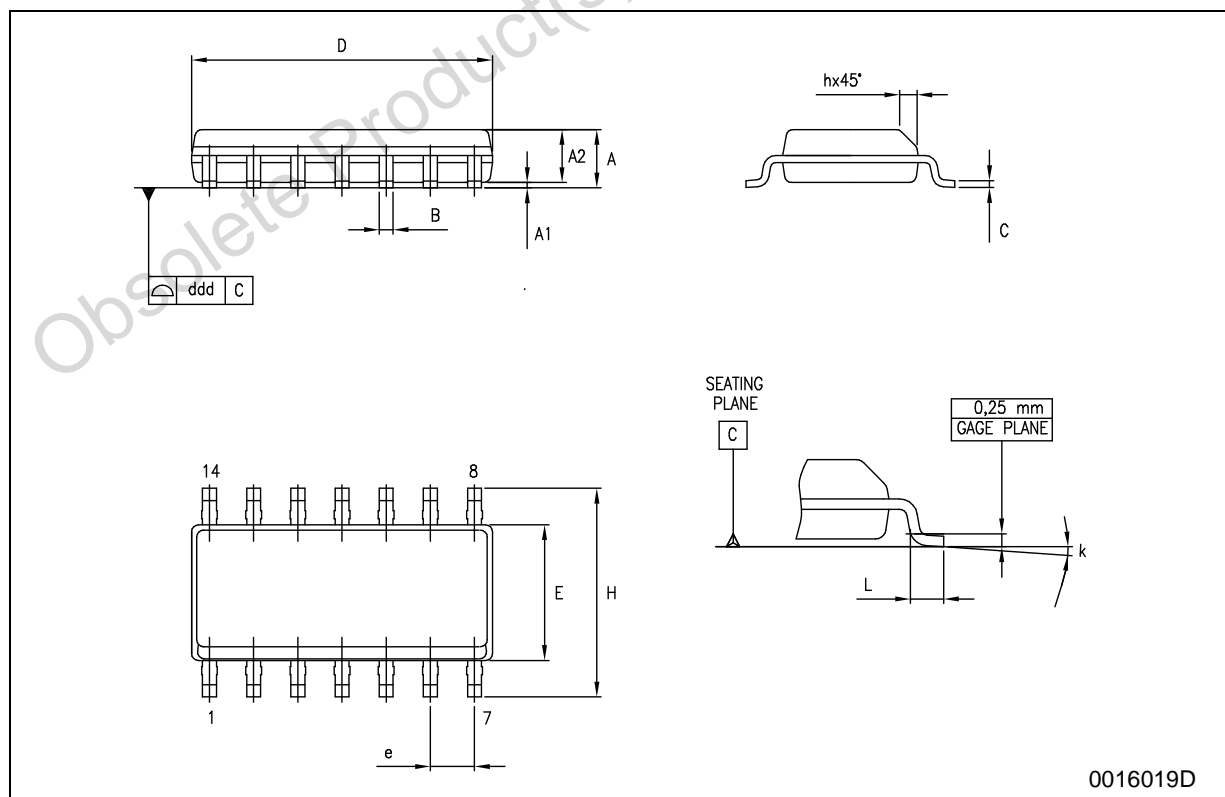
Figure 6: WAVEFORM 2: PROPAGATION DELAYS ($f=1\text{MHz}$; 50% duty cycle)Figure 7: Waveform - Recovery Times ($f=1\text{MHz}$; 50% duty cycle)

Figure 8: Waveform - Pulse Width



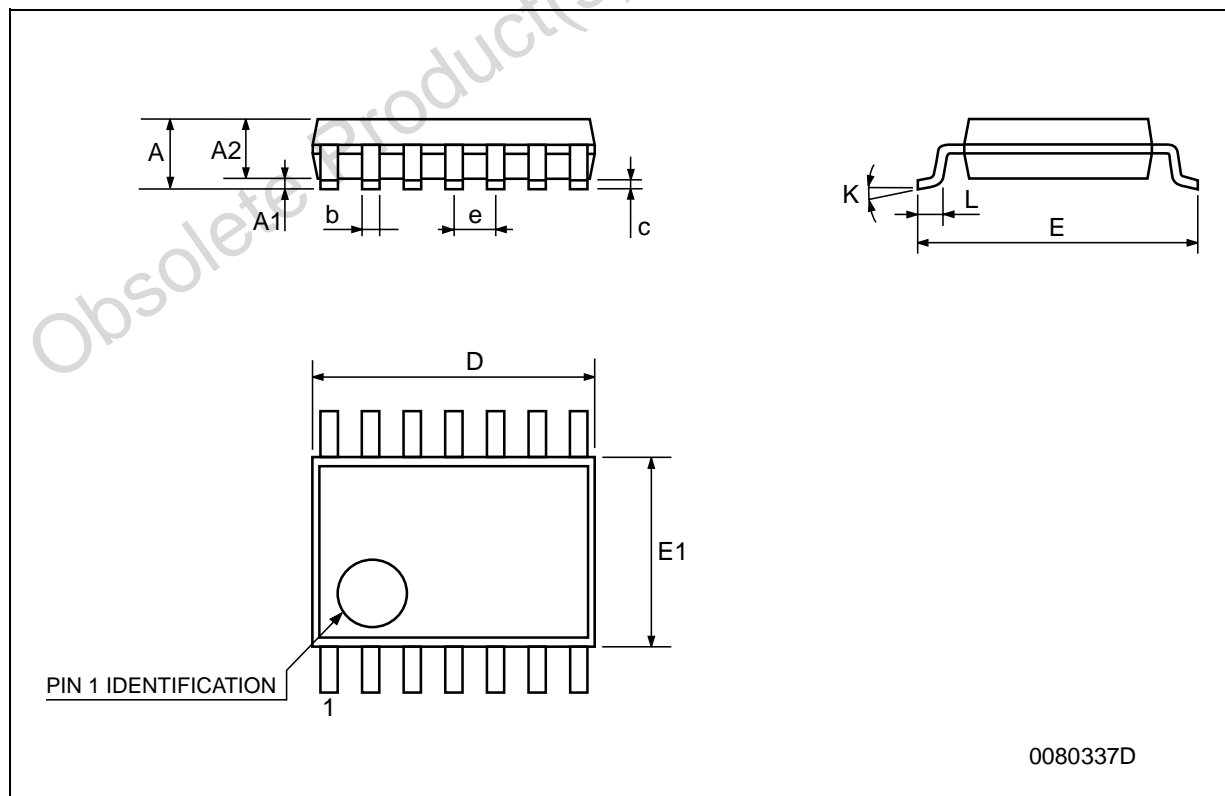
SO-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.1		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	8.55		8.75	0.337		0.344
E	3.8		4.0	0.150		0.157
e		1.27			0.050	
H	5.8		6.2	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.4		1.27	0.016		0.050
k	0°		8°	0°		8°
ddd			0.100			0.004



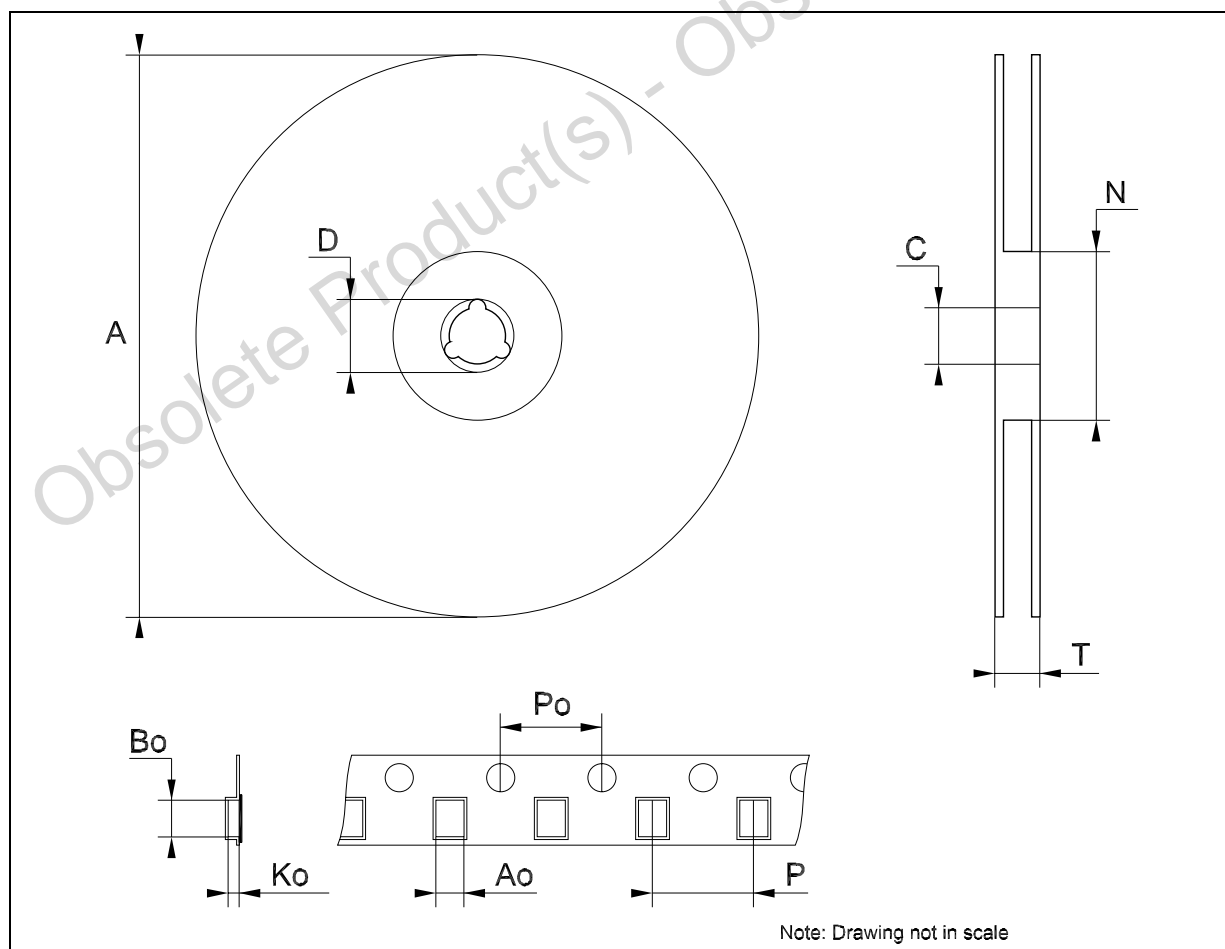
TSSOP14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



Tape & Reel SO-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.4		6.6	0.252		0.260
Bo	9		9.2	0.354		0.362
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Tape & Reel TSSOP14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.7		6.9	0.264		0.272
Bo	5.3		5.5	0.209		0.217
Ko	1.6		1.8	0.063		0.071
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319

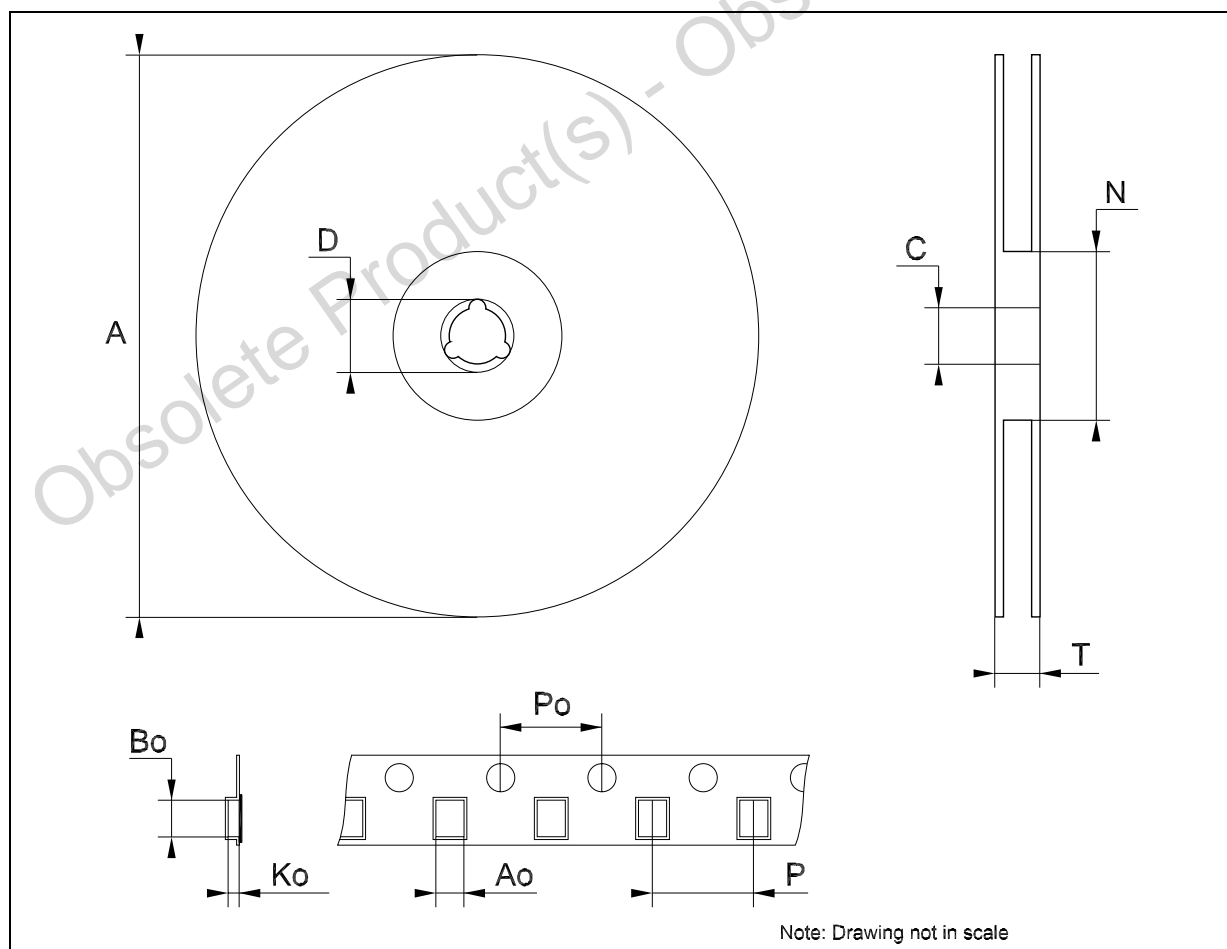


Table 9: Revision History

Date	Revision	Description of Changes
12-Nov-2004	4	Order Codes Revision - pag. 1.

Obsolete Product(s) - Obsolete Product(s)

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