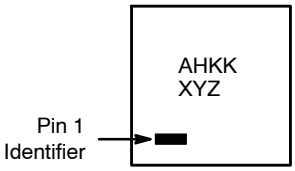
TinyLogic® Low Power Configurable Gate with Voltage-Level Translator

74AUP1T97

UDFN6
CASE 517DP

SIP6
CASE 127EB

MARKING DIAGRAM



AH = Specific Device Code
KK = Lot Code
XY = Date Code
Z = Assembly Plant Code

ORDERING INFORMATION

Device	Package	Shipping†
74AUP1T97FHX	UDFN−6 (Pb-Free/Halide Free)	5000 / Tape & Reel
74AUP1T97L6X	SIP−6 (Pb-Free/Halide Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Description

The 74AUP1T97 is a universal configurable 2−input logic gate that provides single supply voltage level translation. This device is designed for applications with inputs switching levels that accept 1.8 V low voltage CMOS signals while operating from either a single 2.5 V or 3.3 V supply voltage. The 74AUP1T97 is an ideal low power solution for mixed voltage signal applications especially for battery−powered portable applications. This product guarantees very low static and dynamic power consumption across entire voltage range. All inputs are implemented with hysteresis to allow for slower transition input signals and better switching noise immunity.

The 74AUP1T97 provides for multiple functions as determined by various configurations of the three inputs. The potential logic functions provided are MUX, AND, NAND, OR, and NOR, inverter and buffer. Refer to Figures 3 to 9.

Features

- Single Supply Voltage Translator
  - 1.8 V to 3.3 V Input at V_{CC} = 3.3 V
  - 1.8 V to 2.5 V Input at V_{CC} = 2.5 V
- 2.3 V to 3.6 V V_{CC} Supply Voltage Operation
- 3.6 V Over−Voltage Tolerant I/O's at V_{CC} from 2.3 V to 3.6 V
- Power−Off High−Impedance Inputs and Outputs
- Low Static Power Consumption
  - I_{CC} = 0.9 μA Maximum
- Low Dynamic Power Consumption
  - C_{PD} = 2.7 pF Typical at 3.3 V
- Ultra−Small MicroPak™ Packages

Logic Diagram

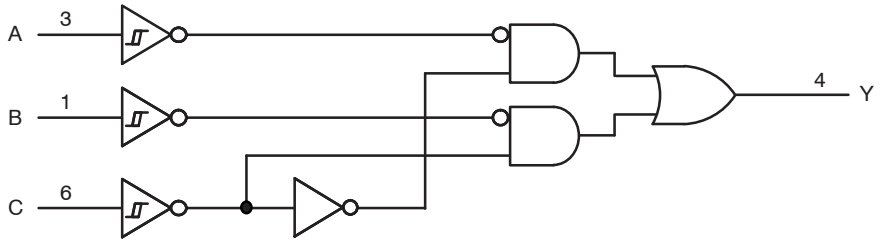


Figure 1. Logic Diagram (Positive Logic)

PIN CONFIGURATIONS

Table 1. PIN DESCRIPTIONS

Pin	Name	Description
1	B	Data Input
2	GND	Ground
3	A	Data Input
4	Y	Output
5	V_{CC}	Supply Voltage
6	C	Data Input

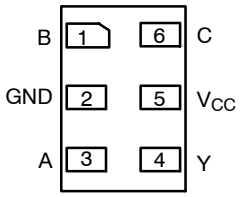


Figure 2. MicroPak™ (Top View)

Table 2. FUNCTION TABLE

Inputs			Output
C	**B**	**A**	**Y**
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

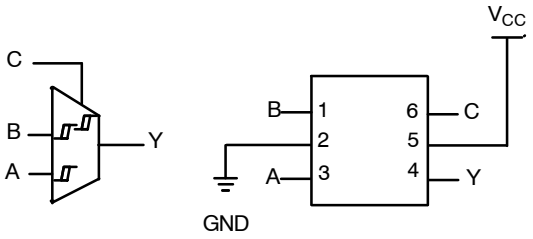
1. H = HIGH Logic Level
2. L = LOW Logic Level

Table 3. FUNCTION SELECTION TABLE

Logic Function	Connection Configuration
2−to−1 MUX	Figure 3
2−Input AND Gate	Figure 4
2−Input OR Gate with One Inverted Input	Figure 5
2−Input NAND Gate with One Inverted Input	Figure 5
2−Input AND Gate with One Inverted Input	Figure 6
2−Input NOR Gate with One Inverted Input	Figure 6
2−Input OR Gate	Figure 7
Inverter	Figure 8
Buffer	Figure 9

Logic Configurations

Figure 3 through Figure 9 show the logical functions that can be implemented using the 74AUP1T97. The diagrams show the DeMorgan's equivalent logic duals for a given two−input function. The logical implementation is next to the board−level physical implementation of how the pins of the function should be connected.



Note:
1. When C is L, Y = B.
2. When C is H, Y = A.

Figure 3. 2−to−1 MUX

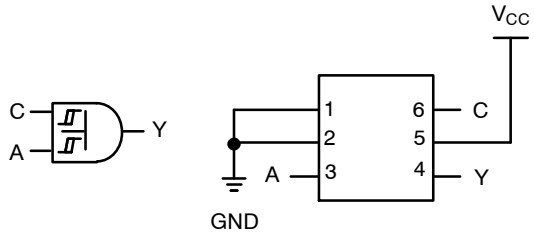


Figure 4. 2−Input AND Gate

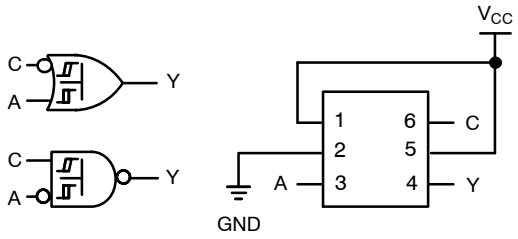


Figure 5. Input OR Gate with One Inverted Input 2−Input NAND Gate with One Inverted Input

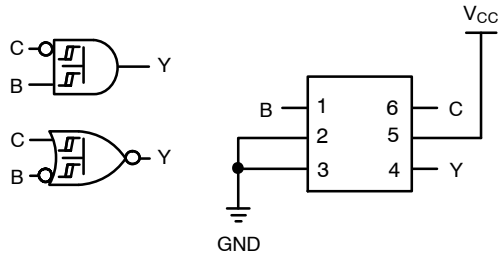


Figure 6. 2−Input AND Gate with One Inverted Input 2−Input NOR Gate with One Inverted Input

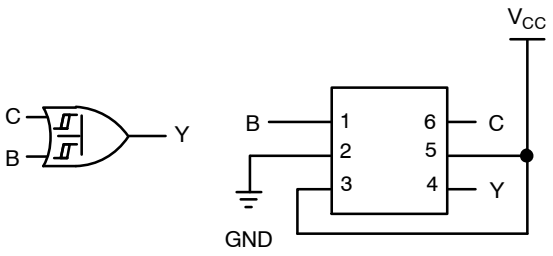


Figure 7. 2−Input OR Gate

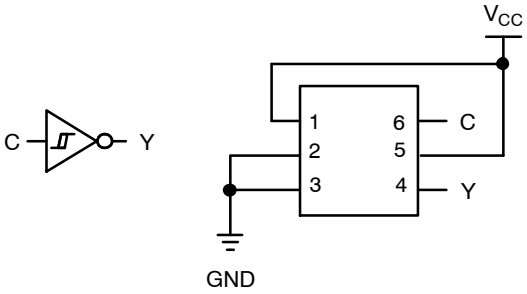


Figure 8. Inverter

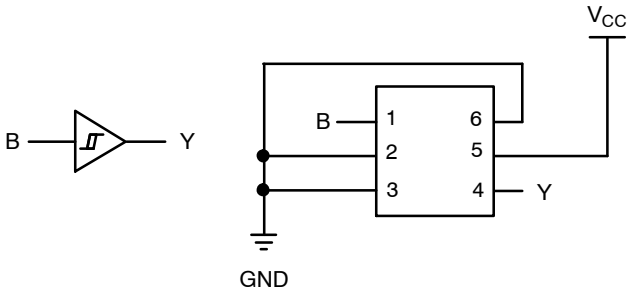


Figure 9. Buffer

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		−0.5	4.6	V
V_{IN}	DC Input Voltage		−0.5	4.6	V
V_{OUT}	DC Output Voltage	HIGH or LOW State(Note 3) V_{CC} = 0 V	−0.5 −0.5	V_{CC} + 0.5 4.6	V
I_{IK}	DC Input Diode Current	V_{IN} < 0 V	−	−50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < 0 V V_{OUT} > V_{CC}	−	−50 +50	mA
I_{OH} / I_{OL}	DC Output Source / Sink Current		−	±50	mA
IO	Continuous Output Current		−	±20	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Supply Pin		−	±50	mA
T_{STG}	Storage Temperature Range		−65	+150	°C
T_J	Junction Temperature Under Bias		−	+150	°C
T_L	Junction Lead Temperature, Soldering 10s		−	+260	°C
P_D	Power Dissipation at +85°C	MicroPak−6 MicroPak2−6	−	130 120	mW
ESD	Human Body Model, JEDEC:JESD22−A114 Charged Device Model, JEDEC:JESD22−C101		−	5000+ 2000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. I_O absolute maximum rating must be observed.

Table 4. RECOMMENDED OPERATING CONDITIONS (Note 4)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage		2.3	3.6	V
V_{IN}	Input Voltage		0	3.6	V
V_{OUT}	Output Voltage	V_{CC} = 0 V HIGH or LOW State	0 0	3.6 V_{CC}	V
I_{OH} / I_{OL}	Output Current	V_{CC} = 3.0 V to 3.6 V V_{CC} = 2.3 V to 2.7 V	−	±4.0 ±3.1	mA
T_A	Operating Free−Air Temperature		−40	+85	°C
θ_{JA}	Thermal Resistance	MicroPak−6 MicroPak2−6	−	500 560	°C/W

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must be held HIGH or LOW. They may not float.

Table 5. DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = +25°C		T_A = −40°C to +85°C		Unit
				Min	Max	Min	Max	
V_P	Positive Threshold Voltage	–	2.3 V to 2.7 V	0.60	1.10	0.60	1.10	V
			3.0 V to 3.6 V	0.75	1.16	0.75	1.19	V
V_N	Negative Threshold Voltage	–	2.3 V to 2.7 V	0.35	0.60	0.35	0.60	V
			3.0 V to 3.6 V	0.50	0.85	0.50	0.85	V
V_H	Hysteresis Voltage	–	2.3 V to 2.7 V	0.23	0.60	0.10	0.60	V
			3.0 V to 3.6 V	0.25	0.56	0.15	0.56	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −20 μA	2.3 V ≤ V_{CC} ≤ 3.6 V	V_{CC} −0.1	–	V_{CC} −0.1	–	V
		I_{OH} = −2.3 mA	2.3 V	2.05	–	1.97	–	V
		I_{OH} = −3.1 mA		1.90	–	1.85	–	V
		I_{OH} = −2.7 mA	3.0 V	2.72	–	2.67	–	V
		I_{OH} = −4 mA		2.60	–	2.55	–	V
V_{OL}	LOW Level Output Voltage	I_{OL} = 20 μA	2.3 V ≤ V_{CC} ≤ 3.6 V	–	0.10	–	0.10	V
		I_{OL} = 2.3 mA	2.3 V	–	0.31	–	0.33	V
		I_{OH} = 3.1 mA		–	0.44	–	0.45	V
		I_{OL} = 2.7 mA	3.0 V	–	0.31	–	0.33	V
		I_{OL} = 4.0 mA		–	0.44	–	0.45	V
I_{IN}	Input Leakage Current	0 ≤ V_{IN} ≤ 3.6	0 V to 3.6 V	–	±0.10	–	±0.50	μA
I_{OFF}	Power Off Leakage Current	0 ≤ (V_{IN},V_O) ≤ 3.6	0 V	–	0.10	–	0.50	μA
ΔI_{OFF}	Additional Power Off Leakage Current	V_{IN} or V_O = 0 V to 3.6 V	0 V to 0.2 V	–	0.20	–	0.60	μA
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND	2.3 V to 3.6 V	–	0.50	–	0.90	μA
		V_{CC} ≤ V_{IN} ≤ 3.6 V		–	–	–	±0.90	μA
ΔI_{CC}	Increase in I_{CC} per Input	One Input at 0.3 V or 1.1 V, other Inputs at 0 or V_{CC}	2.3 V to 2.7 V	–	–	–	4	μA
		One Input at 0.45 V or 1.2 V, other Inputs at 0 or V_{CC}	3.0 V to 3.6 V	–	–	–	12	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 6. AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = +25°C			T_A = −40 to +85°C		Unit	Figure
				Min	Typ	Max	Typ	Max		
t_{PHL}, t_{PLH}	Propagation Delay	C_L = 5 pF, R_L = 1 MΩ	2.30 V ≤ V_{CC} ≤ 2.70 V, V_{IN} = 1.65 V to 1.95 V	1.1	3.7	5.5	1.1	6.8	ns	Figure 10 & 11
			2.30 V ≤ VCC ≤ 2.70 V V_{IN} = 2.30 V to 2.70 V	1.1	3.8	6.5	1.1	7.0		
			2.30 V ≤ V_{CC} ≤ 2.70 V, V_{IN} = 3.0 V to 3.60 V	1.1	3.9	6.0	1.1	6.5		
			3.00 V ≤ V_{CC} ≤ 3.60 V, V_{IN} = 1.65 V to 1.95 V	1.0	3.3	4.9	1.0	8.0		
			3.00 V ≤ V_{CC} ≤ 3.60 V, V_{IN} = 2.30 V to 2.70 V	1.0	3.2	4.6	1.0	5.8		
			3.00 V ≤ V_{CC} ≤ 3.60 V, V_{IN} = 3.00 V to 3.60 V	1.0	3.1	4.7	1.0	5.5		
		C_L = 10 pF, R_L = 1 MΩ	2.30 V ≤ V_{CC} ≤ 2.70 V, V_{IN} = 1.65 V to 1.95 V	1.3	4.1	6.5	1.0	7.9		
			2.30 V ≤ V_{CC} ≤ 2.70 V, V_{IN} = 2.30 V to 2.70 V	1.3	4.0	6.2	1.0	7.1		
			2.30 V ≤ V_{CC} ≤ 2.70 V, V_{IN} = 3.0 V to 3.60 V	1.3	3.7	5.7	1.0	6.5		
			3.00 V ≤ V_{CC} ≤ 3.60 V, V_{IN} = 1.65 V to 1.95 V	1.3	3.5	5.6	1.0	8.5		
			3.00 V ≤ V_{CC} ≤ 3.60 V, V_{IN} = 2.30 V to 2.70 V	1.3	3.4	5.3	1.0	6.1		
			3.00 V ≤ V_{CC} ≤ 3.60 V, V_{IN} = 3.00 V to 3.60 V	1.3	3.3	5.2	1.0	5.9		
		C_L = 15 pF, R_L = 1 MΩ	2.30 V ≤ V_{CC} ≤ 2.70 V, V_{IN} = 1.65 V to 1.95 V	1.5	4.6	6.9	1.0	8.7		
			2.30 V ≤ V_{CC} ≤ 2.70 V, V_{IN} = 2.30 V to 2.70 V	1.5	4.4	6.8	1.0	7.9		
			2.30V ≤ V_{CC} ≤ 2.70 V, V_{IN} = 3.0 V to 3.60 V	1.5	4.2	6.3	1.0	7.4		
			3.00 V ≤ V_{CC} ≤ 3.60 V, V_{IN} = 1.65 V to 1.95 V	1.3	3.9	6.2	1.0	9.1		
			3.00 V ≤ V_{CC} ≤ 3.60 V, V_{IN} = 2.30 V to 2.70 V	1.3	3.8	5.6	1.0	6.8		
			3.00 V ≤ V_{CC} ≤ 3.60 V, V_{IN} = 3.00 V to 3.60 V	1.3	3.8	5.6	1.0	6.2		
		C_L = 30 pF, R_L = 1 MΩ	2.30 V ≤ V_{CC} ≤ 2.70 V, V_{IN} = 1.65 V to 1.95 V	1.3	4.2	7.9	1.3	8.5		
			2.30 V ≤ V_{CC} ≤ 2.70 V, V_{IN} = 2.30 V to 2.70 V	1.3	3.9	7.9	1.3	8.5		
			2.30V ≤ V_{CC} ≤ 2.70 V, V_{IN} = 3.0 V to 3.60 V	1.0	3.7	7.3	1.0	8.9		
			3.00 V ≤ V_{CC} ≤ 3.60 V, V_{IN} = 1.65 V to 1.95 V	1.3	3.5	6.1	1.3	7.9		
			3.00V ≤ V_{CC} ≤ 3.60 V, V_{IN} = 2.30 V to 2.70 V	1.1	3.0	5.9	1.1	6.8		
			3.00 V ≤ V_{CC} ≤ 3.60 V, V_{IN} = 2.30 V to 2.70 V	1.0	2.7	5.7	1.0	6.5		
C_{IN}	Input Capacitance	–	0	–	2.1	–	–	–	pF	–
C_{OUT}	Output Capacitance	–	0	–	3.0	–	–	–		
C_{PD}	Power Dissipation Capacitance	–	2.30 V ≤ V_{CC} ≤ 2.70 V	–	2.0	–	–	–		
			3.00 V ≤ V_{CC} ≤ 3.60 V	–	2.7	–	–	–		

AC LOADINGS AND WAVEFORMS

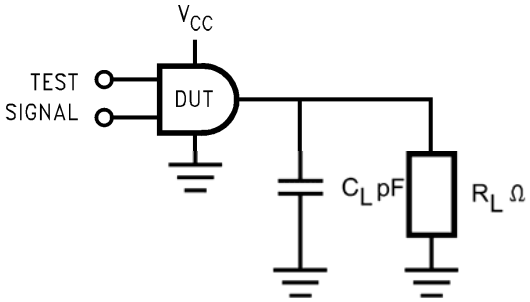


Figure 10. AC Test Circuit

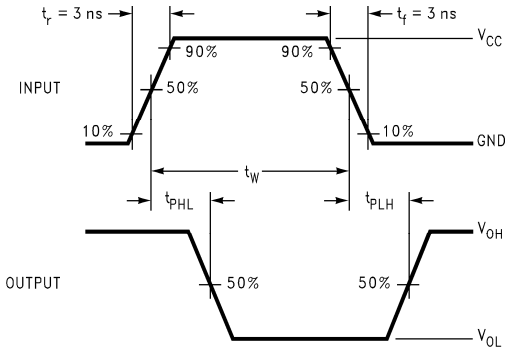


Figure 11. AC Waveforms

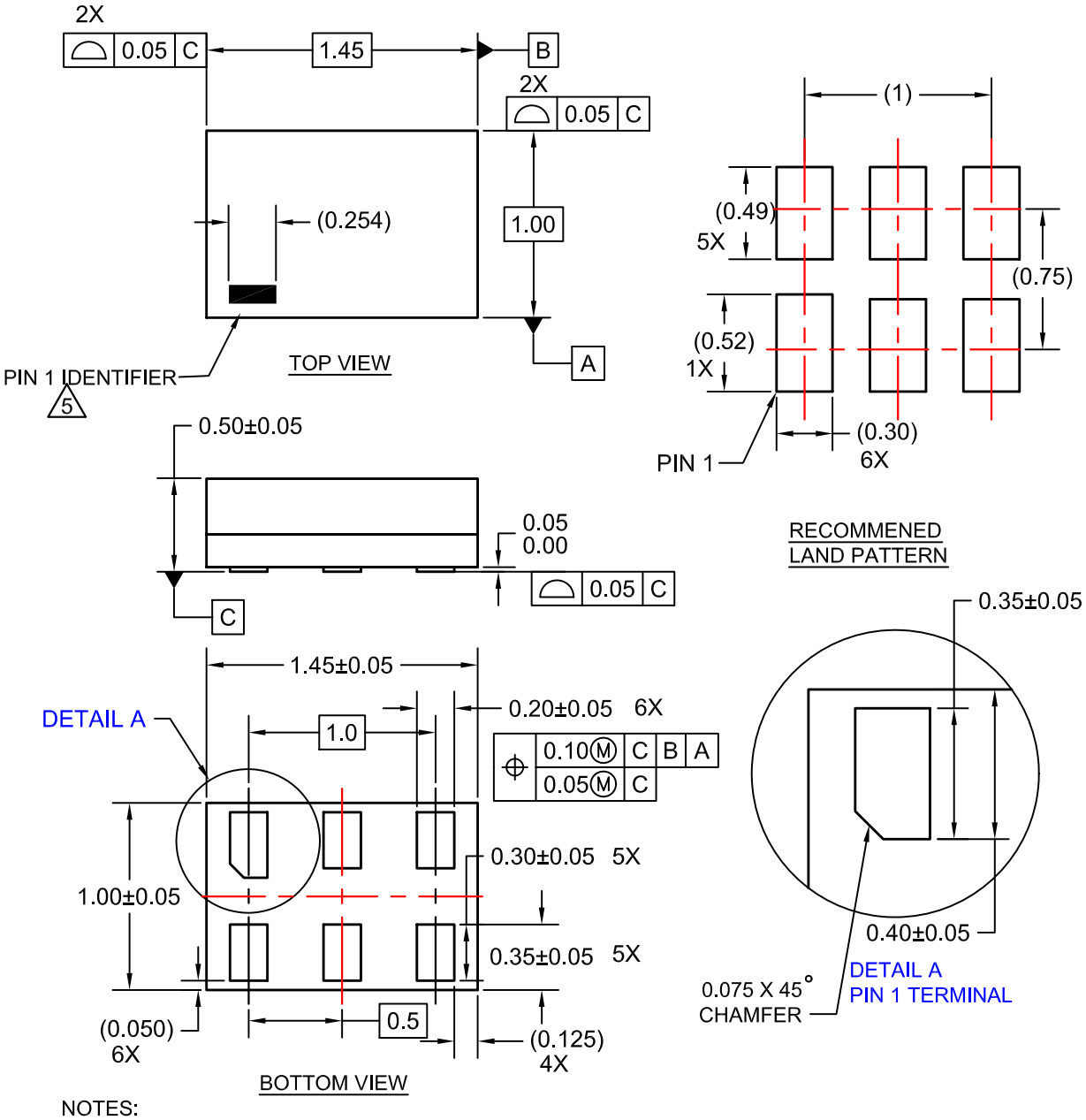
Symbol	V_{CC}	
	3.3 V ±0.3 V	**2.5 V ±0.2 V**
V_{mi}	V_{IN} / 2	V_{IN} / 2
V_{mo}	V_{CC} / 2	V_{CC} / 2

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SIP6 1.45X1.0
CASE 127EB
ISSUE O

DATE 31 AUG 2016



NOTES:

1. CONFORMS TO JEDEC STANDARD MO-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-2009
4. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

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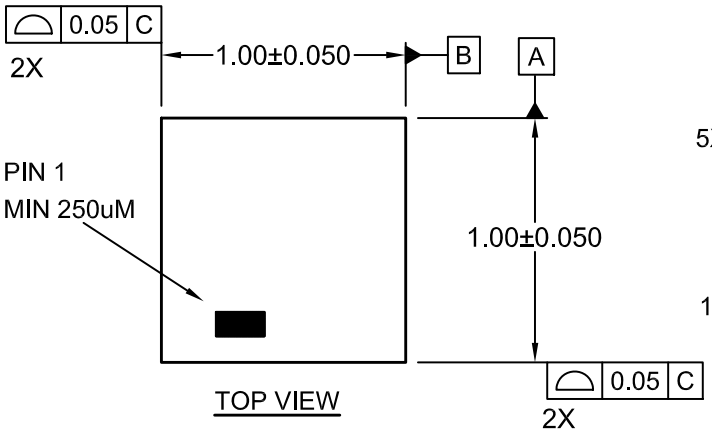
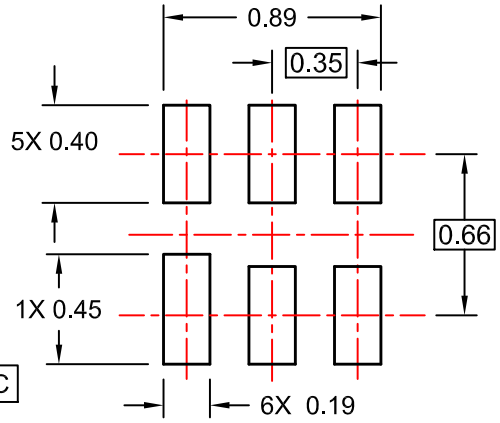
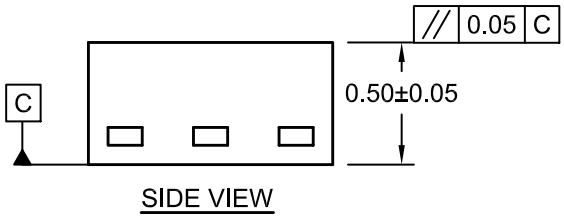
UDFN6 1.0X1.0, 0.35P
CASE 517DP
ISSUE O

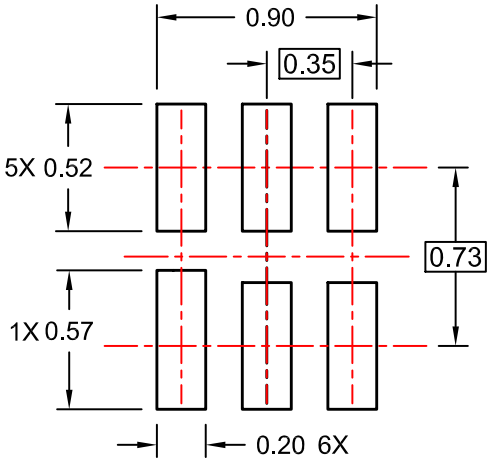
DATE 31 AUG 2016



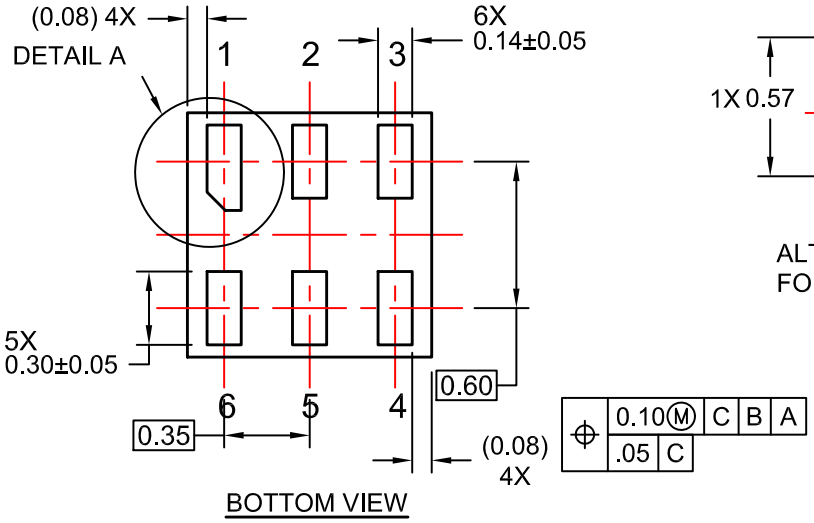


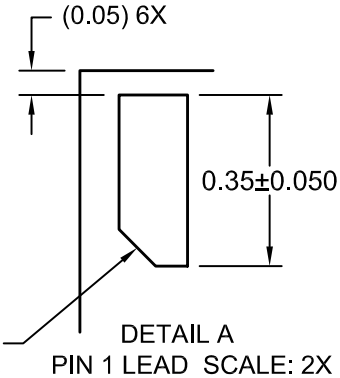
RECOMMENDED LAND PATTERN
FOR SPACE CONSTRAINED PCB





ALTERNATIVE LAND PATTERN
FOR UNIVERSAL APPLICATION





NOTES:

A. COMPLIES TO JEDEC MO-252 STANDARD
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009

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