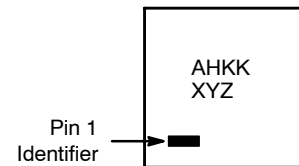


# TinyLogic® Low Power Configurable Gate with Voltage-Level Translator

## 74AUP1T97



### MARKING DIAGRAM



AH = Specific Device Code  
 KK = Lot Code  
 XY = Date Code  
 Z = Assembly Plant Code

### Description

The 74AUP1T97 is a universal configurable 2-input logic gate that provides single supply voltage level translation. This device is designed for applications with inputs switching levels that accept 1.8 V low voltage CMOS signals while operating from either a single 2.5 V or 3.3 V supply voltage. The 74AUP1T97 is an ideal low power solution for mixed voltage signal applications especially for battery-powered portable applications. This product guarantees very low static and dynamic power consumption across entire voltage range. All inputs are implemented with hysteresis to allow for slower transition input signals and better switching noise immunity.

The 74AUP1T97 provides for multiple functions as determined by various configurations of the three inputs. The potential logic functions provided are MUX, AND, NAND, OR, and NOR, inverter and buffer. Refer to Figures 3 to 9.

### Features

- Single Supply Voltage Translator
  - ◆ 1.8 V to 3.3 V Input at  $V_{CC} = 3.3$  V
  - ◆ 1.8 V to 2.5 V Input at  $V_{CC} = 2.5$  V
- 2.3 V to 3.6 V  $V_{CC}$  Supply Voltage Operation
- 3.6 V Over-Voltage Tolerant I/O's at  $V_{CC}$  from 2.3 V to 3.6 V
- Power-Off High-Impedance Inputs and Outputs
- Low Static Power Consumption
  - ◆  $I_{CC} = 0.9$   $\mu$ A Maximum
- Low Dynamic Power Consumption
  - ◆  $C_{PD} = 2.7$  pF Typical at 3.3 V
- Ultra-Small MicroPak™ Packages

### Logic Diagram

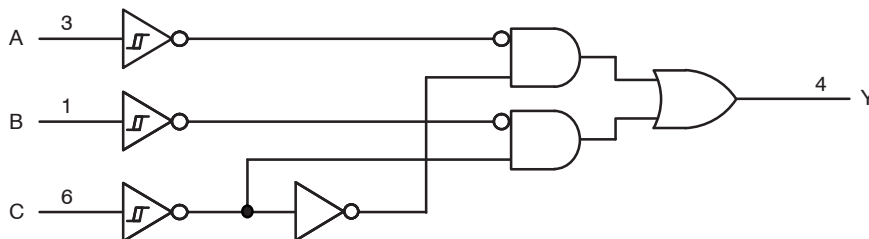


Figure 1. Logic Diagram (Positive Logic)

### ORDERING INFORMATION

Device	Package	Shipping†
74AUP1T97FHX	UDFN-6 (Pb-Free/Halide Free)	5000 / Tape & Reel
74AUP1T97L6X	SIP-6 (Pb-Free/Halide Free)	5000 / Tape & Reel

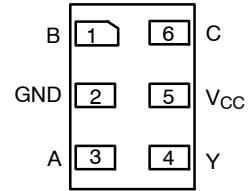
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# 74AUP1T97

## PIN CONFIGURATIONS

**Table 1. PIN DESCRIPTIONS**

Pin	Name	Description
1	B	Data Input
2	GND	Ground
3	A	Data Input
4	Y	Output
5	V <sub>CC</sub>	Supply Voltage
6	C	Data Input



**Figure 2. MicroPak™ (Top View)**

**Table 2. FUNCTION TABLE**

Inputs			Output
C	B	A	Y
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

1. H = HIGH Logic Level
2. L = LOW Logic Level

**Table 3. FUNCTION SELECTION TABLE**

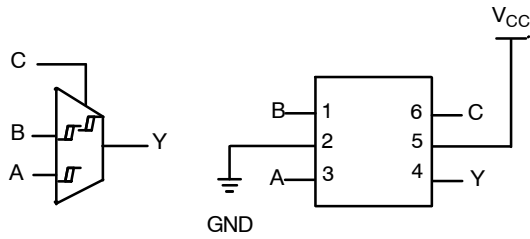
Logic Function	Connection Configuration
2-to-1 MUX	Figure 3
2-Input AND Gate	Figure 4
2-Input OR Gate with One Inverted Input	Figure 5
2-Input NAND Gate with One Inverted Input	Figure 5
2-Input AND Gate with One Inverted Input	Figure 6
2-Input NOR Gate with One Inverted Input	Figure 6
2-Input OR Gate	Figure 7
Inverter	Figure 8
Buffer	Figure 9

# 74AUP1T97

## Logic Configurations

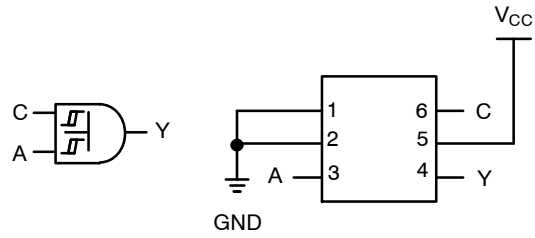
Figure 3 through Figure 9 show the logical functions that can be implemented using the 74AUP1T97. The diagrams show the DeMorgan's equivalent logic duals for a given

two-input function. The logical implementation is next to the board-level physical implementation of how the pins of the function should be connected.

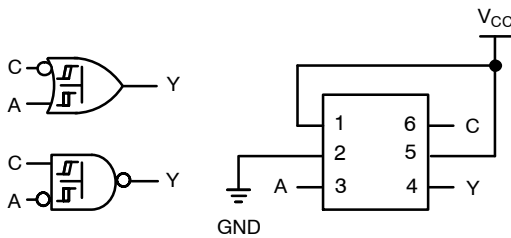


**Note:**  
 1. When C is L, Y = B.  
 2. When C is H, Y = A.

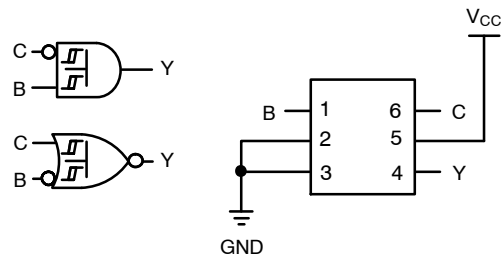
**Figure 3. 2-to-1 MUX**



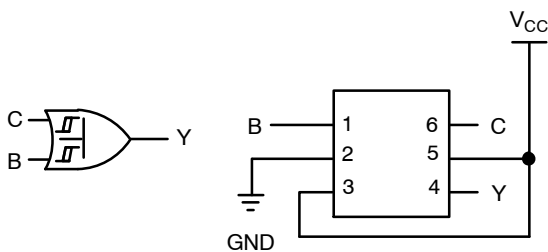
**Figure 4. 2-Input AND Gate**



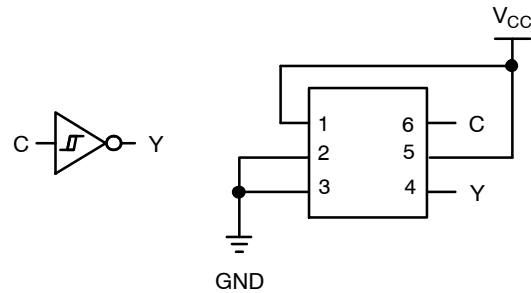
**Figure 5. Input OR Gate with One Inverted Input  
 2-Input NAND Gate with One Inverted Input**



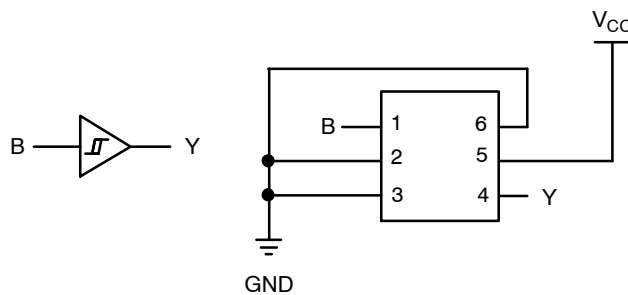
**Figure 6. 2-Input AND Gate with One Inverted Input  
 2-Input NOR Gate with One Inverted Input**



**Figure 7. 2-Input OR Gate**



**Figure 8. Inverter**



**Figure 9. Buffer**

# 74AUP1T97

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Unit
$V_{CC}$	Supply Voltage	-0.5	4.6	V
$V_{IN}$	DC Input Voltage	-0.5	4.6	V
$V_{OUT}$	DC Output Voltage HIGH or LOW State(Note 3) $V_{CC} = 0\text{ V}$	-0.5 -0.5	$V_{CC} + 0.5$ 4.6	V
$I_{IK}$	DC Input Diode Current $V_{IN} < 0\text{ V}$	-	-50	mA
$I_{OK}$	DC Output Diode Current $V_{OUT} < 0\text{ V}$ $V_{OUT} > V_{CC}$	-	-50 +50	mA
$I_{OH} / I_{OL}$	DC Output Source / Sink Current	-	$\pm 50$	mA
$I_O$	Continuous Output Current	-	$\pm 20$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current per Supply Pin	-	$\pm 50$	mA
$T_{STG}$	Storage Temperature Range	-65	+150	$^{\circ}\text{C}$
$T_J$	Junction Temperature Under Bias	-	+150	$^{\circ}\text{C}$
$T_L$	Junction Lead Temperature, Soldering 10s	-	+260	$^{\circ}\text{C}$
$P_D$	Power Dissipation at +85 $^{\circ}\text{C}$ MicroPak-6 MicroPak2-6	-	130 120	mW
ESD	Human Body Model, JEDEC:JESD22-A114 Charged Device Model, JEDEC:JESD22-C101	-	5000+ 2000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3.  $I_O$  absolute maximum rating must be observed.

**Table 4. RECOMMENDED OPERATING CONDITIONS** (Note 4)

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	Supply Voltage		2.3	3.6	V
$V_{IN}$	Input Voltage		0	3.6	V
$V_{OUT}$	Output Voltage	$V_{CC} = 0\text{ V}$ HIGH or LOW State	0 0	3.6 $V_{CC}$	V
$I_{OH} / I_{OL}$	Output Current	$V_{CC} = 3.0\text{ V to } 3.6\text{ V}$ $V_{CC} = 2.3\text{ V to } 2.7\text{ V}$	-	$\pm 4.0$ $\pm 3.1$	mA
$T_A$	Operating Free-Air Temperature		-40	+85	$^{\circ}\text{C}$
$\theta_{JA}$	Thermal Resistance	MicroPak-6 MicroPak2-6	-	500 560	$^{\circ}\text{C/W}$

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must be held HIGH or LOW. They may not float.

# 74AUP1T97

**Table 5. DC ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C		Unit
				Min	Max	Min	Max	
V <sub>P</sub>	Positive Threshold Voltage	-	2.3 V to 2.7 V	0.60	1.10	0.60	1.10	V
			3.0 V to 3.6 V	0.75	1.16	0.75	1.19	V
V <sub>N</sub>	Negative Threshold Voltage	-	2.3 V to 2.7 V	0.35	0.60	0.35	0.60	V
			3.0 V to 3.6 V	0.50	0.85	0.50	0.85	V
V <sub>H</sub>	Hysteresis Voltage	-	2.3 V to 2.7 V	0.23	0.60	0.10	0.60	V
			3.0 V to 3.6 V	0.25	0.56	0.15	0.56	V
V <sub>OH</sub>	HIGH Level Output Voltage	I <sub>OH</sub> = -20 μA	2.3 V ≤ V <sub>CC</sub> ≤ 3.6 V	V <sub>CC</sub> - 0.1	-	V <sub>CC</sub> - 0.1	-	V
		I <sub>OH</sub> = -2.3 mA	2.3 V	2.05	-	1.97	-	V
		I <sub>OH</sub> = -3.1 mA		1.90	-	1.85	-	V
		I <sub>OH</sub> = -2.7 mA	3.0 V	2.72	-	2.67	-	V
		I <sub>OH</sub> = -4 mA		2.60	-	2.55	-	V
V <sub>OL</sub>	LOW Level Output Voltage	I <sub>OL</sub> = 20 μA	2.3 V ≤ V <sub>CC</sub> ≤ 3.6 V	-	0.10	-	0.10	V
		I <sub>OL</sub> = 2.3 mA	2.3 V	-	0.31	-	0.33	V
		I <sub>OH</sub> = 3.1 mA		-	0.44	-	0.45	V
		I <sub>OL</sub> = 2.7 mA	3.0 V	-	0.31	-	0.33	V
		I <sub>OL</sub> = 4.0 mA		-	0.44	-	0.45	V
I <sub>IN</sub>	Input Leakage Current	0 ≤ V <sub>IN</sub> ≤ 3.6	0 V to 3.6 V	-	±0.10	-	±0.50	μA
I <sub>OFF</sub>	Power Off Leakage Current	0 ≤ (V <sub>IN</sub> , V <sub>O</sub> ) ≤ 3.6	0 V	-	0.10	-	0.50	μA
ΔI <sub>OFF</sub>	Additional Power Off Leakage Current	V <sub>IN</sub> or V <sub>O</sub> = 0 V to 3.6 V	0 V to 0.2 V	-	0.20	-	0.60	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	2.3 V to 3.6 V	-	0.50	-	0.90	μA
		V <sub>CC</sub> ≤ V <sub>IN</sub> ≤ 3.6 V		-	-	-	±0.90	μA
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	One Input at 0.3 V or 1.1 V, other Inputs at 0 or V <sub>CC</sub>	2.3 V to 2.7 V	-	-	-	4	μA
		One Input at 0.45 V or 1.2 V, other Inputs at 0 or V <sub>CC</sub>	3.0 V to 3.6 V	-	-	-	12	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# 74AUP1T97

**Table 6. AC ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40 to +85°C		Unit	Figure
				Min	Typ	Max	Typ	Max		
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay	C <sub>L</sub> = 5 pF, R <sub>L</sub> = 1 MΩ	2.30 V ≤ V <sub>CC</sub> ≤ 2.70 V, V <sub>IN</sub> = 1.65 V to 1.95 V	1.1	3.7	5.5	1.1	6.8	ns	Figure 10 & 11
			2.30 V ≤ V <sub>CC</sub> ≤ 2.70 V, V <sub>IN</sub> = 2.30 V to 2.70 V	1.1	3.8	6.5	1.1	7.0		
			2.30 V ≤ V <sub>CC</sub> ≤ 2.70 V, V <sub>IN</sub> = 3.0 V to 3.60 V	1.1	3.9	6.0	1.1	6.5		
			3.00 V ≤ V <sub>CC</sub> ≤ 3.60 V, V <sub>IN</sub> = 1.65 V to 1.95 V	1.0	3.3	4.9	1.0	8.0		
			3.00 V ≤ V <sub>CC</sub> ≤ 3.60 V, V <sub>IN</sub> = 2.30 V to 2.70 V	1.0	3.2	4.6	1.0	5.8		
			3.00 V ≤ V <sub>CC</sub> ≤ 3.60 V, V <sub>IN</sub> = 3.00 V to 3.60 V	1.0	3.1	4.7	1.0	5.5		
		C <sub>L</sub> = 10 pF, R <sub>L</sub> = 1 MΩ	2.30 V ≤ V <sub>CC</sub> ≤ 2.70 V, V <sub>IN</sub> = 1.65 V to 1.95 V	1.3	4.1	6.5	1.0	7.9		
			2.30 V ≤ V <sub>CC</sub> ≤ 2.70 V, V <sub>IN</sub> = 2.30 V to 2.70 V	1.3	4.0	6.2	1.0	7.1		
			2.30 V ≤ V <sub>CC</sub> ≤ 2.70 V, V <sub>IN</sub> = 3.0 V to 3.60 V	1.3	3.7	5.7	1.0	6.5		
			3.00 V ≤ V <sub>CC</sub> ≤ 3.60 V, V <sub>IN</sub> = 1.65 V to 1.95 V	1.3	3.5	5.6	1.0	8.5		
			3.00 V ≤ V <sub>CC</sub> ≤ 3.60 V, V <sub>IN</sub> = 2.30 V to 2.70 V	1.3	3.4	5.3	1.0	6.1		
			3.00 V ≤ V <sub>CC</sub> ≤ 3.60 V, V <sub>IN</sub> = 3.00 V to 3.60 V	1.3	3.3	5.2	1.0	5.9		
		C <sub>L</sub> = 15 pF, R <sub>L</sub> = 1 MΩ	2.30 V ≤ V <sub>CC</sub> ≤ 2.70 V, V <sub>IN</sub> = 1.65 V to 1.95 V	1.5	4.6	6.9	1.0	8.7		
			2.30 V ≤ V <sub>CC</sub> ≤ 2.70 V, V <sub>IN</sub> = 2.30 V to 2.70 V	1.5	4.4	6.8	1.0	7.9		
			2.30 V ≤ V <sub>CC</sub> ≤ 2.70 V, V <sub>IN</sub> = 3.0 V to 3.60 V	1.5	4.2	6.3	1.0	7.4		
			3.00 V ≤ V <sub>CC</sub> ≤ 3.60 V, V <sub>IN</sub> = 1.65 V to 1.95 V	1.3	3.9	6.2	1.0	9.1		
			3.00 V ≤ V <sub>CC</sub> ≤ 3.60 V, V <sub>IN</sub> = 2.30 V to 2.70 V	1.3	3.8	5.6	1.0	6.8		
			3.00 V ≤ V <sub>CC</sub> ≤ 3.60 V, V <sub>IN</sub> = 3.00 V to 3.60 V	1.3	3.8	5.6	1.0	6.2		
		C <sub>L</sub> = 30 pF, R <sub>L</sub> = 1 MΩ	2.30 V ≤ V <sub>CC</sub> ≤ 2.70 V, V <sub>IN</sub> = 1.65 V to 1.95 V	1.3	4.2	7.9	1.3	8.5		
			2.30 V ≤ V <sub>CC</sub> ≤ 2.70 V, V <sub>IN</sub> = 2.30 V to 2.70 V	1.3	3.9	7.9	1.3	8.5		
			2.30 V ≤ V <sub>CC</sub> ≤ 2.70 V, V <sub>IN</sub> = 3.0 V to 3.60 V	1.0	3.7	7.3	1.0	8.9		
			3.00 V ≤ V <sub>CC</sub> ≤ 3.60 V, V <sub>IN</sub> = 1.65 V to 1.95 V	1.3	3.5	6.1	1.3	7.9		
			3.00 V ≤ V <sub>CC</sub> ≤ 3.60 V, V <sub>IN</sub> = 2.30 V to 2.70 V	1.1	3.0	5.9	1.1	6.8		
			3.00 V ≤ V <sub>CC</sub> ≤ 3.60 V, V <sub>IN</sub> = 2.30 V to 2.70 V	1.0	2.7	5.7	1.0	6.5		
C <sub>IN</sub>	Input Capacitance	-	0	-	2.1	-	-	-	pF	-
C <sub>OUT</sub>	Output Capacitance	-	0	-	3.0	-	-	-		
C <sub>PD</sub>	Power Dissipation Capacitance	-	2.30 V ≤ V <sub>CC</sub> ≤ 2.70 V	-	2.0	-	-	-		
			3.00 V ≤ V <sub>CC</sub> ≤ 3.60 V	-	2.7	-	-	-		

# 74AUP1T97

## AC LOADINGS AND WAVEFORMS

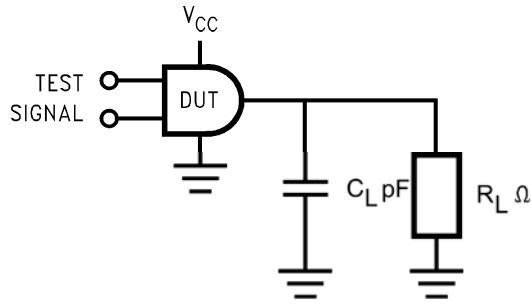


Figure 10. AC Test Circuit

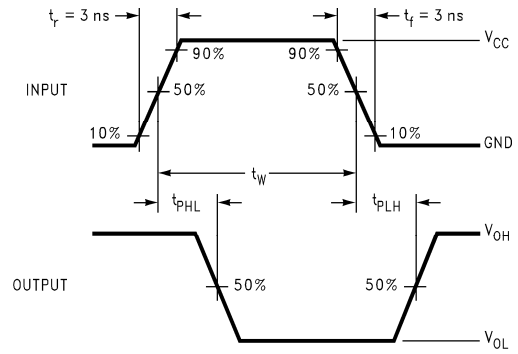


Figure 11. AC Waveforms

Symbol	V <sub>CC</sub>	
	3.3 V ±0.3 V	2.5 V ±0.2 V
V <sub>mi</sub>	V <sub>IN</sub> / 2	V <sub>IN</sub> / 2
V <sub>mo</sub>	V <sub>CC</sub> / 2	V <sub>CC</sub> / 2

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



SIP6 1.45X1.0  
CASE 127EB  
ISSUE O

DATE 31 AUG 2016



NOTES:

1. CONFORMS TO JEDEC STANDARD MO-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-2009
4. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

<b>DOCUMENT NUMBER:</b>	<b>98AON13590G</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SIP6 1.45X1.0</b>	<b>PAGE 1 OF 1</b>

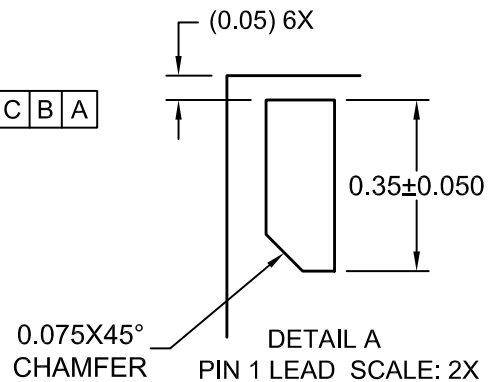
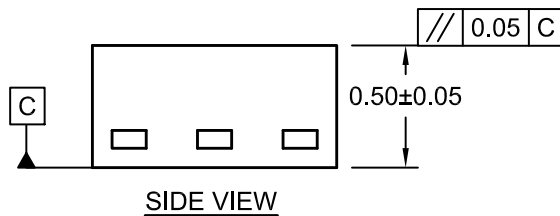
ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.





**UDFN6 1.0X1.0, 0.35P**  
CASE 517DP  
ISSUE O

DATE 31 AUG 2016



- NOTES:  
A. COMPLIES TO JEDEC MO-252 STANDARD  
B. DIMENSIONS ARE IN MILLIMETERS.  
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009

<b>DOCUMENT NUMBER:</b>	<b>98AON13593G</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>UDFN6 1.0X1.0, 0.35P</b>	<b>PAGE 1 OF 1</b>

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)