



HEF4073B

Triple 3-input AND gate

Rev. 5 — 20 October 2023

Product data sheet

1. General description

The HEF4073B is a triple 3-input AND gate. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Wide supply voltage range from 3.0 to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Complies with JEDEC standard JESD 13-B
- ESD protection:
 - HBM ANSI/ESDA/JEDEC JS-001 exceeds 2000 V
 - MM EIA/JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
HEF4073BT	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

4. Functional diagram

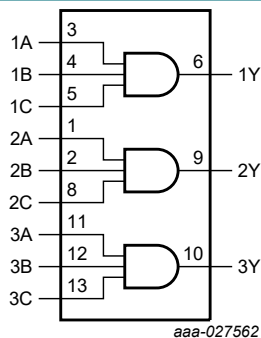


Fig. 1. Functional diagram

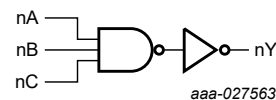
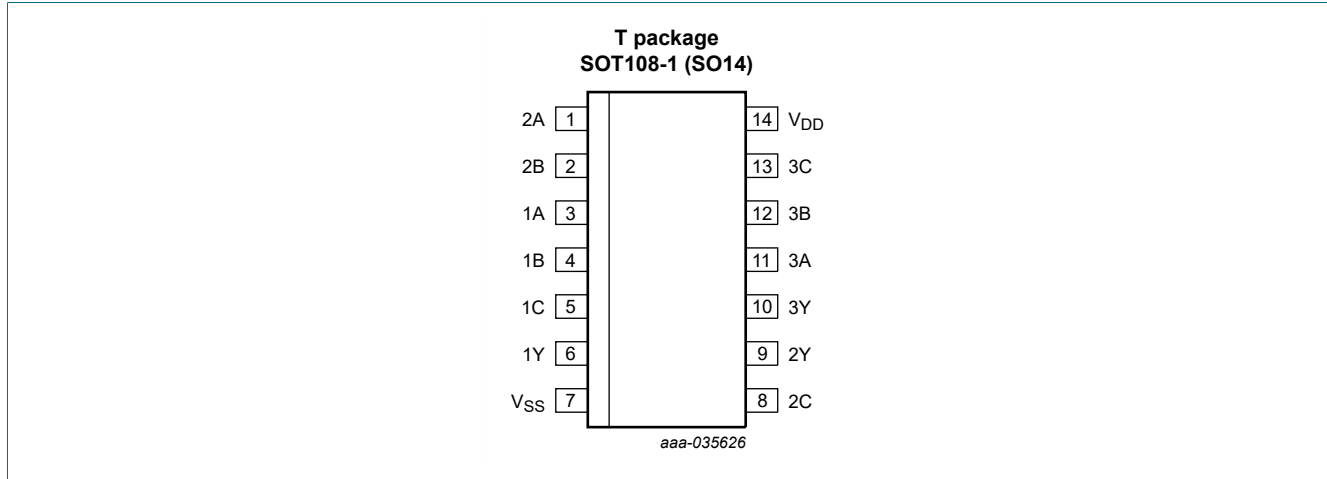


Fig. 2. Logic diagram (one gate)

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A	3, 1, 11	data input
1B, 2B, 3B	4, 2, 12	data input
1C, 2C, 3C	5, 8, 13	data input
1Y, 2Y, 3Y	6, 9, 10	data output
V _{SS}	7	ground (0 V)
V _{DD}	14	supply voltage

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; X = don't care

Input				Output
nA	nB	nC	nY	nY
L	X	X	L	L
X	L	X	L	L
X	X	L	L	L
H	H	H	H	H

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to $V_{SS} = 0\text{ V}$ (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{DD} + 0.5\text{ V}$	-	± 10	mA
V_I	input voltage		-0.5	$V_{DD} + 0.5$	V
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{DD} + 0.5\text{ V}$	-	± 10	mA
$I_{I/O}$	input/output current		-	± 10	mA
I_{DD}	supply current		-	50	mA
T_{stg}	storage temperature		-65	+150	°C
T_{amb}	ambient temperature		-40	+85	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+85\text{ °C}$	-	500	mW
P	power dissipation	per output	-	100	mW

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		3	15	V
V_I	input voltage		0	V_{DD}	V
T_{amb}	ambient temperature	in free air	-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	3.75	ns/V
		$V_{DD} = 10\text{ V}$	-	0.5	ns/V
		$V_{DD} = 15\text{ V}$	-	0.08	ns/V

9. Static characteristics

Table 6. Static characteristics

$V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD} ; unless otherwise specified.

Symbol	Parameter	Conditions	V _{DD}	T _{amb} = -40 °C		T _{amb} = +25 °C		T _{amb} = +85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level input voltage	I _O < 1 μA	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V _{IL}	LOW-level input voltage	I _O < 1 μA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V _{OH}	HIGH-level output voltage	I _O < 1 μA	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V _{OL}	LOW-level output voltage	I _O < 1 μA	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I _{OH}	HIGH-level output current	V _O = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		V _O = 4.6 V	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		V _O = 9.5 V	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		V _O = 13.5 V	15 V	-	-3.6	-	-3.0	-	-2.4	mA
I _{OL}	LOW-level output current	V _O = 0.4 V	5 V	0.52	-	0.44	-	0.36	-	mA
		V _O = 0.5 V	10 V	1.3	-	1.1	-	0.9	-	mA
		V _O = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mA
I _I	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	μA
I _{DD}	supply current	all valid input combinations; I _O = 0 A	5 V	-	1.0	-	1.0	-	7.5	μA
			10 V	-	2.0	-	2.0	-	15.0	μA
			15 V	-	4.0	-	4.0	-	30.0	μA
C _I	input capacitance			-	-	-	7.5	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; for test circuit see Fig. 4.

Symbol	Parameter	Conditions	Extrapolation formula[1]	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	nA, nB, nC to nY; see Fig. 3					
		$V_{DD} = 5\text{ V}$	$23 + 0.55 \times C_L$	-	55	110	ns
		$V_{DD} = 10\text{ V}$	$14 + 0.23 \times C_L$	-	25	50	ns
		$V_{DD} = 15\text{ V}$	$12 + 0.16 \times C_L$	-	20	40	ns
t_{PLH}	LOW to HIGH propagation delay	nA, nB, nC to nY; see Fig. 3					
		$V_{DD} = 5\text{ V}$	$13 + 0.55 \times C_L$	-	45	90	ns
		$V_{DD} = 10\text{ V}$	$9 + 0.23 \times C_L$	-	20	40	ns
		$V_{DD} = 15\text{ V}$	$7 + 0.16 \times C_L$	-	15	30	ns
t_t	output transition time	nY; see Fig. 3 [2]	$10 + 1.0 \times C_L$	-	60	120	ns
			$9 + 0.42 \times C_L$	-	30	60	ns
			$6 + 0.28 \times C_L$	-	20	40	ns

[1] The typical value of the propagation delay and output transition time can be calculated with the extrapolation formula (C_L in pF).

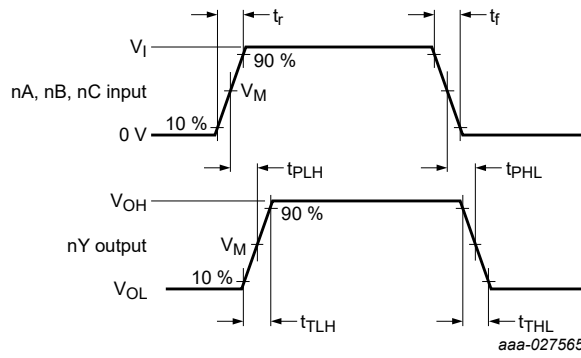
[2] t_t is the same as t_{THL} and t_{TLH} .

Table 8. Dynamic power dissipation

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$.

Symbol	Parameter	V_{DD}	Typical formula	where:
P_D	dynamic power dissipation	5 V	$P_D = 600 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ (μW)	f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF; $\Sigma(f_o \times C_L)$ = sum of the outputs; V_{DD} = supply voltage in V.
		10 V	$P_D = 2700 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ (μW)	
		15 V	$P_D = 8400 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ (μW)	

10.1. Waveforms and test circuit



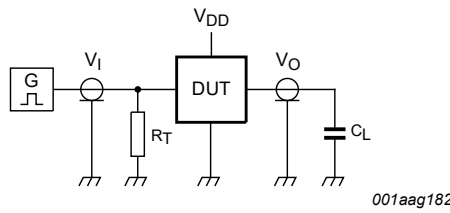
Measurement points are given in [Table 9](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 3. Input to output propagation delay and output transition times

Table 9. Measurement points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5 V to 15 V	$0.5 \times V_{DD}$	$0.5 \times V_{DD}$



Test data is given in [Table 10](#).

Definitions for test circuit:

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig. 4. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input	Load
V_{DD}	V_I	C_L
5 V to 15 V	V_{SS} or V_{DD}	≤ 20 ns
		50 pF

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



Fig. 5. Package outline SOT108-1 (SO14)

12. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
HBM	Human Body Model
MM	Machine Model

13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4073B v.5	20231020	Product data sheet	-	HEF4073B v.4
Modifications:	<ul style="list-style-type: none"> • Section 1 and Section 2 updated. • Section 7: Derating value for P_{tot} total power dissipation removed. 			
HEF4073B v.4	20171006	Product data sheet	-	HEF4073B_CNV v.3
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type numbers HEF4073BP and HEF4073BD removed. 			
HEF4073B_CNV v.3	19950101	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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