Analog Multiplexers/ Demultiplexers with Injection Current Effect Control with LSTTL Compatible Inputs

Automotive Customized

ON Semiconductor®

www.onsemi.com

MC74HCT4851A, MC74HCT4852A

This device is pin compatible to standard HC405x and MC1405xB analog mux/demux devices, but feature injection current effect control. This makes them especially suited for usage in automotive applications where voltages in excess of normal logic voltage are common.

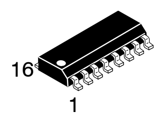
The injection current effect control allows signals at disabled analog input channels to exceed the supply voltage range without affecting the signal of the enabled analog channel. This eliminates the need for external diode/ resistor networks typically used to keep the analog channel signals within the supply voltage range.

The devices utilize low power silicon gate CMOS technology. The Channel Select and Enable inputs are compatible with standard CMOS or LSTTL outputs.

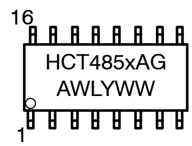
Features

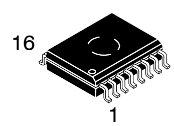
- Injection Current Cross−Coupling Less than 1mV/mA (See Figure 6)
- Pin Compatible to HC405x and MC1405xB Devices
- Power Supply Range (V_{CC} − GND) = 4.5 to 5.5 V
- In Compliance With the Requirements of JEDEC Standard No. 7 A
- Chip Complexity: 154 FETs or 36 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

MARKING DIAGRAMS

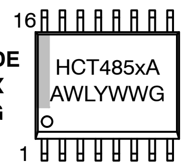


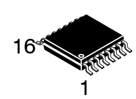
SOIC−16 D SUFFIX CASE 751B



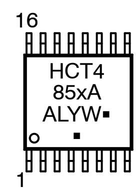


SOIC−16 WIDE DW SUFFIX CASE 751G





TSSOP−16 DT SUFFIX CASE 948F



X	= 1 or 2
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

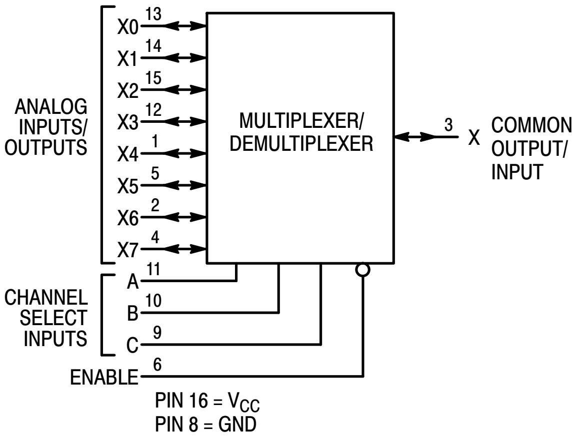


Figure 1. MC74HCT4851A Logic Diagram Single−Pole, 8−Position Plus Common Off

FUNCTION TABLE − MC74HCT4851A

Control Inputs				
	Select			
Enable	**C**	**B**	**A**	**ON Channels**
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	NONE

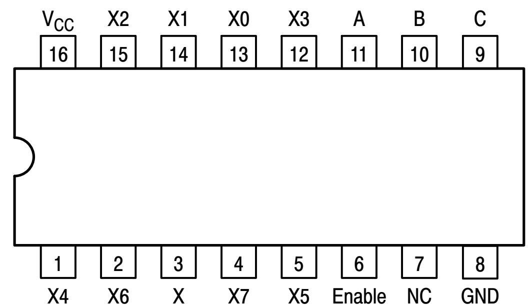


Figure 2. MC74HCT4851A 16−Lead Pinout (Top View)

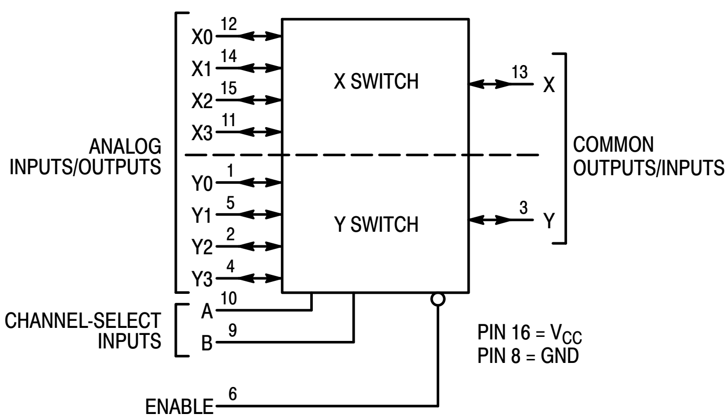


Figure 3. MC74HCT4852A Logic Diagram Double−Pole, 4−Position Plus Common Off

FUNCTION TABLE − MC74HCT4852A

Control Inputs				
	Select			
Enable	**B**	**A**	**ON Channels**	
L	L	L	Y0	X0
L	L	H	Y1	X1
L	H	L	Y2	X2
L	H	H	Y3	X3
H	X	X	NONE	

X = Don't Care

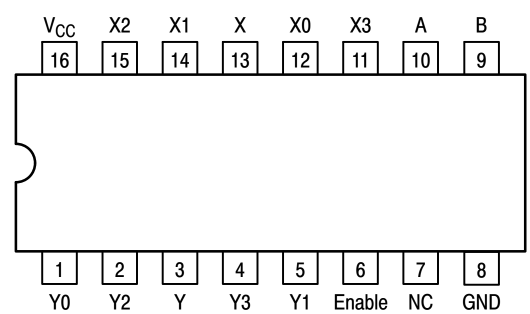


Figure 4. MC74HCT4852A 16−Lead Pinout (Top View)

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	–0.5 to + 7.0	V
V_{in}	DC Input Voltage (Any Pin) (Referenced to GND)	–0.5 to V_{CC} + 0.5	V
I	DC Current, Into or Out of Any Pin	± 25	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature Range	–65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds SOIC or TSSOP Package	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}	DC Input Voltage (Any Pin) (Referenced to GND)	GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch	0.0	1.2	V
T_A	Operating Temperature Range, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise/Fall Time V_{CC} = 2.0 V (Channel Select or Enable Inputs) V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

*For voltage drops across switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC CHARACTERISTICS — Digital Section (Voltages Referenced to GND) V_{EE} = GND, Except Where Noted

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit –55 to 25°C	≤85°C	≤125°C	Unit
V_{IH}	Minimum High–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	4.5 to 5.5	2.0	2.0	2.0	V
V_{IL}	Maximum Low–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	4.5 to 5.5	0.8	0.8	0.8	V
I_{in}	Maximum Input Leakage Current on Digital Pins (Enable/A/B/C)	V_{in} = V_{CC} or GND	5.5	± 0.1	± 1.0	± 1.0	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in(digital)}$ = V_{CC} or GND $V_{in(analog)}$ = GND	5.5	2.0	20	40	µA

DC CHARACTERISTICS — Analog Section

Symbol	Parameter	Condition	V_{CC}	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
R_{on}	Maximum “ON” Resistance	$V_{in} = V_{IL}$ or V_{IH}; $V_{IS} = V_{CC}$ to GND (Note 1); $I_S \leq 2.0$ mA (Note 2)	4.5 5.5	550 400	650 500	750 600	Ω
ΔR_{on}	Delta “ON” Resistance	$V_{in} = V_{IL}$ or V_{IH}; $V_{IS} = V_{CC}/2$ (Note 1); $I_S \leq 2.0$ mA (Note 2)	4.5 5.5	80 60	100 80	120 100	Ω
I_{off}	Maximum Off–Channel Leakage Current, Any One Channel Common Channel	$V_{in} = V_{CC}$ or GND	5.5	±0.1 ±0.1	±0.1 ±0.1	±0.1 ±0.1	μA
I_{on}	Maximum On–Channel Leakage Channel–to–Channel	$V_{in} = V_{CC}$ or GND	5.5	±0.1	±0.1	±0.1	μA

1. V_{IS} is the input voltage of an analog I/O pin.
2. I_S is the currebnt flowing in or out of analog I/O pin.

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns, V_{CC} = 5.0 V ± 10%)

Symbol	Parameter	V_{CC}	–55 to 25°C	≤85°C	≤125°C	Unit
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Analog Input to Analog Output	5.0	40	45	50	ns
t_{PHL}, $t_{PHZ,PZH}$ t_{PLH}, $t_{PLZ,PZL}$	Maximum Propagation Delay, Enable or Channel–Select to Analog Output	5.0	80	90	100	ns
C_{in}	Maximum Input Capacitance — Digital Pins (All Switches Off) — Any Single Analog Pin (All Switches Off) — Common Analog Pin		10 35 40	10 35 40	10 35 40	pF
C_{PD}	Power Dissipation Capacitance — Typical	5.0	20			pF

INJECTION CURRENT COUPLING SPECIFICATIONS (V_{CC} = 5V, T_A = –55°C to +125°C)

Symbol	Parameter	Condition	Typ	Max	Unit
$V\Delta_{out}$	Maximum Shift of Output Voltage of Enabled Analog Channel	$I_{in}^* \leq 1$ mA, $R_S \leq 3{,}9$ kΩ $I_{in}^* \leq 10$ mA, $R_S \leq 3{,}9$ kΩ $I_{in}^* \leq 1$ mA, $R_S \leq 20$ kΩ $I_{in}^* \leq 10$ mA, $R_S \leq 20$ kΩ	0.1 1.0 0.5 5.0	1.0 5.0 2.0 20	mV

* I_{in} = Total current injected into all disabled channels.

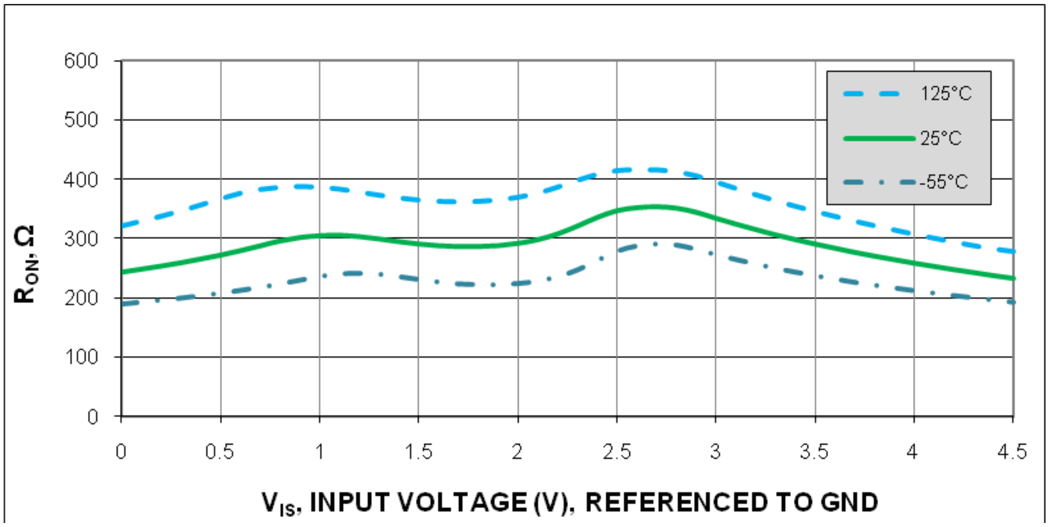


Figure 5. Typical On Resistance V_{CC} = 4.5V

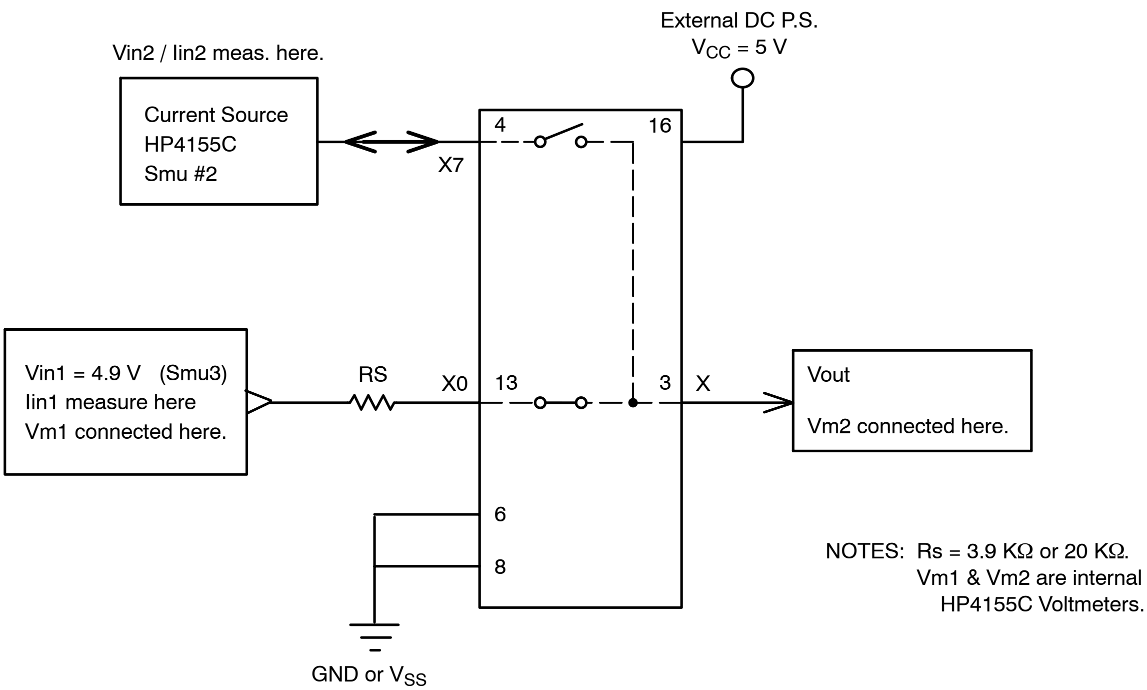


Figure 6. Injection Current Coupling Specification

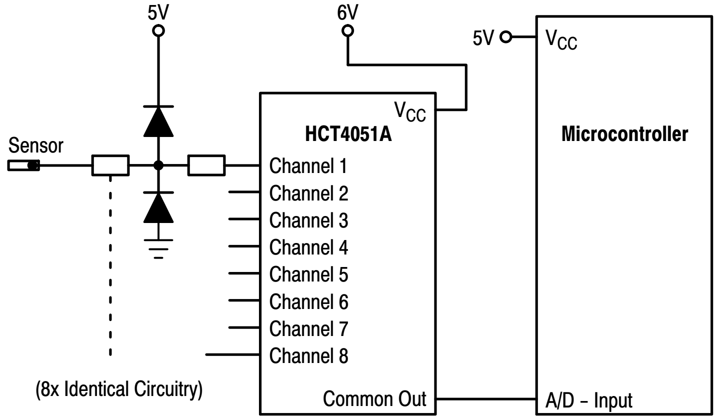


Figure 7. Actual Technology
Requires 32 passive components and one extra 6V regulator
to suppress injection current into a standard HCT4051 multiplexer

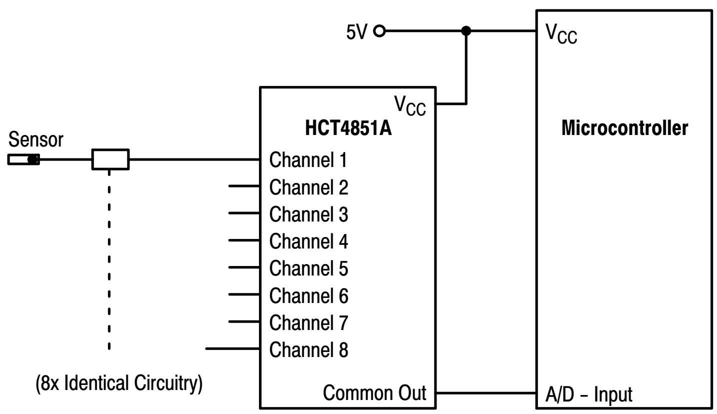


Figure 8. MC74HCT4851A Solution
Solution by applying the HCT4851A multiplexer

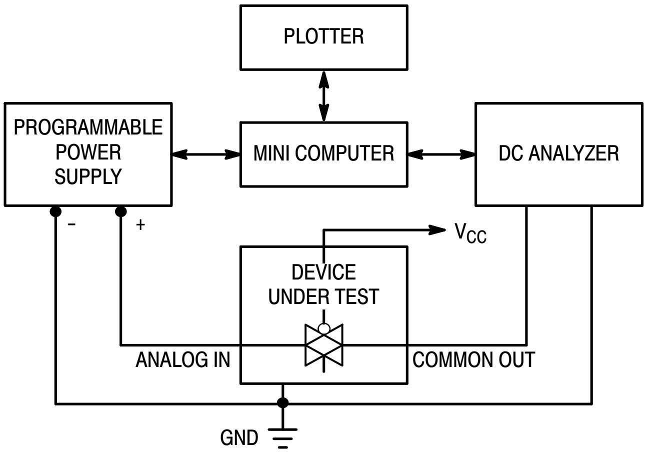


Figure 9. On Resistance Test Set−Up

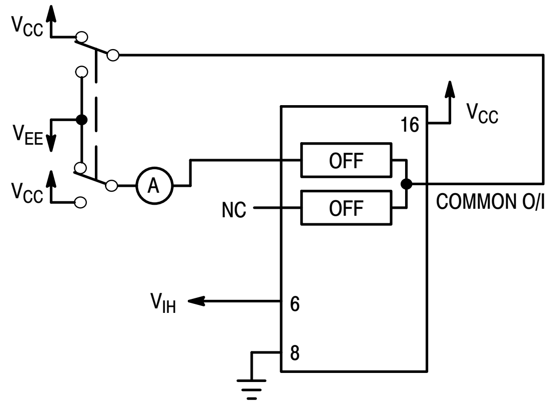


Figure 10. Maximum Off Channel Leakage Current, Any One Channel, Test Set−Up

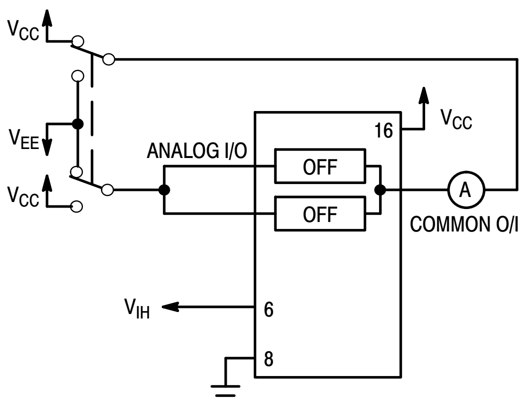


Figure 11. Maximum Off Channel Leakage Current, Common Channel, Test Set−Up

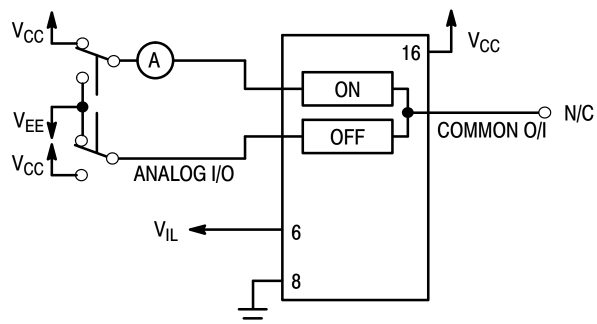


Figure 12. Maximum On Channel Leakage Current, Channel to Channel, Test Set−Up

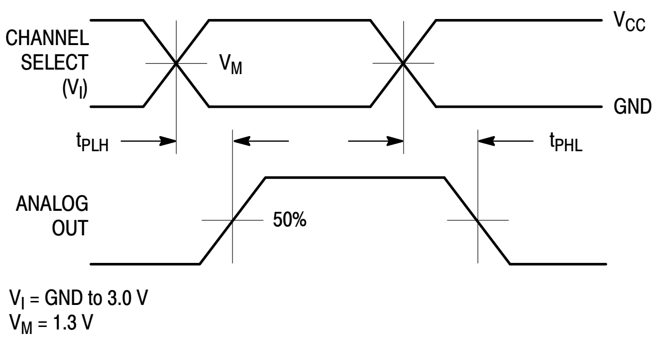
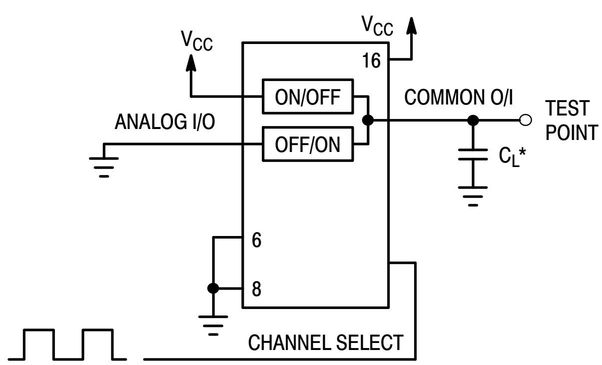


Figure 13. Propagation Delays, Channel Select to Analog Out



*Includes all probe and jig capacitance

Figure 14. Propagation Delay, Test Set−Up Channel Select to Analog Out

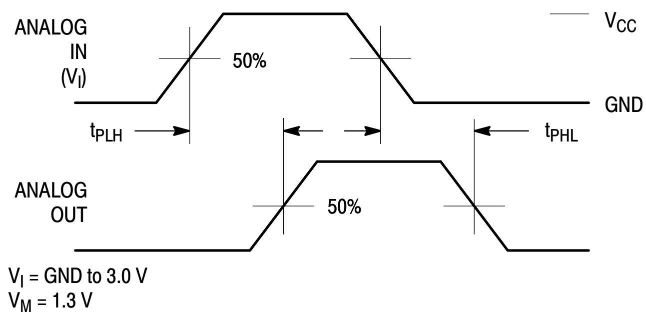


Figure 15. Propagation Delays, Analog In to Analog Out

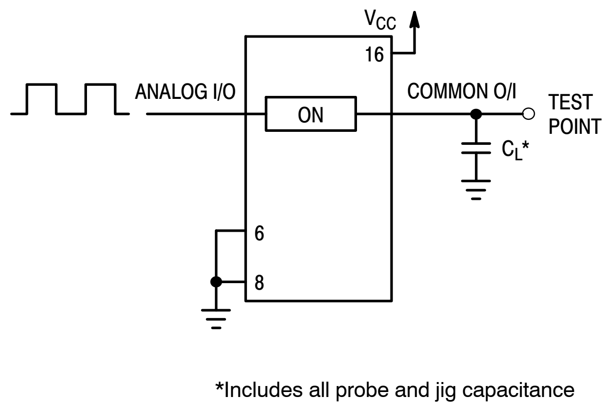


Figure 16. Propagation Delay, Test Set−Up Analog In to Analog Out

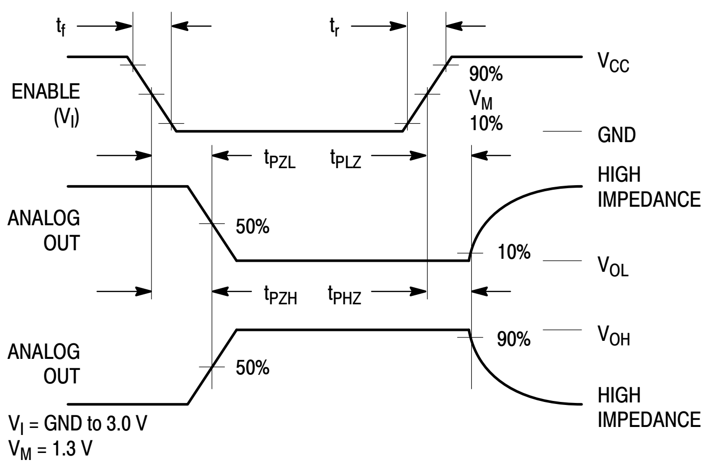


Figure 17. Propagation Delays, Enable to Analog Out

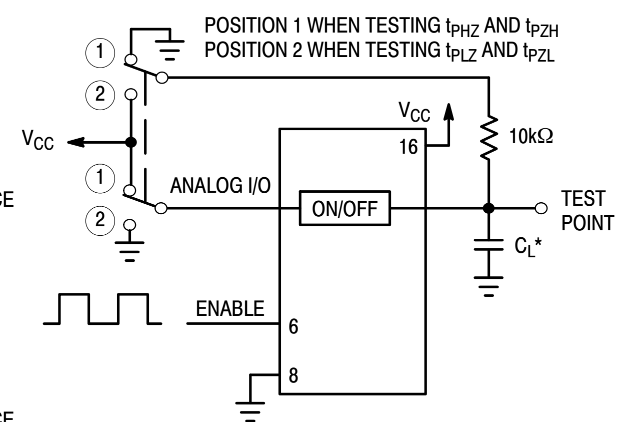


Figure 18. Propagation Delay, Test Set−Up Enable to Analog Out

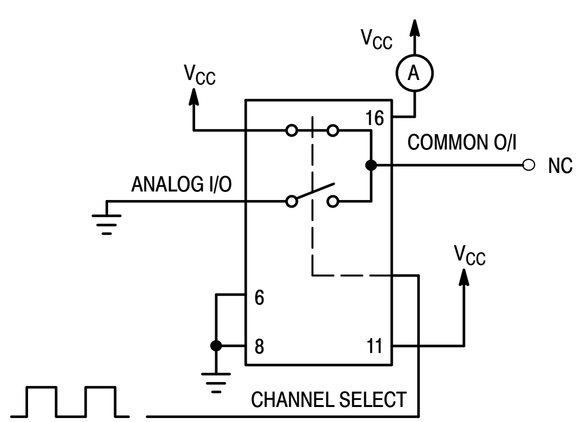


Figure 19. Power Dissipation Capacitance, Test Set−Up

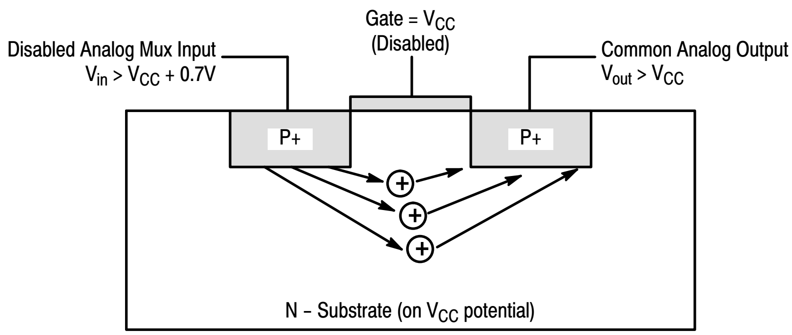


Figure 20. Diagram of Bipolar Coupling Mechanism
Appears if V_{in} exceeds V_{CC}, driving injection current into the substrate

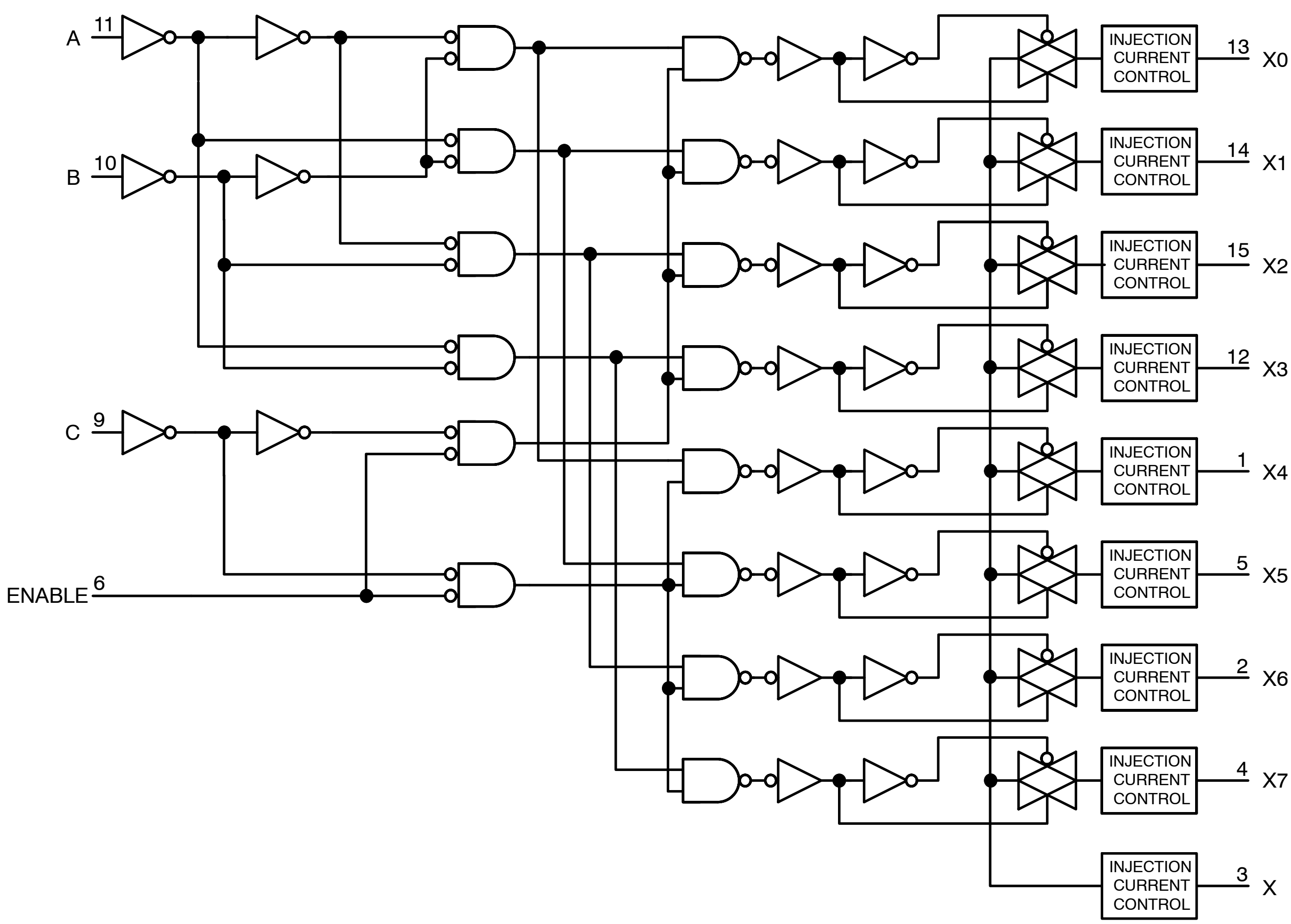


Figure 21. Function Diagram, HCT4851A

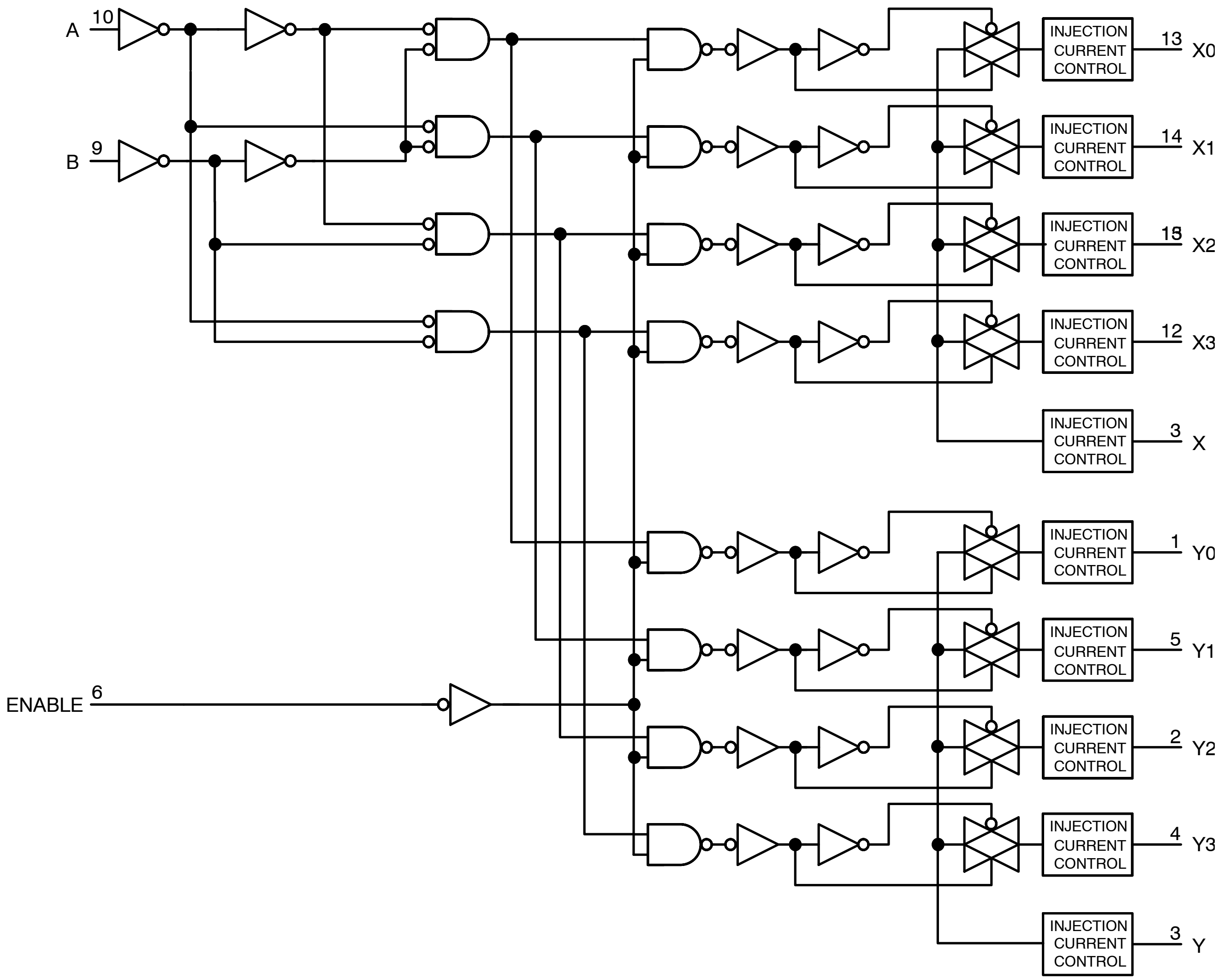


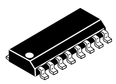
Figure 22. Function Diagram, HCT4852A

ORDERING INFORMATION

Device	Package	Shipping†
MC74HCT4851ADG	SOIC−16 (Pb−Free)	48 Units / Rail
MC74HCT4851ADR2G		2500 Units / Tape & Reel
NLV74HCT4851ADRG*		2500 Units / Tape & Reel
MC74HCT4851AADR2G		2500 Units / Tape & Reel
NLV74HCT4851AADR2G* (Contact ON Semiconductor)		2500 Units / Tape & Reel
MC74HCT4851ADTG	TSSOP−16 (Pb−Free)	48 Units / Rail
M74HCT4851ADTR2G		2500 Units / Tape & Reel
NLVHCT4851ADTR2G*		2500 Units / Tape & Reel
M74HCT4851ADWR2G	SOIC−16 WIDE (Pb−Free)	1000 Units / Tape & Reel
MC74HCT4852ADG	SOIC−16 (Pb−Free)	48 Units / Rail
MC74HCT4852ADR2G		2500 Units / Tape & Reel
MC74HCT4852ADTG	TSSOP−16 (Pb−Free)	48 Units / Rail
M74HCT4852ADTR2G		2500 Units / Tape & Reel
NLVHCT4852ADTR2G*		2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

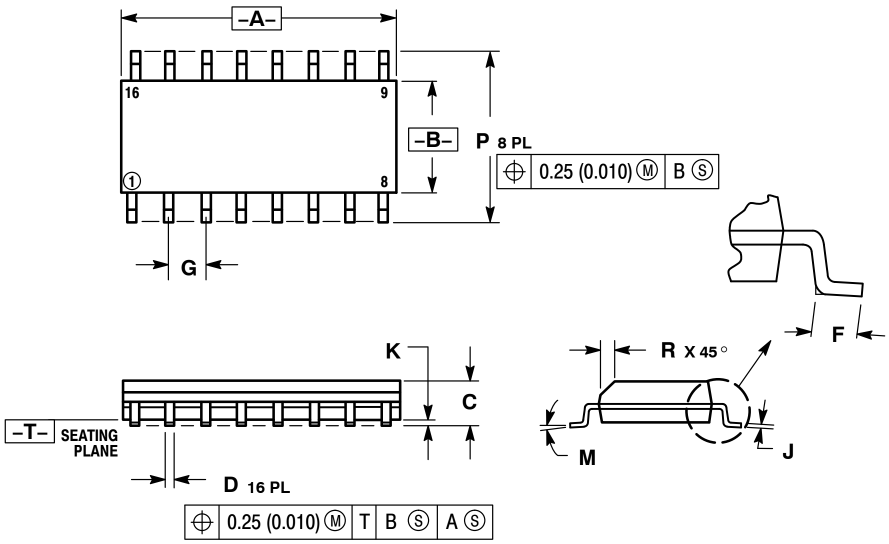
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 1:1

SOIC−16
CASE 751B−05
ISSUE K

DATE 29 DEC 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

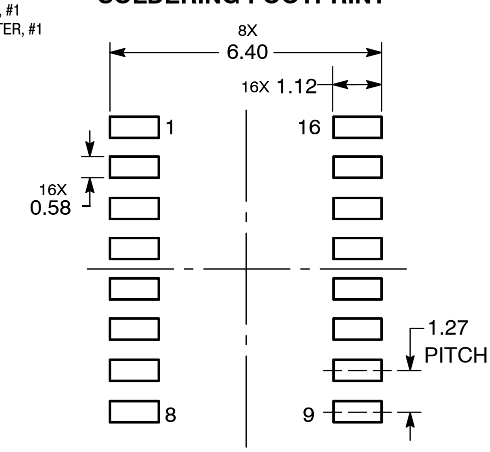
STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

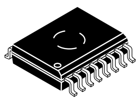
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98ASB42566B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC−16	PAGE 1 OF 1



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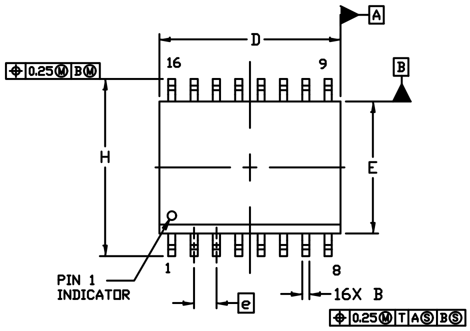
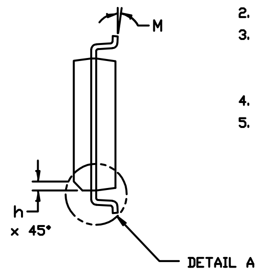
SCALE 1:1

SOIC−16 WB
CASE 751G
ISSUE E

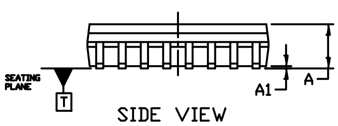
DATE 08 OCT 2021



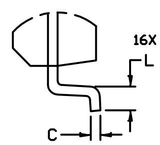
TOP VIEW



END VIEW



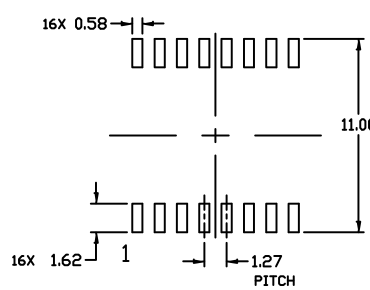
SIDE VIEW



DETAIL A
2X SCALE

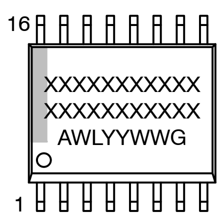
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION OR FLASH TO BE 0.15 PER SIDE.

	MILLIMETERS	
DIM	MIN.	MAX.
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.53 REF	
L	0.50	0.90
M	0°	7°



RECOMMENDED
MOUNTING FOOTPRINT

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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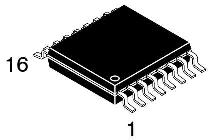
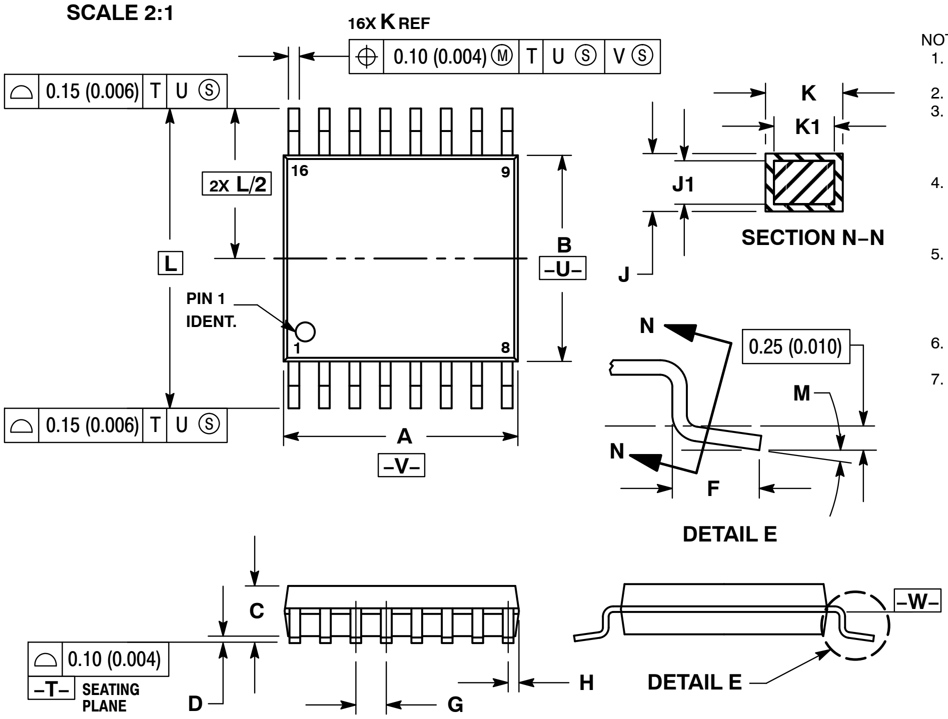
DESCRIPTION:	SOIC−16 WB	PAGE 1 OF 1



SCALE 2:1

TSSOP−16 WB
CASE 948F
ISSUE B

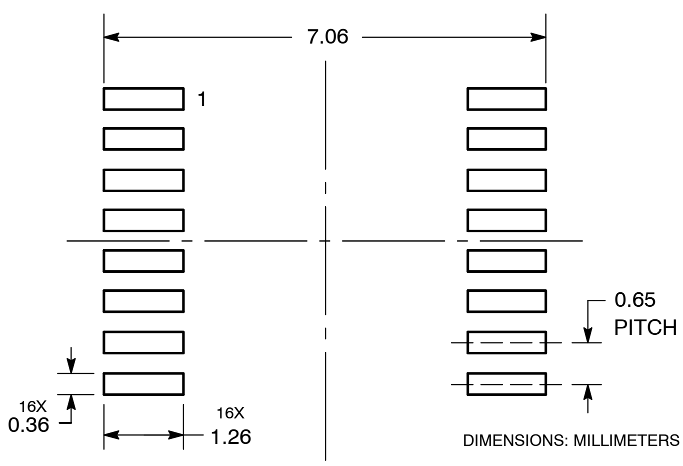
DATE 19 OCT 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



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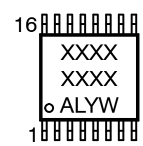
GENERIC MARKING DIAGRAM*



XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
G or ▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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