



14 Gbps, DUAL D-TYPE FLIP-FLOP WITH COMMON CLOCK & PROGRAMMABLE OUTPUT VOLTAGE

Typical Applications

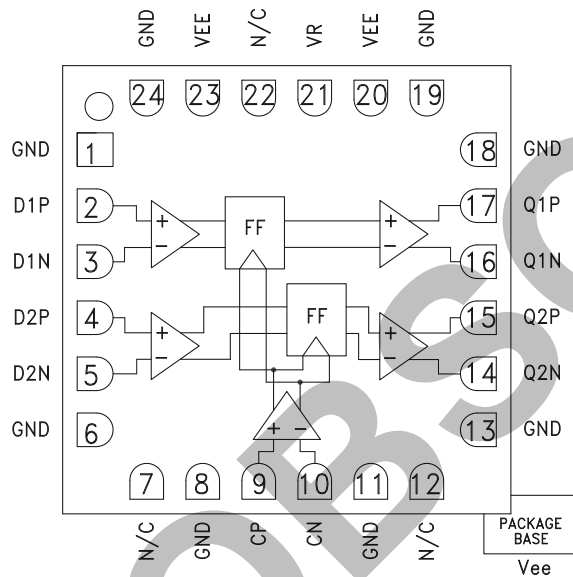
The HMC953LC4B is ideal for:

- 16G Fiber Channel
- Serial Data Transmission up to 14 Gbps
- Digital Logic Systems up to 14 GHz
- Matched Delay Applications
- Broadband Test & Measurement

Features

- Supports High Data Rates: up to 14 Gbps
- Differential or Single-Ended Operation
- Fast Rise and Fall Times: 22 / 20 ps
- Low Power Consumption: 442 mW typ.
- Programmable Differential Output Voltage Swing: 600 - 1300 mVp-p
- Propagation Delay: 104 ps
- Single Supply: -3.3 V
- 24 Lead Ceramic 4x4 mm SMT Package: 16 mm²

Functional Diagram



General Description

The HMC953LC4B is a Differential Dual D-Type Flip Flop with a common clock to support data transmission rates of up to 14 Gbps, and clock port operation of up to 14 GHz. During normal operation, dual differential data is transferred to the respective outputs on the positive edge of the clock. Reversing the clock inputs allows for negative-edge triggered applications. The HMC953LC4B also features an output level control pin, VR, which allows for loss compensation or for signal level optimization.

All differential input signals to the HMC953LC4B are terminated with 50 Ohms to ground on-chip, and may be either AC or DC coupled. The outputs of the HMC953LC4B may be operated either differentially or single-ended. Outputs can be connected directly to a 50 Ohm terminated system, while DC blocking capacitors may be used if the terminating system is 50 Ohms to a non-ground DC voltage. The HMC-953LC4B operates from a single -3.3 V DC supply and is available in a ceramic RoHS-compliant 4x4 mm SMT package.

Electrical Specifications, T_A = +25 °C, V_{ee} = -3.3 V

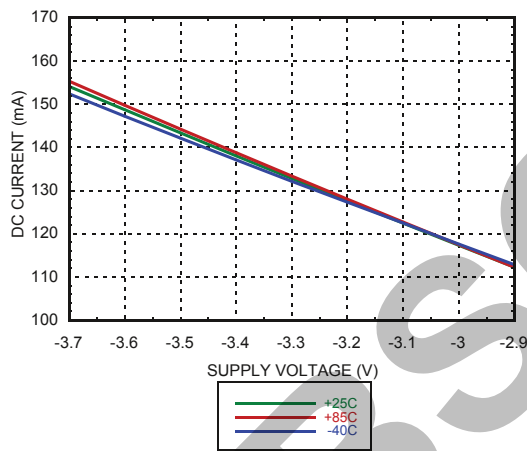
| Parameter | Conditions | Min. | Typ. | Max | Units |
|--------------------------|----------------------------|------|------|------|-------|
| Power Supply Voltage | | -3.6 | -3.3 | -3.0 | V |
| Power Supply Current | | | 134 | | mA |
| Maximum Data Rate | | | 14 | | Gbps |
| Maximum Select Rate | | | 14 | | GHz |
| Input Voltage Range | | -1.5 | | 0.5 | V |
| Input Differential Range | | 0.1 | | 2.0 | Vp-p |
| Input Return Loss | Frequency <11 GHz | | 10 | | dB |
| Output Amplitude | Single-Ended, peak-to-peak | | 580 | | mVp-p |
| | Differential, peak-to-peak | | 1160 | | mVp-p |

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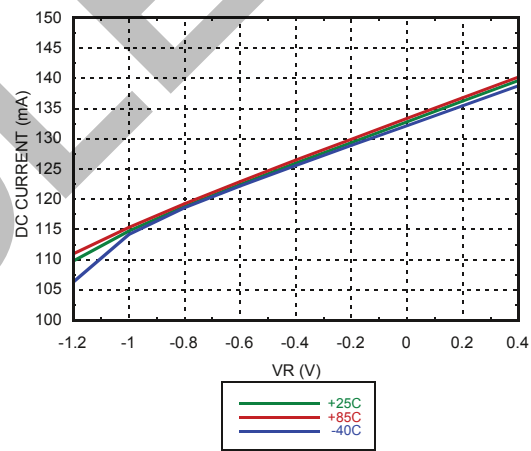
Electrical Specifications (continued)

| Parameter | Conditions | Min. | Typ. | Max | Units |
|--------------------------------------|---|------|---------|------|---------|
| Output High Voltage | | | -20 | | mV |
| Output Low Voltage | | | -600 | | mV |
| Output Rise / Fall Time | Differential, 20% - 80% | | 22 / 20 | | ps |
| Output Return Loss | Frequency <13 GHz | | 10 | | dB |
| Random Jitter, Jr | rms | | 0.11 | 0.16 | ps rms |
| Deterministic Jitter, Jd | peak-to-peak, 2 ¹⁵ -1 PRBS input [2] | | 2 | | ps, p-p |
| Propagation Delay, Clock to Data, td | | | 104 | | ps |
| Clock Phase Margin | 13 GHz | | 245 | | deg |
| Set Up & Hold Time, t _{SH} | | | 25 | | ps |

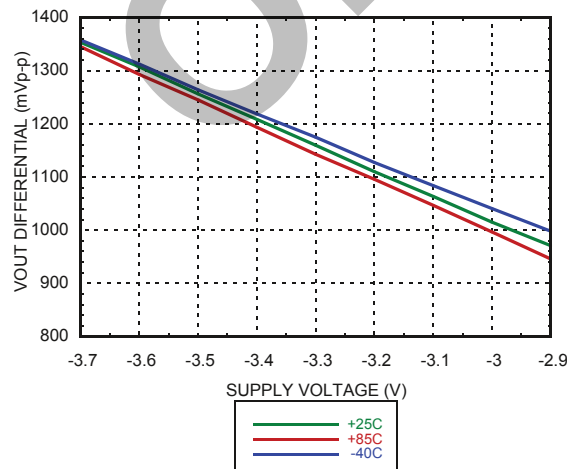
DC Current vs. Supply Voltage [1][2]



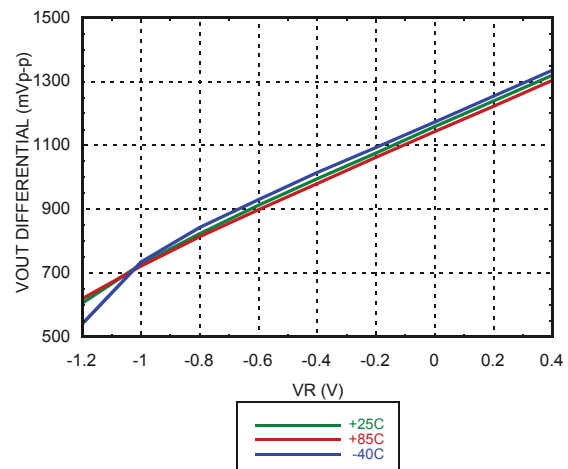
DC Current vs. VR [2][3]



Output Differential Voltage vs. Supply Voltage [1][2]



Output Differential Voltage vs. VR [2][3]



[1] VR = 0.0 V

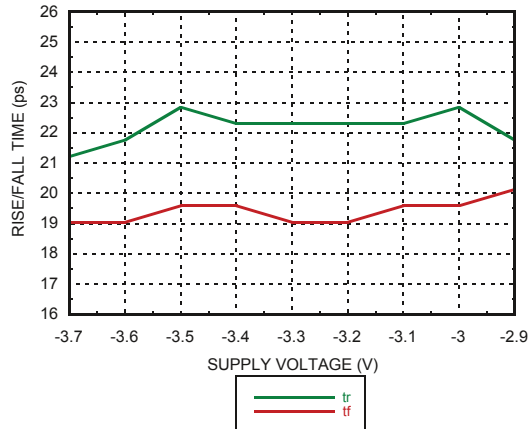
[2] Frequency = 13 GHz

Vee = -3.3 V

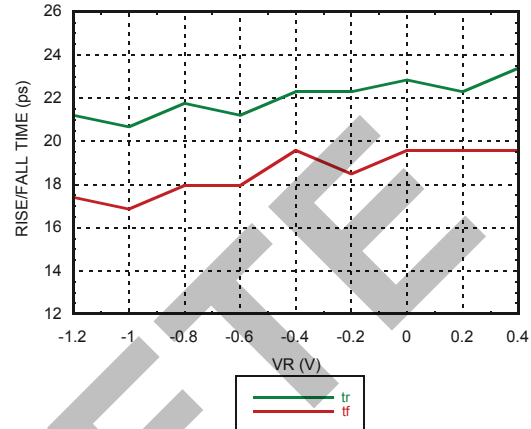


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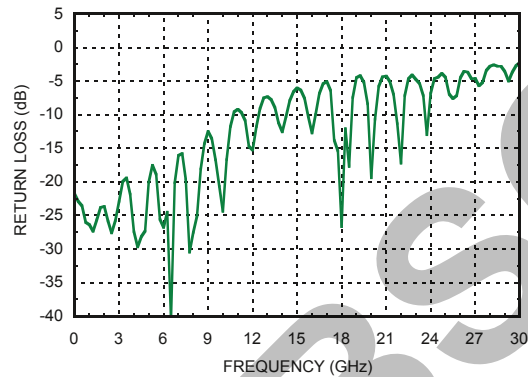
Rise / Fall Time vs. Supply Voltage [1][2]



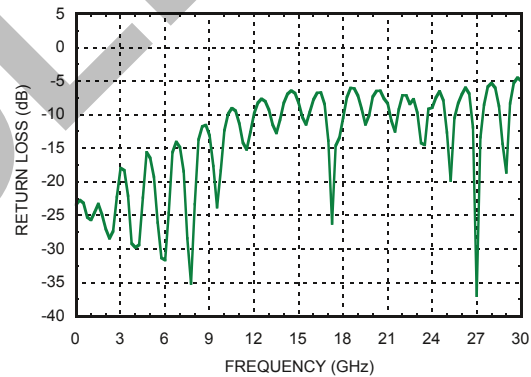
Rise / Fall Time vs. VR [2][3]



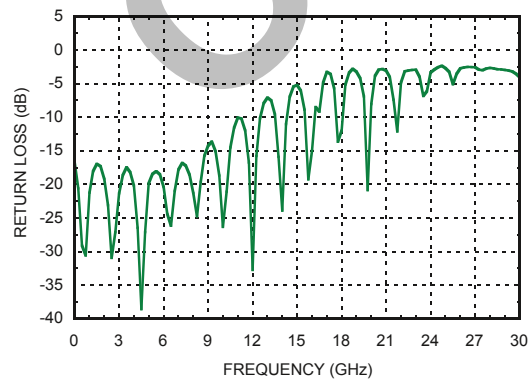
Clock Input Return Loss vs. Frequency [1][3][4]



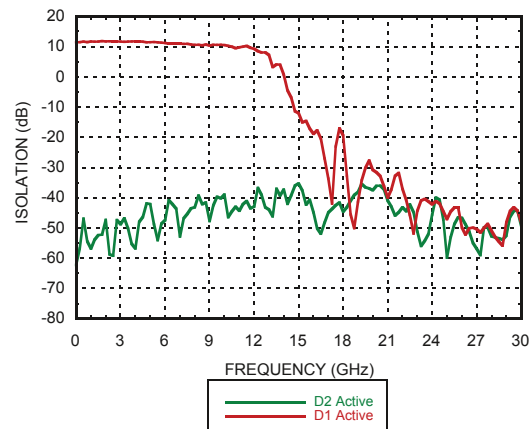
Data Input Return Loss vs. Frequency [1][3][4]



Output Return Loss vs. Frequency [1][3][4]



Isolation [1][3][5]



[1] VR = 0.0 V

[2] Frequency = 13 GHz

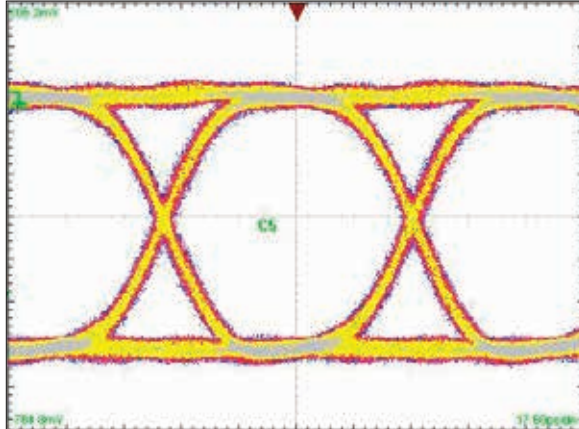
[3] Vee = -3.3 V

[4] Device measured on evaluation board with gating after connector

[5] Device measured on evaluation board with port extensions

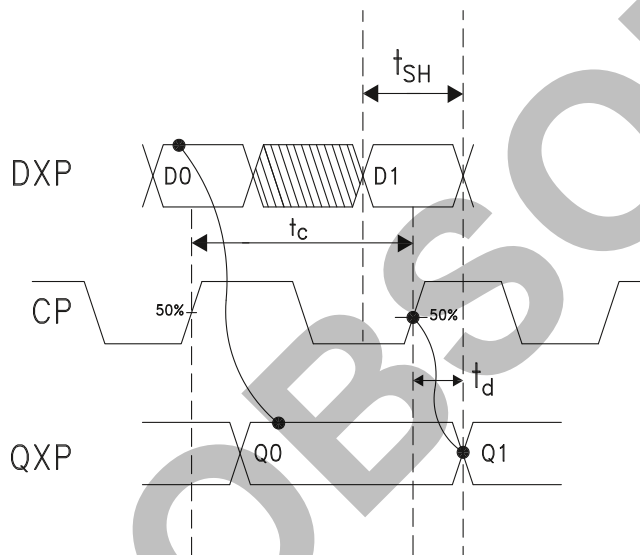
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Eye Diagram



[1] Test Conditions:
 Waveform generated with an Agilent N4903A
 J-Bert differential 400 mV 13 Gbps PN 2¹⁵-1 input signal.
 Eye Diagram data presented on a Tektronix CSA 8000

Timing Diagram



Truth Table

| Inputs | | | Outputs | |
|--------|----|------|---------|----|
| D1 | D2 | C | Q1 | Q2 |
| L | X | L->H | L | X |
| H | X | L->H | H | X |
| X | L | L->H | X | L |
| X | H | L->H | X | H |

H = Positive voltage level
 L = Negative voltage level

Notes:
 DX = DXP - DXN
 C = CP - CN
 QX = QXP - QXN

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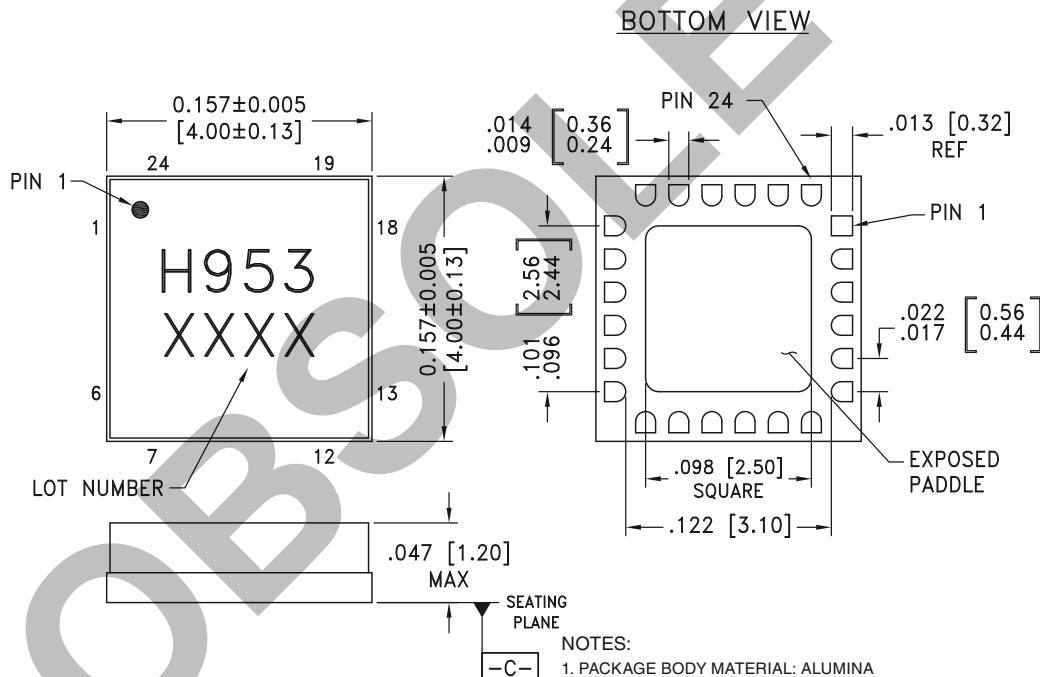
Absolute Maximum Ratings

| | |
|--|-------------------|
| Power Supply Voltage (Vee) | -3.75 V to +0.5 V |
| Input Signals | -2.0 V to 0.5 V |
| Output Signals | -1.5 V to 0.5 V |
| Junction Temperature | 125 °C |
| Continuous P _{diss} (T = 85 °C (derate 30.0 mW/°C above 85 °C)) | 1.22 W |
| Thermal Resistance (R _{th-j-p}) Worst case device to package paddle | 32.8 °C/W |
| Storage Temperature | -65 °C to +150 °C |
| Operating Temperature | -40 to +85 °C |
| ESD Sensitivity (HBM) | Class 1B |



**ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS**

Outline Drawing



Package Information


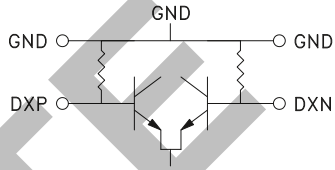
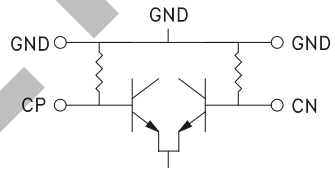
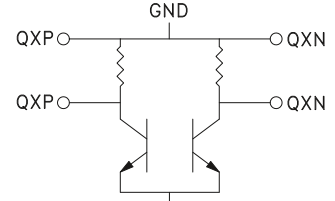

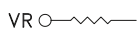
| Part Number | Package Body Material | Lead Finish | MSL Rating | Package Marking ^[2] |
|-------------|-----------------------|------------------|---------------------|--------------------------------|
| HMC953LC4B | Alumina, White | Gold over Nickel | MSL3 ^[1] | H953 XXXX |

[1] Max peak reflow temperature of 260 °C

[2] 4-Digit lot number XXXX

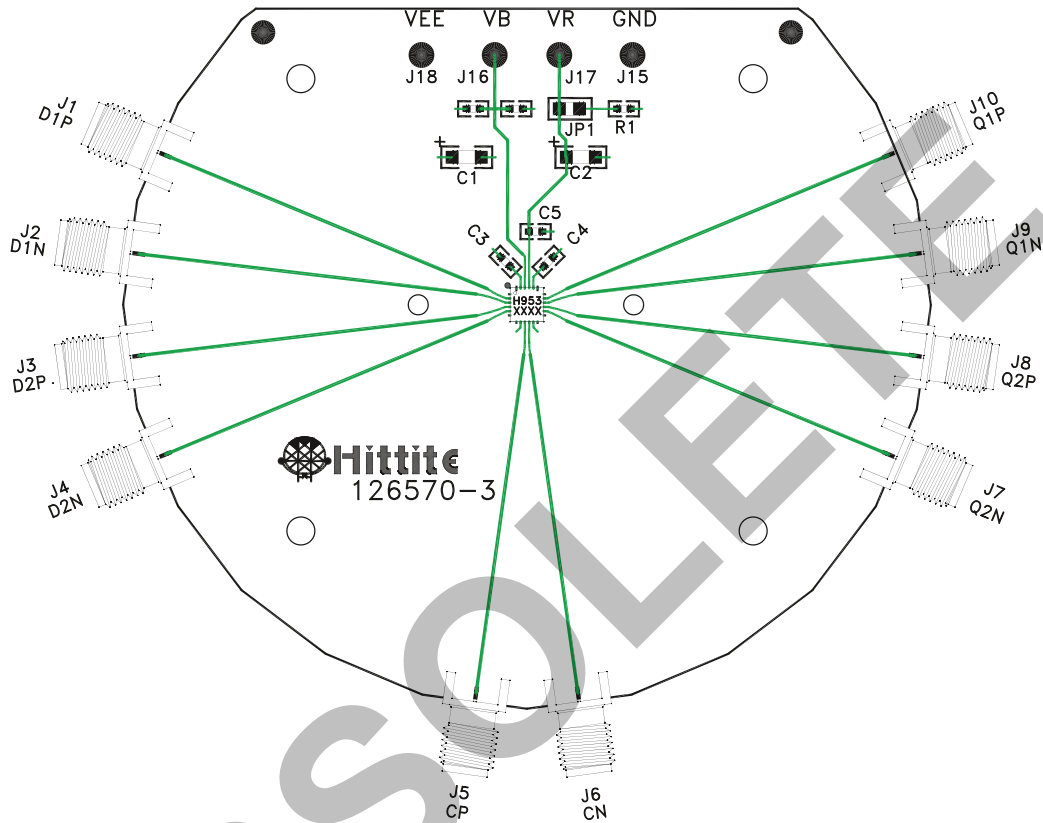
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Pin Descriptions

| Pin Number | Function | Description | Interface Schematic |
|------------------------|--------------------|---|---|
| 1, 6, 8, 11, 13, 18 | GND | Signal Grounds. |  |
| 2, 3, 4, 5 | D1P, D1N, D2P, D2N | Differential Inputs: Current Mode Logic (CML) referenced to positive supply. |  |
| 7, 12, 22 | N/C | No connection necessary. These pins may be connected to RF/DC ground without affecting performance. | |
| 9, 10 | CP, CN | Differential Clock Inputs: Current Mode Logic (CML) referenced to positive supply. |  |
| 14, 15, 16, 17 | Q2N, Q2P, Q1N, Q1P | Differential Outputs: Current Mode Logic (CML) referenced to positive supply. |  |
| 19, 24 | GND | Supply Ground |  |
| 20, 23 Package Base | Vee | These pins and the exposed paddle must be connected to the negative voltage supply. | |
| 21 | VR | Output level control. Output level may be increased or decreased by applying a voltage to VR per "Output Differential vs. VR" plot. |  |

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Evaluation PCB



List of Materials for Evaluation PCB 126572 [1]

| Item | Description |
|-----------|----------------------------------|
| J1 - J10 | PCB Mount SMA RF Connectors |
| J15 - J18 | DC Pin |
| JP1 | 0.1" Header with Shorting Jumper |
| C1, C2 | 4.7 μ F Capacitor, Tantalum |
| C3 - C5 | 100 pF Capacitor, 0603 Pkg. |
| R1 | 10 Ohm Resistor, 0603 Pkg. |
| U1 | HMC953LC4B Dual D-Type Flip Flop |
| PCB [2] | 126570 Evaluation Board |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed package base should be connected to Vee. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request. Install jumper on JP1 to short VR to GND for normal operation.

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Application Circuit

