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SMPS Series N-Channel IGBT with Anti-Parallel Hyperfast Diode
600 V

HGTG7N60A4D, HGTP7N60A4D, HGT1S7N60A4DS

The HGTG7N60A4D, HGTP7N60A4D and HGT1S7N60A4DS are MOS gated high voltage switching devices combining the best features of MOSFETs and bipolar transistors. These devices have the high input impedance of a MOSFET and the low on−state conduction loss of a bipolar transistor. The much lower on−state voltage drop varies only moderately between 25°C and 150°C. The IGBT used is the development type TA49331. The diode used in anti−parallel is the development type TA49370.

This IGBT is ideal for many high voltage switching applications operating at high frequencies where low conduction losses are essential. This device has been optimized for high frequency switch mode power supplies.

Formerly Developmental Type TA49333.

Features

- >100 kHz Operation at 390 V, 7 A
- 200 kHz Operation at 390 V, 5 A
- 600 V Switching SOA Capability
- Typical Fall Time: 75 ns at T_J = 125°C
- Low Conduction Loss
- Temperature Compensating SABER™ Model www.onsemi.com
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

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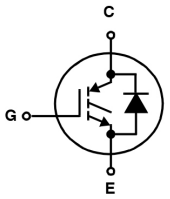
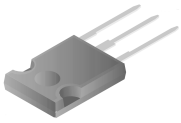
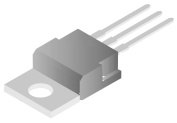




TO−247−3LD
CASE 340CK



TO−220−3LD
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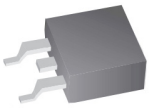
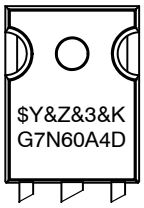
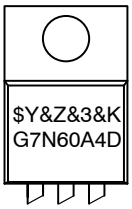
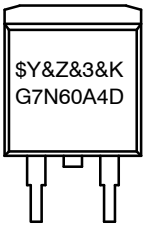


D2PAK−3
CASE 418AJ

MARKING DIAGRAMS







&Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= 3−Digit Date Code
&K	= 2−Digit Lot Traceability Code
G7N60A4D	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

PART NUMBER	PACKAGE	BRAND
HGTG7N60A4D	TO−247	G7N60A4D
HGTP7N60A4D	TO−220AB	G7N60A4D
HGT1S7N60A4DS	TO−263AB	G7N60A4D

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO−263AB variant in tape and reel, e.g., HGT1S7N60A4DS9A.

PACKAGING

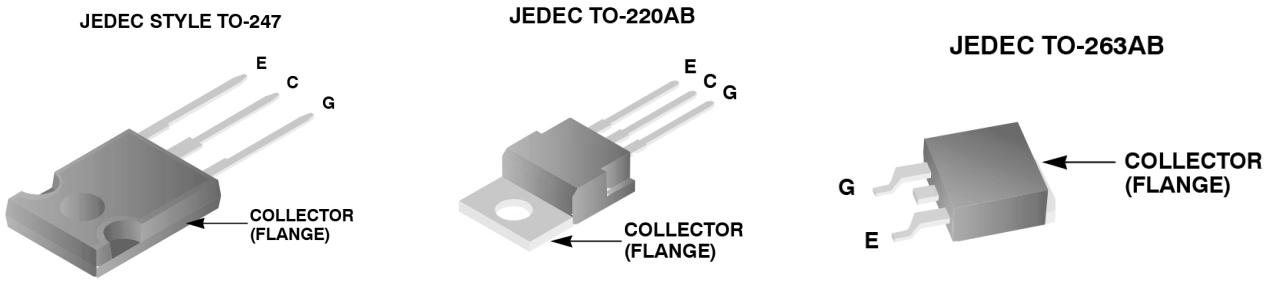


Figure 1.

ABSOLUTE MAXIMUM RATINGS T_C = 25°C Unless Otherwise Specified

Description	Symbol	All Types	Units
Collector to Emitter Voltage	BV_{CES}	600	V
Collector Current Continuous			
At T_C = 25°C	I_{C25}	34	A
At T_C = 110°C	I_{C110}	14	A
Collector Current Pulsed (Note 1)	I_{CM}	56	A
Gate to Emitter Voltage Continuous	V_{GES}	±20	V
Gate to Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at T_J = 150°C (Figure 1)	SSOA	35 A at 600 V	
Power Dissipation Total at T_C = 25°C	P_D	125	W
Power Dissipation Derating T_C > 25°C		1.0	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	−55 to 150	°C
Maximum Lead Temperature for Soldering			
Leads at 0.063 in (1.6 mm) from case for 10 s	T_L	300	
Package Body for 10 s, see Tech Brief 334	T_{PKG}	260	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Pulse width limited by maximum junction temperature.

ELECTRICAL SPECIFICATIONS T_J = 25 °C Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Collector to Emitter Breakdown Voltage	BV_{CES}	I_C = 250 μA, V_{GE} = 0 V		600	–	–	V
Collector to Emitter Leakage Current	I_{CES}	V_{CE} = 600 V	T_C = 25°C	–	–	250	μA
			T_C = 125°C	–	–	2	mA
Collector to Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 7 A, V_{GE} = 15 V	T_C = 25°C	–	1.9	2.7	V
			T_C = 150°C	–	1.6	2.2	V
Gate to Emitter Threshold Voltage	$V_{GE(TH)}$	I_C = 250 μA, V_{CE} = 600 V		4.5	5.9	7	V
Gate to Emitter Leakage Current	I_{GES}	V_{GE} = ±20 V		–	–	±250	nA
Switching SOA	SSOA	T_J = 150°C, R_G = 25 Ω, V_{GE} = 15 V, L = 100 μH, V_{CE} = 600 V		35	–	–	A
Gate to Emitter Plateau Voltage	V_{GEP}	I_C = 7 A, V_{CE} = 300 V		–	9	–	V
On−State Gate Charge	$Q_{G(ON)}$	I_C = 7 A, V_{CE} = 300 V	V_{GE} = 15 V	–	37	45	nC
			V_{GE} = 20 V	–	48	60	nC
Current Turn−On Delay Time	$t_{d(ON)I}$	IGBT and Diode at T_J = 25°C, I_{CE} = 7 A, V_{CE} = 390 V, V_{GE} = 15 V, R_G = 25 Ω, L = 1 mH, Test Circuit (Figure 24)		–	11	–	ns
Current Rise Time	t_{rI}			–	11	–	ns
Current Turn−Off Delay Time	$t_{d(OFF)I}$			–	100	–	ns
Current Fall Time	t_{fI}			–	45	–	ns
Turn−On Energy	E_{ON1}			–	55	–	μJ
Turn−On Energy	E_{ON2}			–	120	150	μJ
Turn−Off Energy (Note 3)	E_{OFF}			–	60	75	μJ
Current Turn−On Delay Time	$t_{d(ON)I}$	IGBT and Diode at T_J = 150°C, I_{CE} = 7 A, V_{CE} = 390 V, V_{GE} = 15 V, R_G = 25 Ω, L = 1 mH, Test Circuit (Figure 24)		–	10	–	ns
Current Rise Time	t_{rI}			–	7	–	ns
Current Turn−Off Delay Time	$t_{d(OFF)I}$			–	130	150	ns
Current Fall Time	t_{fI}			–	75	85	ns
Turn−On Energy	E_{ON1}			–	50	–	μJ
Turn−On Energy	E_{ON2}			–	200	215	μJ
Turn−Off Energy (Note 3)	E_{OFF}			–	125	170	μJ
Diode Forward Voltage	V_{EC}	I_{EC} = 7 A		–	2.4	–	V
Diode Reverse Recovery Time	t_{rr}	I_{EC} = 7 A, dI_{EC}/dt = 200 A/μs		–	34	–	ns
		I_{EC} = 1 A, dI_{EC}/dt = 200 A/μs		–	22	–	ns
Thermal Resistance Junction To Case	$R_{\theta JC}$	IGBT		–	–	1.0	°C/W
		Diode		–	–	2.2	°C/W

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Values for two Turn−On loss conditions are shown for the convenience of the circuit designer. E_{ON1} is the turn−on loss of the IGBT only. E_{ON2} is the turn−on loss when a typical diode is used in the test circuit and the diode is at the same T_J as the IGBT. The diode type is specified in Figure 24.
3. Turn−Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0 A). All devices were tested per JEDEC Standard No. 24−1 Method for Measurement of Power Device Turn−Off Switching Loss. This test method produces the true total Turn−Off Energy Loss.

TYPICAL PERFORMANCE CURVES

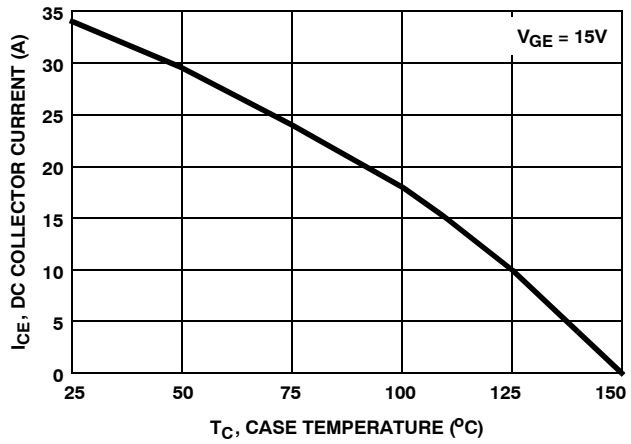


Figure 1. DC COLLECTOR CURRENT vs CASE TEMPERATURE

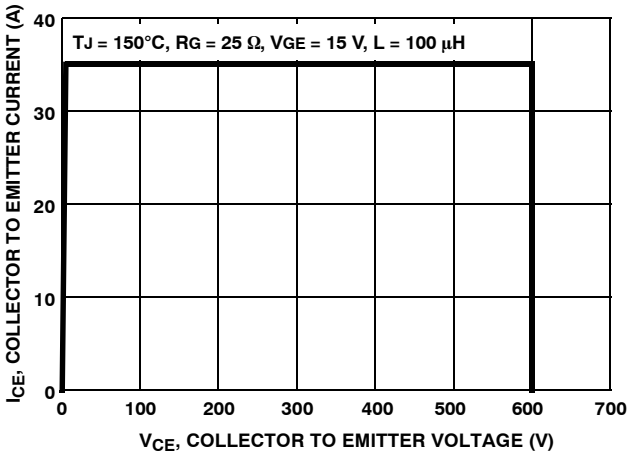


Figure 2. MINIMUM SWITCHING SAFE OPERATING AREA

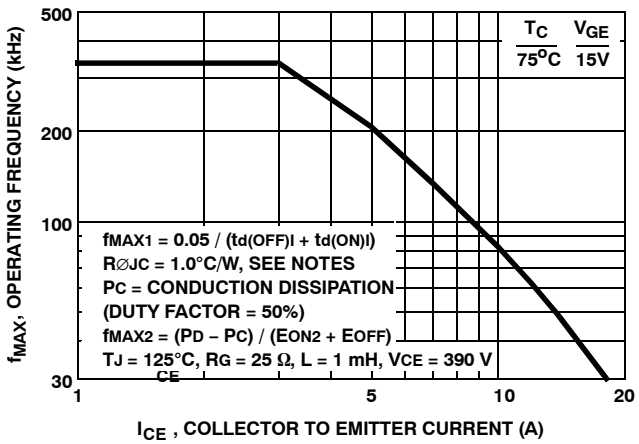


Figure 3. OPERATING FREQUENCY vs COLLECTOR TO EMITTER CURRENT

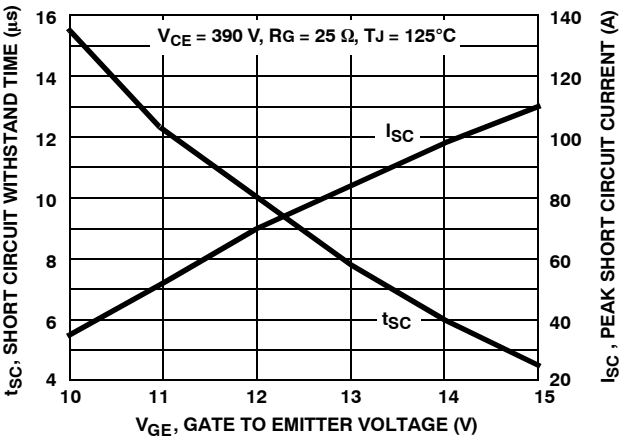


Figure 4. SHORT CIRCUIT WITHSTAND TIME

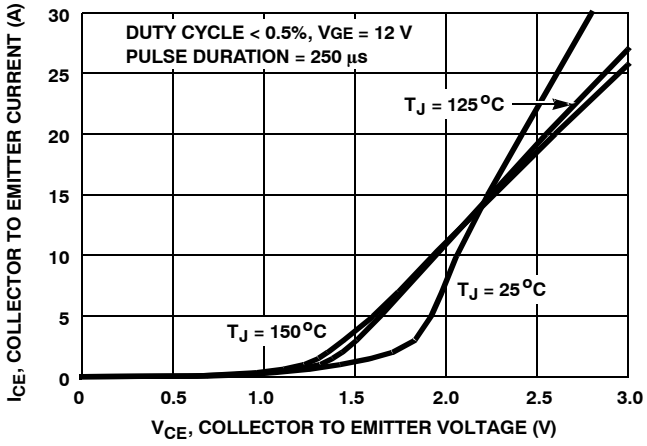


Figure 5. COLLECTOR TO EMITTER ON−STATE VOLTAGE

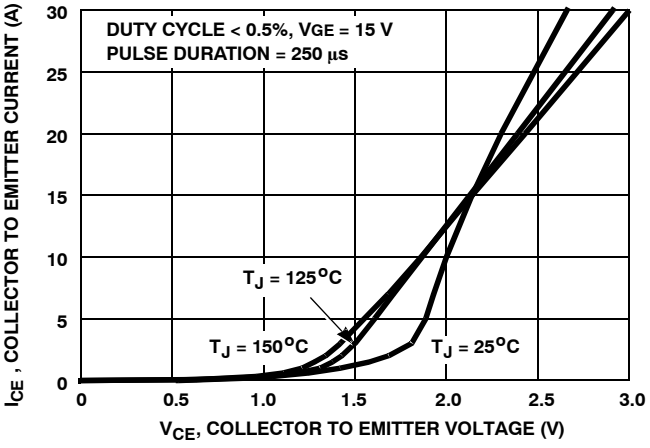


Figure 6. COLLECTOR TO EMITTER ON−STATE VOLTAGE

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

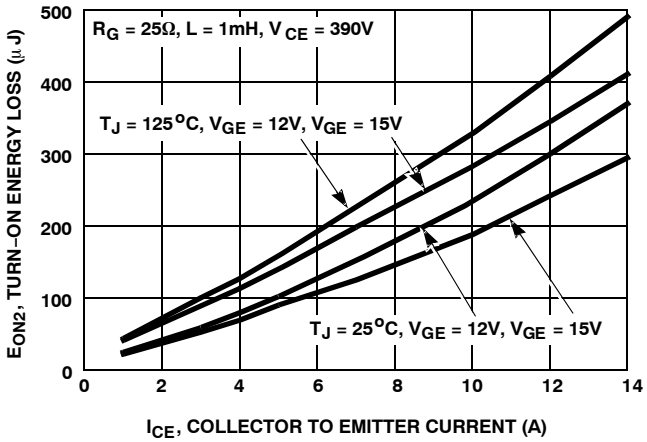


Figure 7. TURN−ON ENERGY LOSS vs COLLECTOR TO EMITTER CURRENT

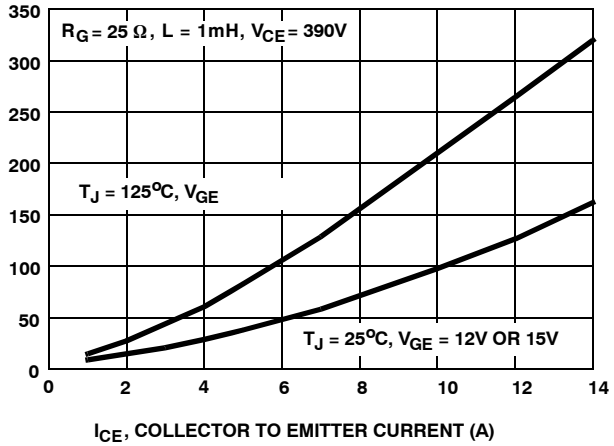


Figure 8. TURN−OFF ENERGY LOSS vs COLLECTOR TO EMITTER CURRENT

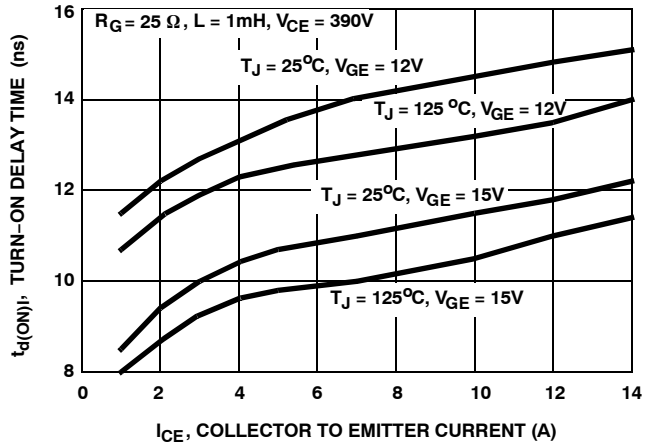


Figure 9. TURN−ON DELAY TIME vs COLLECTOR TO EMITTER CURRENT

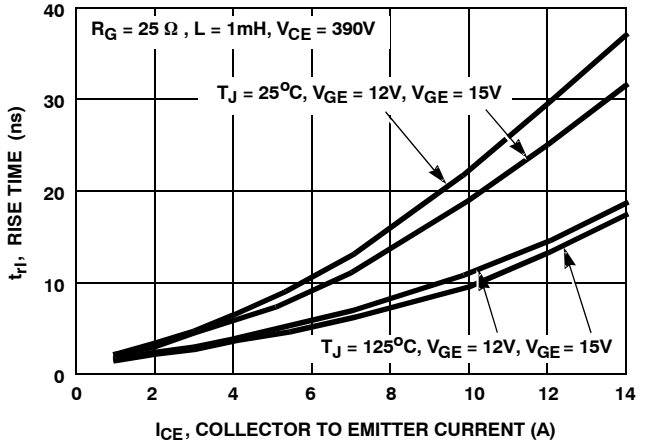


Figure 10. TURN−ON RISE TIME vs COLLECTOR TO EMITTER CURRENT

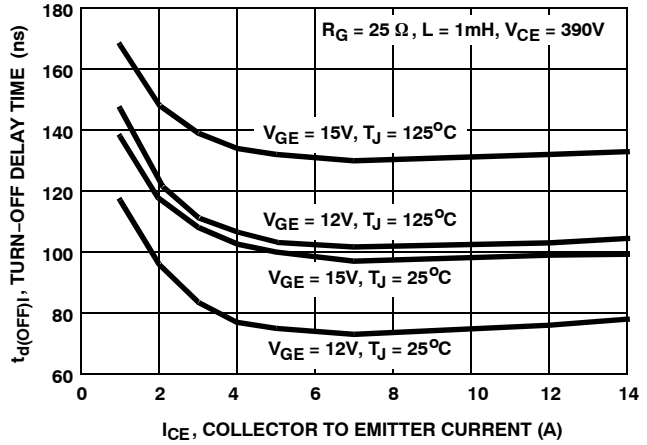


Figure 11. TURN−OFF DELAY TIME vs COLLECTOR TO EMITTER CURRENT

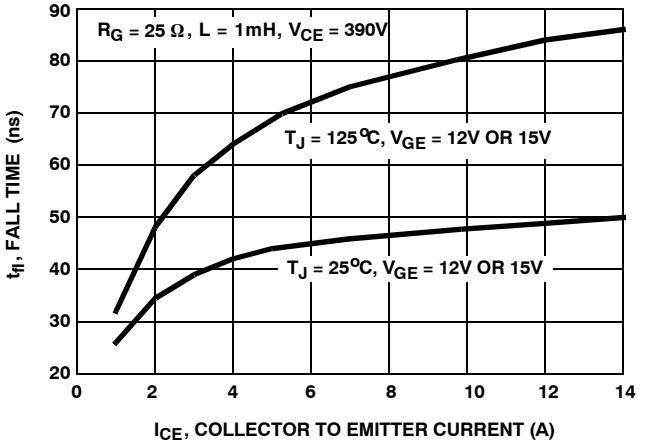


Figure 12. FALL TIME vs COLLECTOR TO EMITTER CURRENT

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

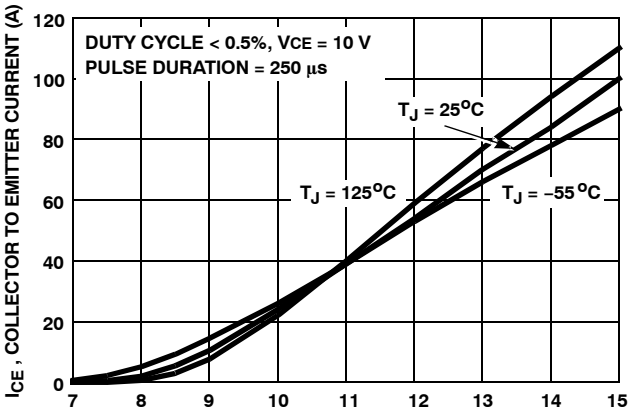


Figure 13. TRANSFER CHARACTERISTIC

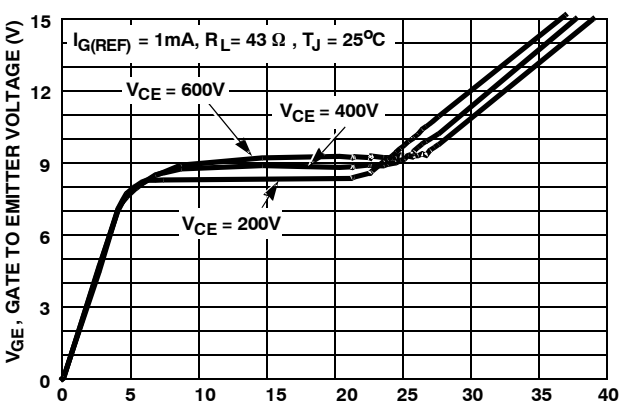


Figure 14. GATE CHARGE WAVEFORMS

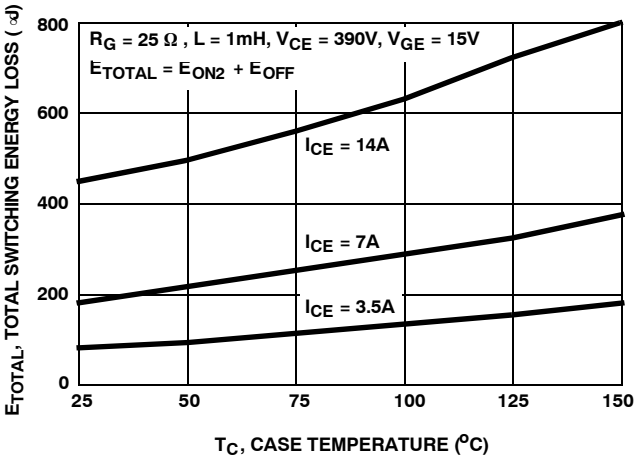


Figure 15. TOTAL SWITCHING LOSS vs CASE TEMPERATURE

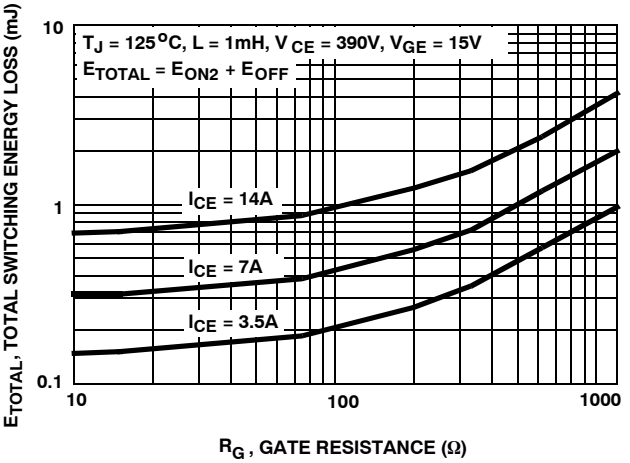


Figure 16. TOTAL SWITCHING LOSS vs GATE RESISTANCE

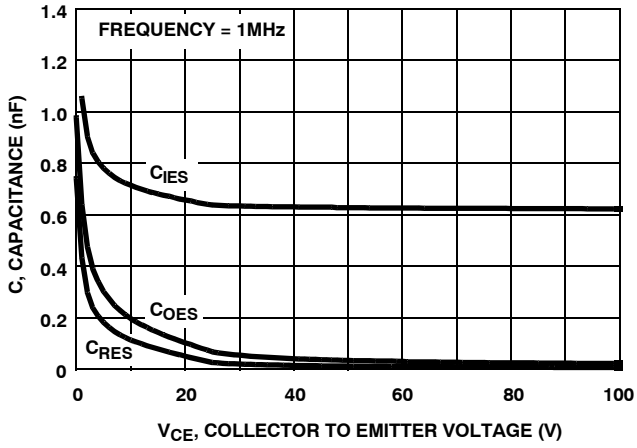


Figure 17. CAPACITANCE vs COLLECTOR TO EMITTER VOLTAGE

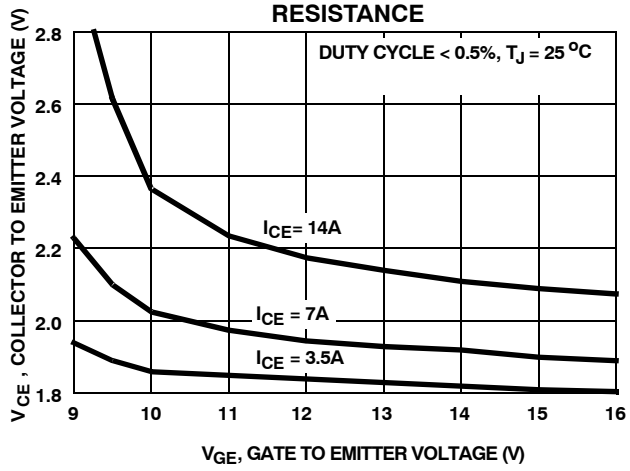


Figure 18. COLLECTOR TO EMITTER ON−STATE VOLTAGE vs GATE TO EMITTER VOLTAGE

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

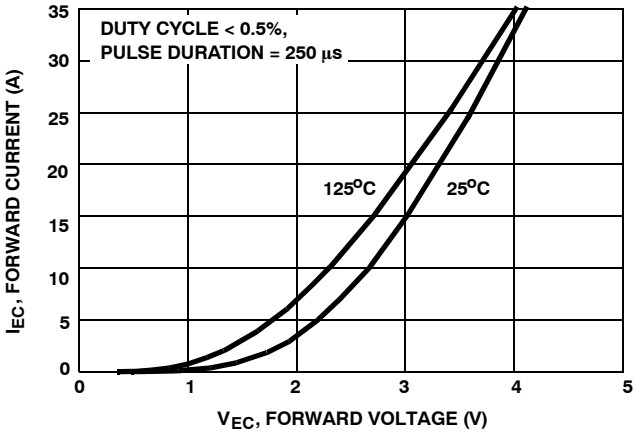


Figure 19. DIODE FORWARD CURRENT vs FORWARD VOLTAGE DROP

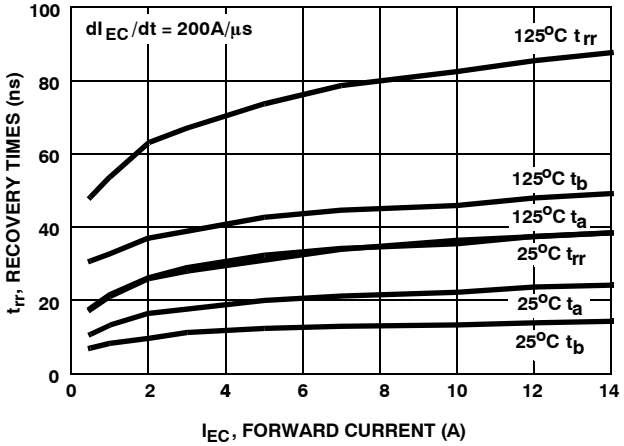


Figure 20. DIODE FORWARD CURRENT vs FORWARD VOLTAGE DROP

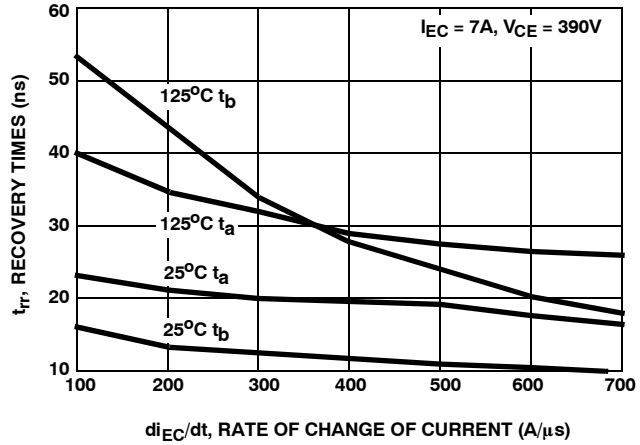


Figure 21. RECOVERY TIMES vs RATE OF CHANGE OF CURRENT

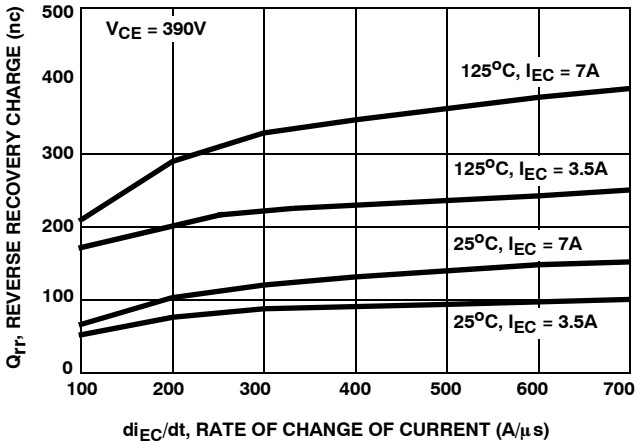


Figure 22. STORED CHARGE vs RATE OF CHANGE OF CURRENT

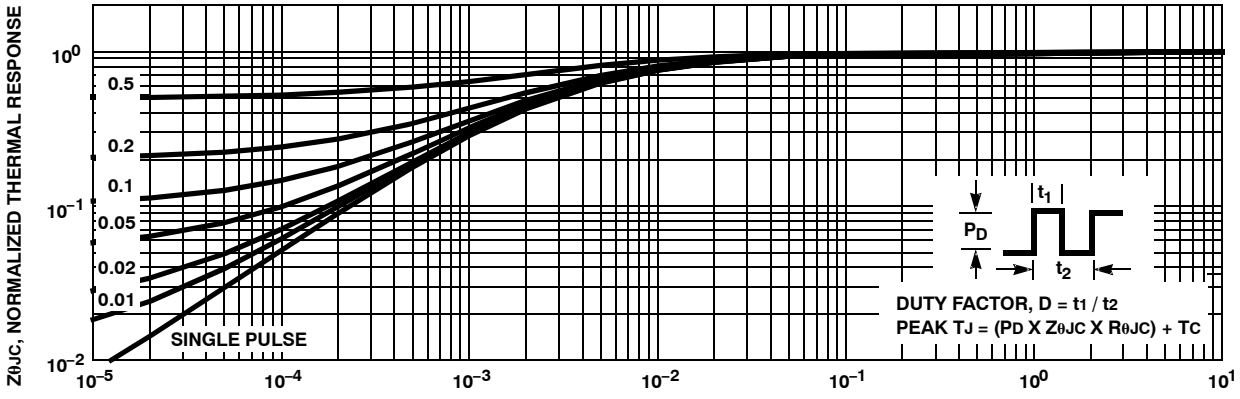


Figure 23. IGBT NORMALIZED TRANSIENT THERMAL RESPONSE, JUNCTION TO CASE

TEST CIRCUITS AND WAVEFORMS

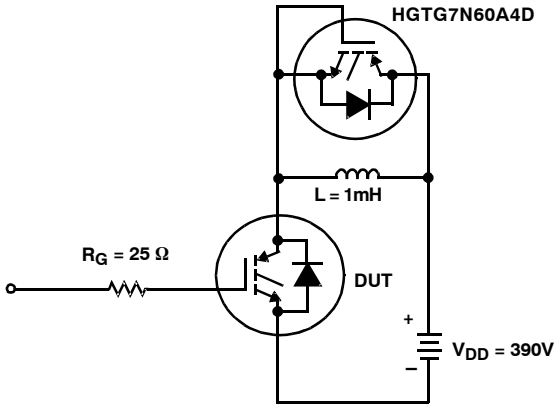


Figure 24. INDUCTIVE SWITCHING TEST CIRCUIT

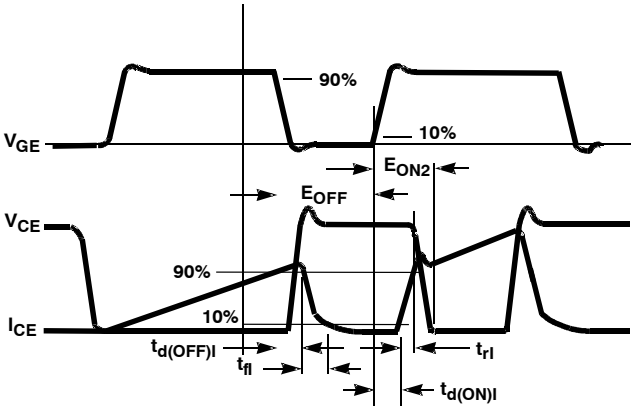


Figure 25. SWITCHING TEST WAVEFORMS

HANDLING PRECAUTIONS FOR IGBTS

Insulated Gate Bipolar Transistors are susceptible to gate−insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORBD™ LD26" or equivalent
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means − for example, with a metallic wristband
3. Tips of soldering irons should be grounded
4. Devices should never be inserted into or removed from circuits with power on
5. Gate Voltage Rating − Never exceed the gate−voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region
6. Gate Termination − The gates of these devices are essentially capacitors. Circuits that leave the gate open− circuited or floating should be avoided. These conditions can result in turn−on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup
7. Gate Protection - These devices do not have an internal monolithic Zener diode from gate to emitter. If gate protection is required an external Zener is recommended

OPERATING FREQUENCY INFORMATION

Operating frequency information for a typical device (Figure 3) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 6, 7, 8, 9 and 11. The operating frequency plot (Figure 3) of a typical device shows f_{MAX1} or f_{MAX2}; whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/(t_{d(OFF)I} + t_{d(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on−state time for a 50% duty factor. Other definitions are possible. $t_{d(OFF)I}$ and $t_{d(ON)I}$ are defined in Figure 25. Device turn−off delay can establish an additional frequency limiting condition for an application other than T_{JM}. $t_{d(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON2})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JM} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 3) and the conduction losses (P_C) are approximated by

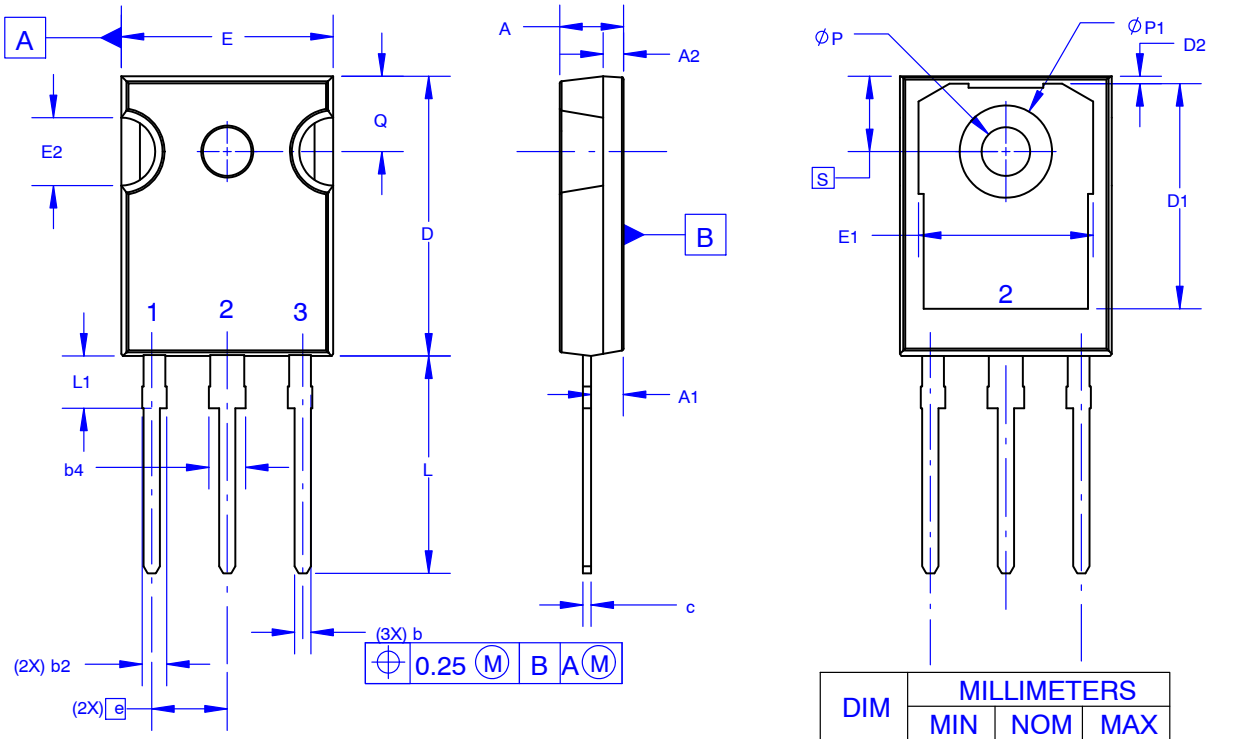
$$P_C = (V_{CE} \times I_{CE})/2 \qquad \text{(eq. 1)}$$

E_{ON2} and E_{OFF} are defined in the switching waveforms shown in Figure 25. E_{ON2} is the integral of the instantaneous power loss (I_{CE} x V_{CE}) during turn−on and E_{OFF} is the integral of the instantaneous power loss (I_{CE} x V_{CE}) during turn−off. All tail losses are included in the calculation for E_{OFF}; i.e., the collector current equals zero ($I_{CE} = 0$).

PACKAGE DIMENSIONS

TO−247−3LD SHORT LEAD
CASE 340CK
ISSUE A

DATE 31 JAN 2019

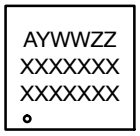


DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D	20.32	20.57	20.82
D1	13.08	~	~
D2	0.51	0.93	1.35
E	15.37	15.62	15.87
E1	12.81	~	~
E2	4.96	5.08	5.20
e	~	5.56	~
L	15.75	16.00	16.25
L1	3.69	3.81	3.93
ØP	3.51	3.58	3.65
ØP1	6.60	6.80	7.00
Q	5.34	5.46	5.58
S	5.34	5.46	5.58

NOTES: UNLESS OTHERWISE SPECIFIED.

A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

GENERIC MARKING DIAGRAM*

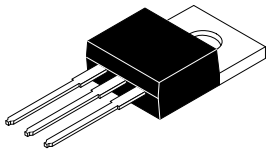


XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

TO−220−3LD
CASE 340AT
ISSUE A

DATE 03 OCT 2017

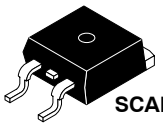


Scale 1:1

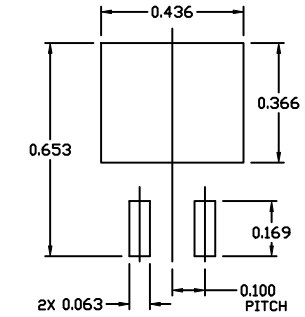
NOTES:
A) REFERENCE JEDEC, TO-220, VARIATION AB
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
E DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS AS BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.10 - 1.45
G PRESENCE IS SUPPLIER DEPENDENT
H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

D²PAK−3 (TO−263, 3−LEAD)
CASE 418AJ
ISSUE E

DATE 25 OCT 2019



SCALE 1:1



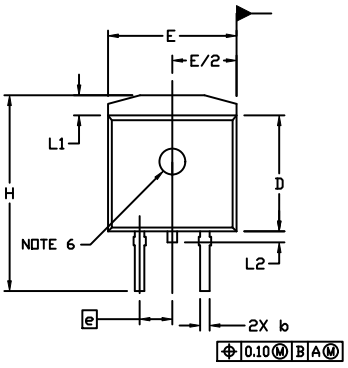
RECOMMENDED
MOUNTING FOOTPRINT

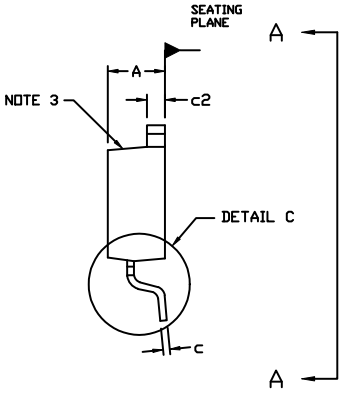
For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

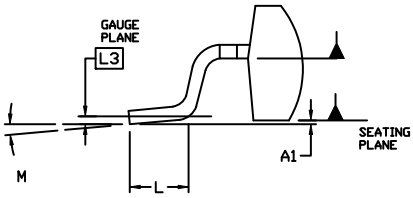
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. CHAMFER OPTIONAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
6. OPTIONAL MOLD FEATURE.
7. ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

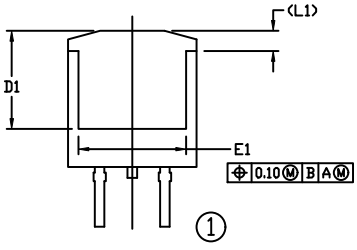
	INCHES		MILLIMETERS	
DIM	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100 BSC		2.54 BSC	
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010 BSC		0.25 BSC	
M	−8°	8°	−8°	8°



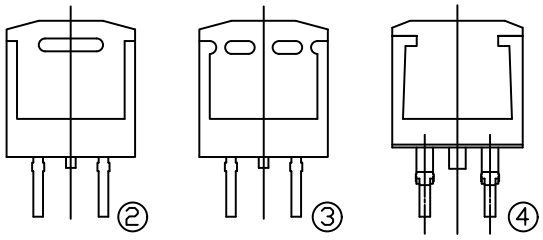




DETAIL C
TIP LEADFORM
ROTATED 90° CW

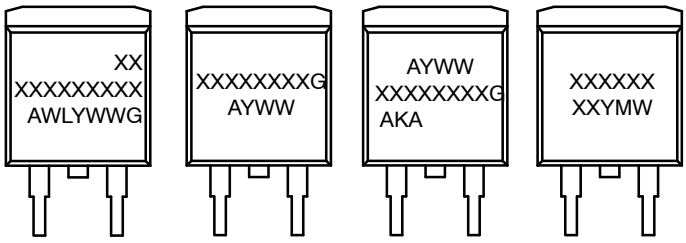


VIEW A−A



VIEW A−A
OPTIONAL CONSTRUCTIONS

GENERIC MARKING DIAGRAMS*



IC **Standard** **Rectifier** **SSG**

XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
W = Week Code (SSG)
M = Month Code (SSG)
G = Pb−Free Package
AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

PUBLICATION ORDERING INFORMATION

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