

**POWER MOSFET
THRU-HOLE (TO-254AA)**
**60V, N-CHANNEL
HEXFET MOSFET TECHNOLOGY**
Product Summary

Part Number	$R_{DS(on)}$	I_D
IRFM044	0.04 Ω	35A*


Description

HEXFET MOSFET technology is the key to IR HiRel advanced line of power MOSFET transistors. The efficient geometry design achieves very low on-state resistance combined with high trans conductance. HEXFET transistors also feature all of the well-established advantages of MOSFETs, such as voltage control, very fast switching, ease of paralleling and electrical parameter temperature stability. They are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, high energy pulse circuits, and virtually any application where high reliability is required. The HEXFET transistor's totally isolated package eliminates the need for additional isolating material between the device and the heat sink. This improves thermal efficiency and reduces drain capacitance.

Features

- Simple Drive Requirements
- Hermetically Sealed
- Electrically Isolated
- Dynamic dv/dt Rating
- Light Weight

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
$I_{D1} @ V_{GS} = 10V, T_C = 25^\circ C$	Continuous Drain Current	35*	A
$I_{D2} @ V_{GS} = 10V, T_C = 100^\circ C$	Continuous Drain Current	28	
I_{DM}	Pulsed Drain Current ①	180	
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	125	W
	Linear Derating Factor	1.0	W/ $^\circ C$
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	340	mJ
I_{AR}	Avalanche Current ①	35	A
E_{AR}	Repetitive Avalanche Energy ①	12.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	$^\circ C$
	Lead Temperature	300 (0.063 in. /1.6 mm from case for	
	Weight	9.3 (Typical)	

* Current is limited by package
For Footnotes refer to the page 2.

Electrical Characteristics @ T_J = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	60	—	—	V	V _{GS} = 0V, I _D = 1.0mA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.68	—	V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-State Resistance	—	—	0.04	Ω	V _{GS} = 10V, I _{D2} = 28A ④
		—	—	0.05		V _{GS} = 10V, I _{D1} = 35A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
G _{fs}	Forward Transconductance	17	—	—	S	V _{DS} = 15V, I _D = 28A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	25	μA	V _{DS} = 48V, V _{GS} = 0V
		—	—	250		V _{DS} = 48V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -20V
Q _G	Total Gate Charge	—	—	88	nC	I _{D1} = 35A
Q _{GS}	Gate-to-Source Charge	—	—	15		V _{DS} = 30V
Q _{GD}	Gate-to-Drain ('Miller') Charge	—	—	52		V _{GS} = 10V
t _{d(on)}	Turn-On Delay Time	—	—	23	ns	V _{DD} = 30V
t _r	Rise Time	—	—	130		I _{D1} = 35A
t _{d(off)}	Turn-Off Delay Time	—	—	81		R _G = 9.1Ω
t _f	Fall Time	—	—	79		V _{GS} = 10V
L _S + L _D	Total Inductance	—	6.8	—	nH	Measured from Drain lead (6mm / 0.25 in from package) to Source lead (6mm/0.25 in from package) with Source wire internally bonded from Source pin to Drain pad
C _{iSS}	Input Capacitance	—	2400	—	pF	V _{GS} = 0V
C _{oSS}	Output Capacitance	—	1100	—		V _{DS} = 25V
C _{rSS}	Reverse Transfer Capacitance	—	230	—		f = 1.0MHz

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	35*	A	
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	180		
V _{SD}	Diode Forward Voltage	—	—	2.5	V	T _J = 25°C, I _S = 35A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	220	ns	T _J = 25°C, I _F = 35A, V _{DD} ≤ 50V
Q _{rr}	Reverse Recovery Charge	—	—	1.6	μC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

* Current is limited by package

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	—	1.0	°C/W
R _{θCS}	Case -to-Sink	—	0.21	—	
R _{θJA}	Junction-to-Ambient (Typical socket mount)	—	—	48	

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② V_{DD} = 25V, starting T_J = 25°C, L = 0.5mH, Peak I_L = 35A, V_{GS} = 10V
- ③ I_{SD} ≤ 35A, di/dt ≤ 100A/μs, V_{DD} ≤ 60V, T_J ≤ 150°C
- ④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%.

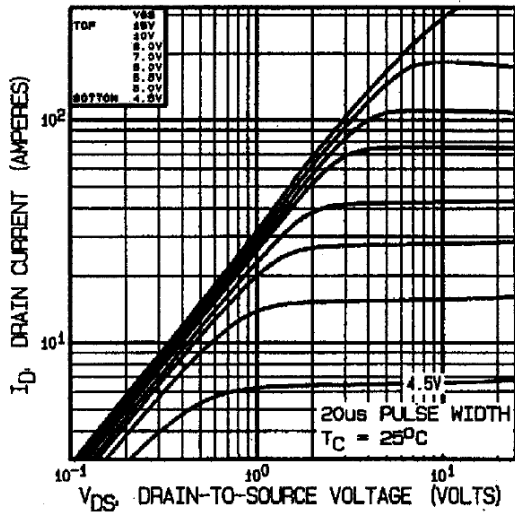


Fig 1. Typical Output Characteristics

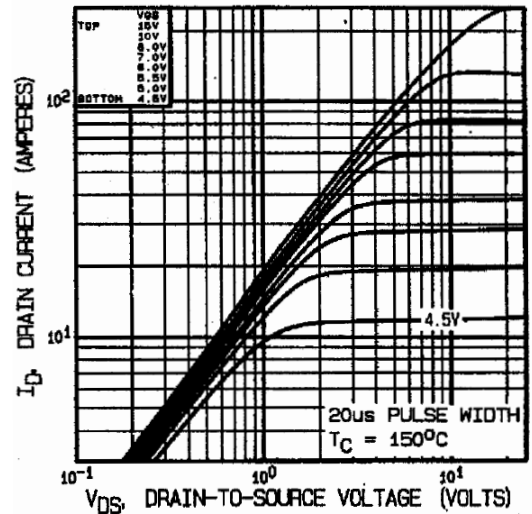


Fig 2. Typical Output Characteristics

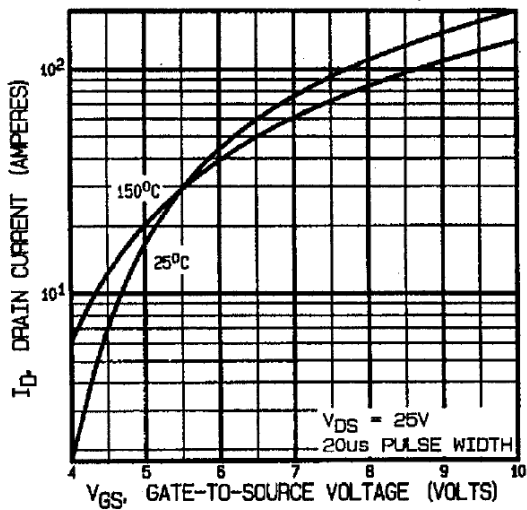


Fig 3. Typical Transfer Characteristics

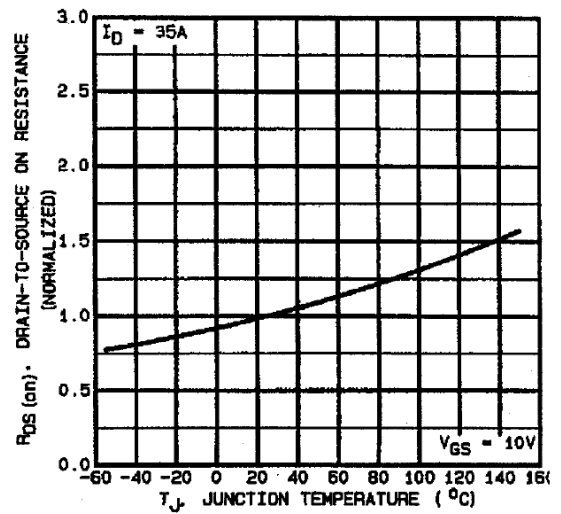


Fig 4. Normalized On-Resistance Vs. Temperature

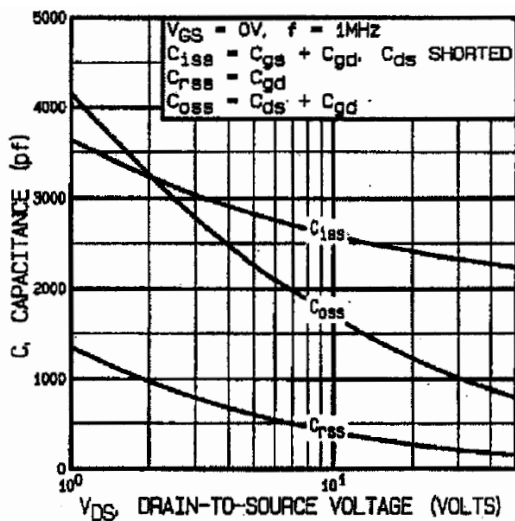


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

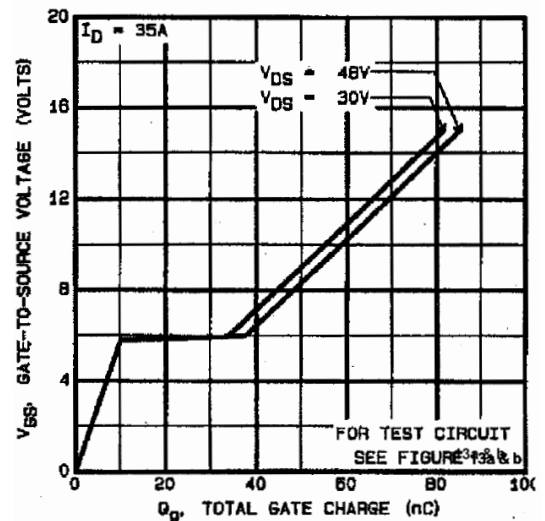


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

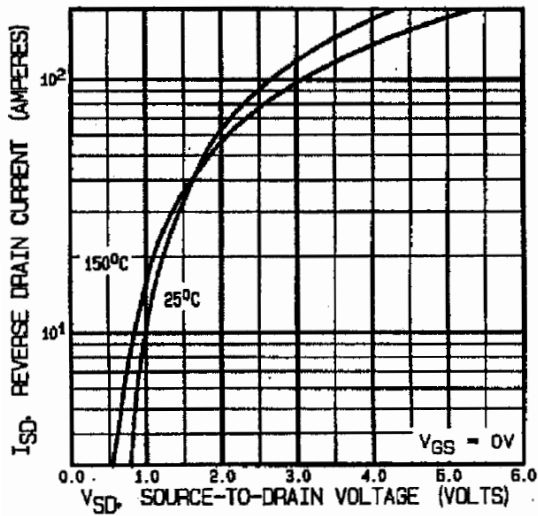


Fig 7. Typical Source-Drain Diode Forward Voltage

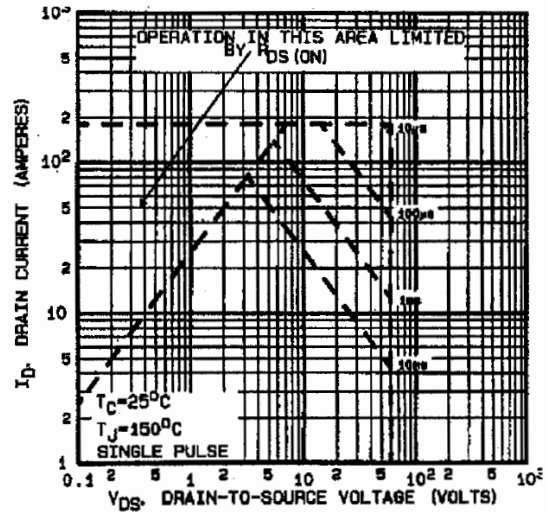


Fig 8. Maximum Safe Operating Area

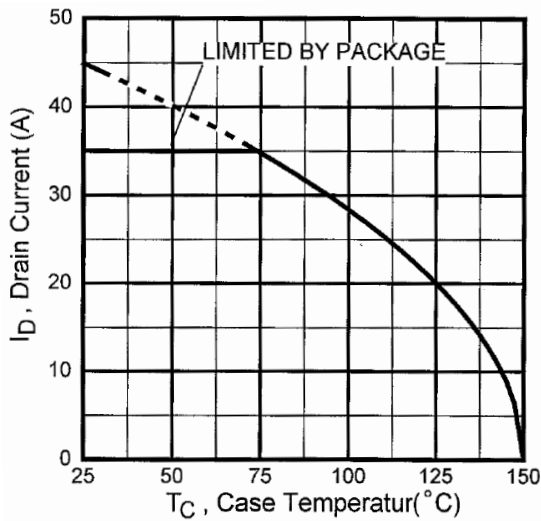


Fig 9. Maximum Drain Current Vs. Case Temperature

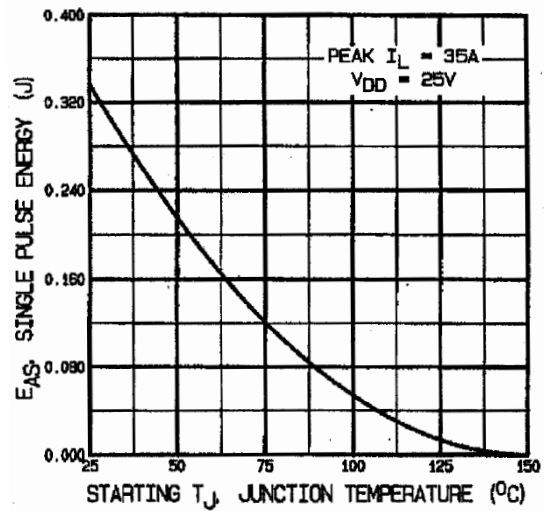


Fig 10. Maximum Avalanche Energy Vs. Drain Current

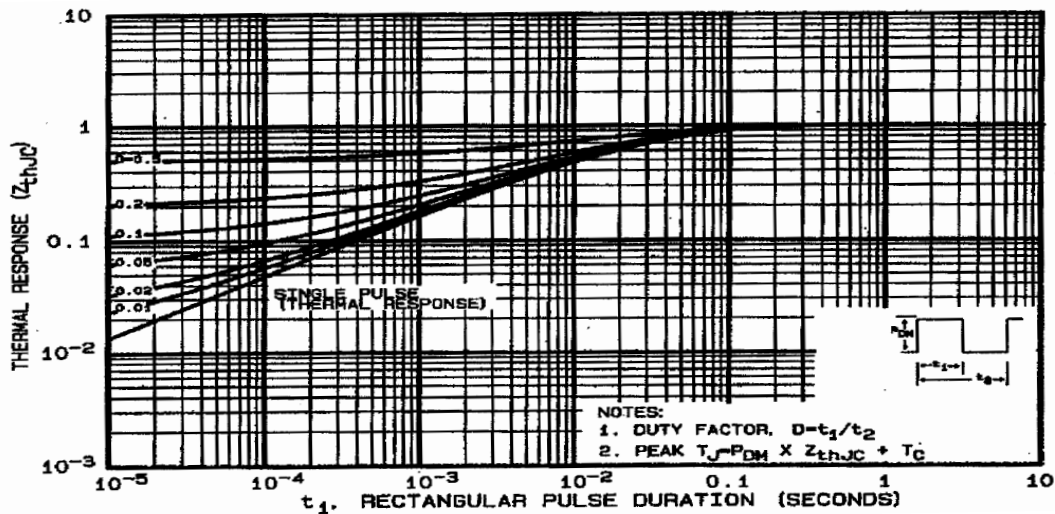


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

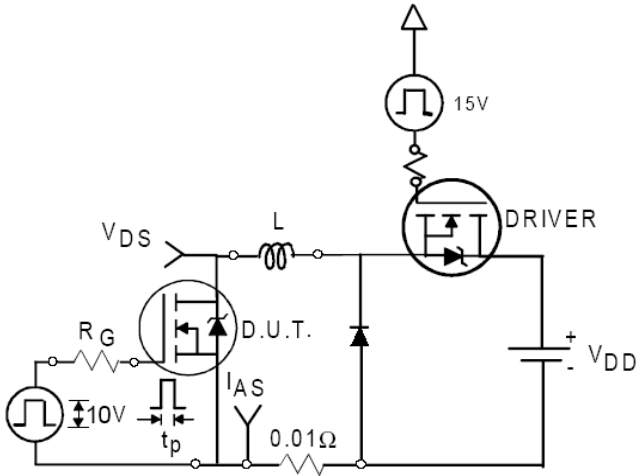


Fig 12a. Unclamped Inductive Test Circuit

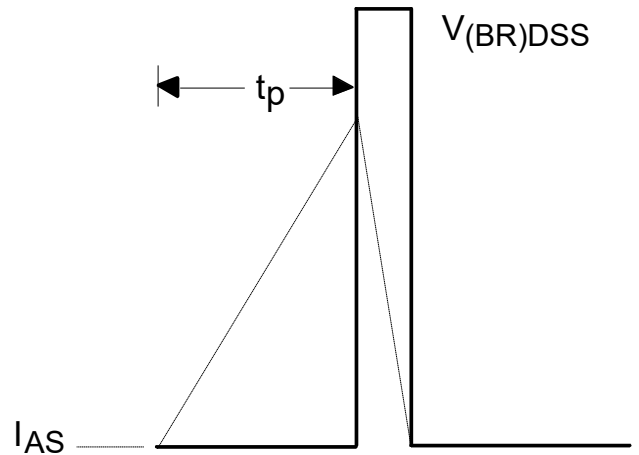


Fig 12b. Unclamped Inductive Waveforms

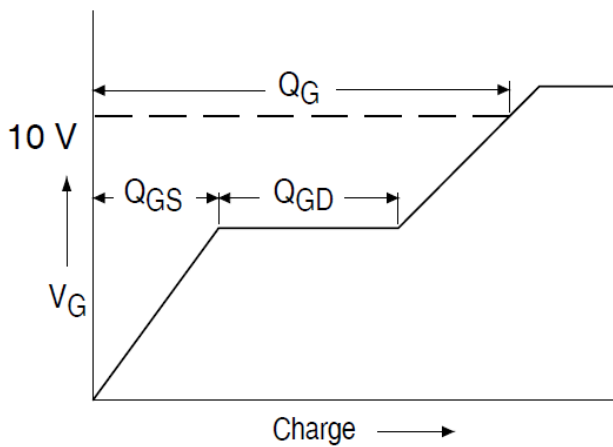


Fig 13a. Basic Gate Charge Waveform

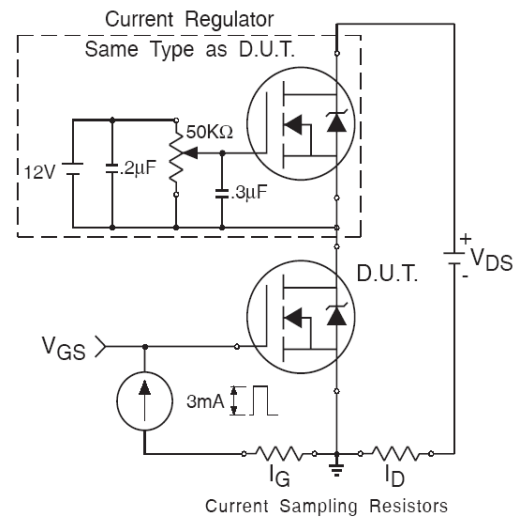


Fig 13b. Gate Charge Test Circuit

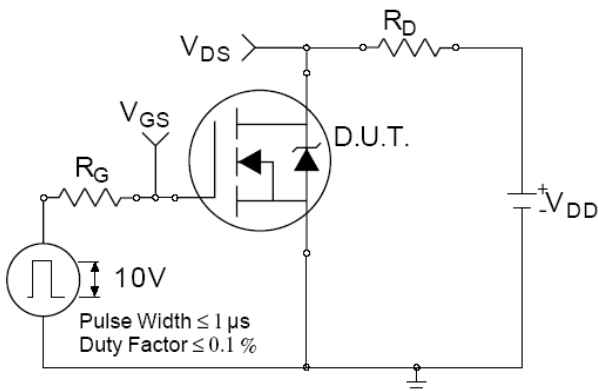


Fig 14a. Switching Time Test Circuit

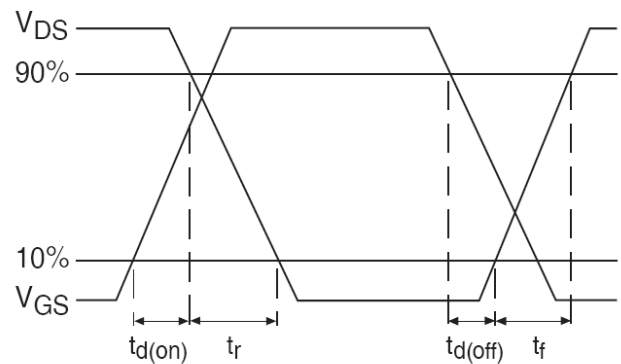
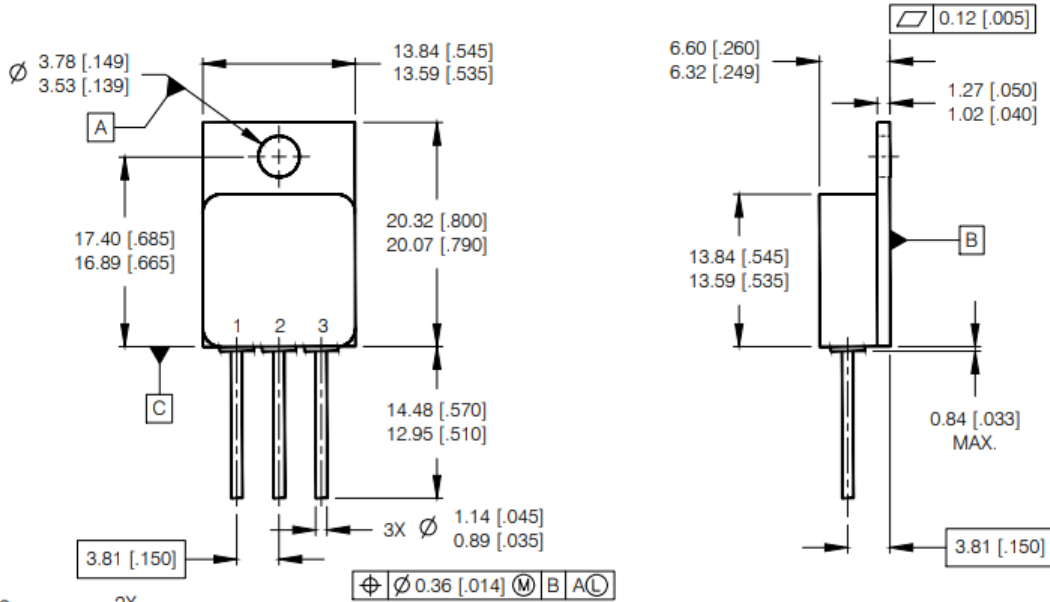


Fig 14b. Switching Time Waveforms

Note: For the most updated package outline, please see the website: TO-254AA

Case Outline and Dimensions - Low-Ohmic TO-254AA

REV.	DESCRIPTION	ECN	DATE
A	INITIAL RELEASE	1120_ER6904	4-3-20



- NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
 3. CONTROLLING DIMENSION: INCH.
 4. CONFORMS TO JEDEC OUTLINE TO-254AA.
 5. FINAL LEAD FINISH IS SOLDER ALLOY 63%Sn 37%Pb.
 6. STANDARD FINAL FINISH ON ALL TERMINALS IS SOLDER ALLOY 63%Sn 37%Pb.

PIN ASSIGNMENTS

- 1 = DRAIN
- 2 = SOURCE
- 3 = GATE



TITLE: TO-254AA PACKAGE OUTLINE (STD & LOW OHMIC)	
DRAWING NO. D100720G-WEB	REV A

BERYLLIA WARNING PER MIL-PRF-19500

Package containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.



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Data and specifications subject to change without notice.

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