PD-90493H

An Infineon Technologies Company

IRFM450
JANTX2N7228
JANTXV2N7228

POWER MOSFET
THRU-HOLE (TO-254AA)

500V, N-CHANNEL
REF: MIL-PRF-19500/592
HEXFET MOSFET TECHNOLOGY

Product Summary

Part Number	$R_{DS(on)}$	I_D
IRFM450	0.415Ω	12A

TO-254

Description

HEXFET MOSFET technology is the key to IR HiRel advanced line of power MOSFET transistors. The efficient geometry design achieves very low on-state resistance combined with high trans conductance. HEXFET transistors also feature all of the well-established advantages of MOSFETs, such as voltage control, very fast switching, ease of paralleling and electrical parameter temperature stability. They are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, high energy pulse circuits, and virtually any application where high reliability is required. The HEXFET transistor's totally isolated package eliminates the need for additional isolating material between the device and the heat sink. This improves thermal efficiency and reduces drain capacitance.

Features

- Simple Drive Requirements
- Hermetically Sealed
- Electrically Isolated
- Dynamic dv/dt Rating
- Light Weight
- ESD Rating: Class 3A per MIL-STD-750, Method 1020

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_{D1} @ V_{GS} = 10V, T_C = 25°C	Continuous Drain Current	12	A
I_{D2} @ V_{GS} = 10V, T_C = 100°C	Continuous Drain Current	8.0	
I_{DM} @T_C = 25°C	Pulsed Drain Current ①	48	
P_D @T_C = 25°C	Maximum Power Dissipation	150	W
	Linear Derating Factor	1.2	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	750	mJ
I_{AR}	Avalanche Current ①	12	A
E_{AR}	Repetitive Avalanche Energy ①	15	mJ
dv/dt	Peak Diode Recovery dv/dt ③	3.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (0.063 in. /1.6 mm from case for 10s)	
	Weight	9.3 (Typical)	g

For Footnotes refer to the page 2.

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	500	——	——	V	V_{GS} = 0V, I_D = 1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.68	——	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	——	——	0.415	Ω	V_{GS} = 10V, I_{D2} = 8.0A ④
		——	——	0.515		V_{GS} = 10V, I_{D1} = 12A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
Gfs	Forward Transconductance	6.5	——	——	S	V_{DS} = 15V, I_D = 8.0A ④
I_{DSS}	Zero Gate Voltage Drain Current	——	——	25	μA	V_{DS} = 400V, V_{GS} = 0V
		——	——	250		V_{DS} = 400V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Leakage Reverse	——	——	-100		V_{GS} = -20V
Q_G	Total Gate Charge	——	——	120	nC	I_{D1} = 12A
Q_{GS}	Gate-to-Source Charge	——	——	19		V_{DS} = 250V
Q_{GD}	Gate-to-Drain ('Miller') Charge	——	——	70		V_{GS} = 10V
$t_{d(on)}$	Turn-On Delay Time	——	——	35	ns	V_{DD} = 250V
tr	Rise Time	——	——	190		I_{D1} = 12A
$t_{d(off)}$	Turn-Off Delay Time	——	——	170		R_G = 2.35Ω
t_f	Fall Time	——	——	130		V_{GS} = 10V
Ls +L_D	Total Inductance	——	6.8	——	nH	Measured from Drain lead (6mm / 0.25 in from package) to Source lead (6mm/ 0.25 in from package) with Source wire internally bonded from Source pin to Drain pad
C_{iss}	Input Capacitance	——	2700	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	600	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	240	——		f = 1.0MHz

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	——	——	12	A	
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	48		
V_{SD}	Diode Forward Voltage	——	——	1.7	V	T_J = 25°C, I_S = 12A, V_{GS} = 0V④
t_{rr}	Reverse Recovery Time	——	——	1600	ns	T_J = 25°C, I_F = 12A, V_{DD} ≤ 50V
Q_{rr}	Reverse Recovery Charge	——	——	14	μC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	——	0.83	°C/W
$R_{\theta CS}$	Case -to-Sink	——	0.21	——	
$R_{\theta JA}$	Junction-to-Ambient (Typical socket mount)	——	——	48	

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} = 50V, starting T_J = 25°C, L = 10.4mH, Peak I_L = 12A, V_{GS} = 10V

③ I_{SD} ≤ 12A, di/dt ≤ 130A/μs, V_{DD} ≤ 500V, T_J ≤ 150°C

④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%.

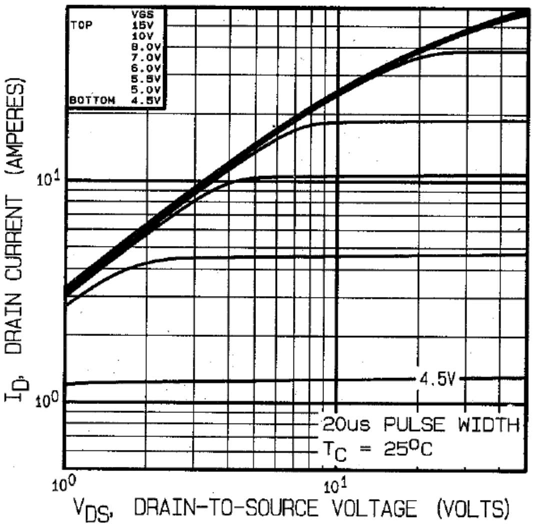


Fig 1. Typical Output Characteristics

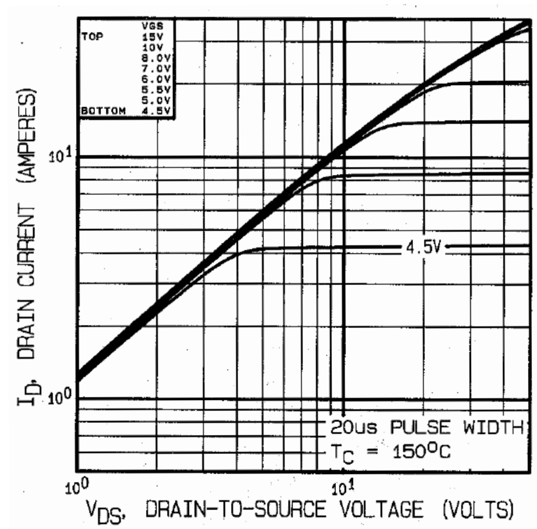


Fig 2. Typical Output Characteristics

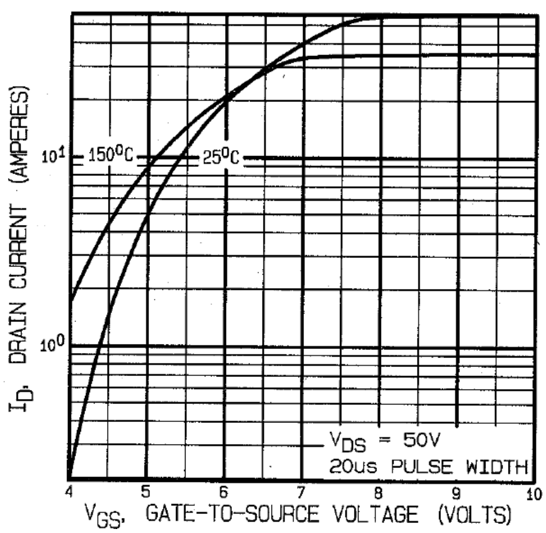


Fig 3. Typical Transfer Characteristics

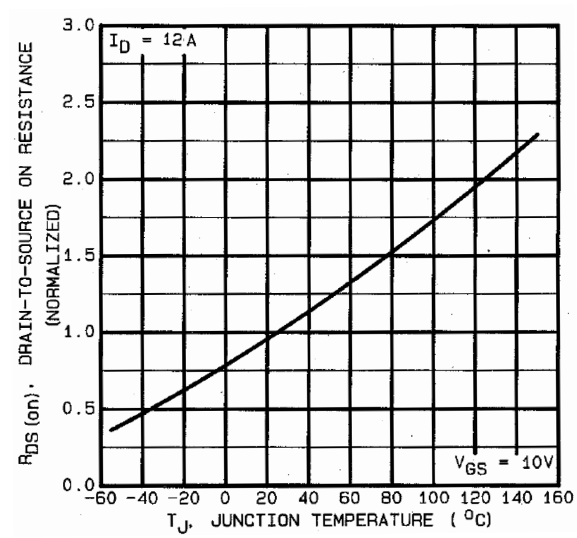


Fig 4. Normalized On-Resistance Vs. Temperature

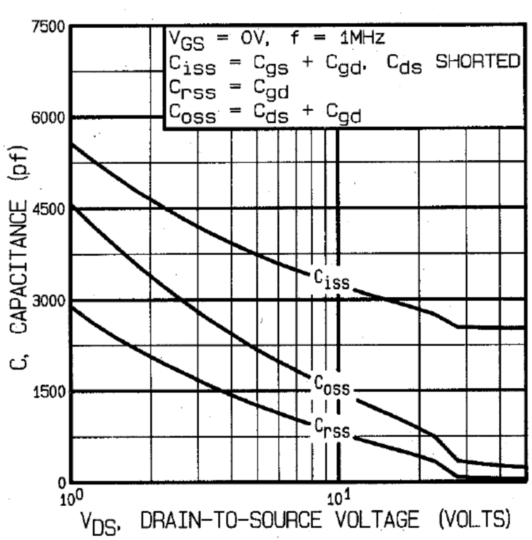


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

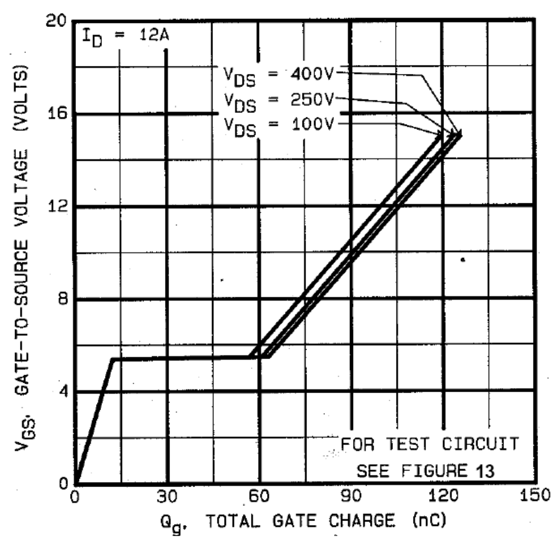


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

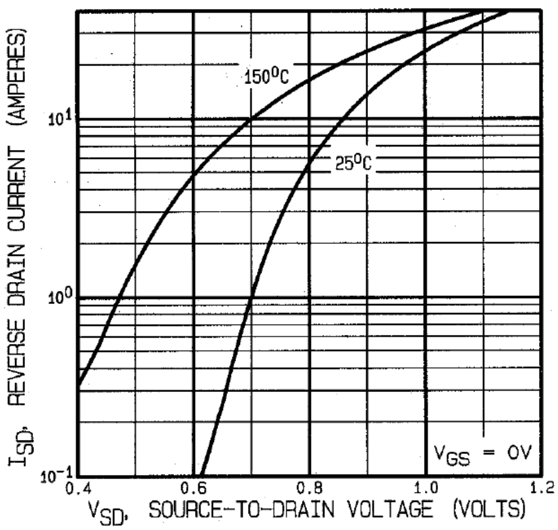


Fig 7. Typical Source-Drain Diode Forward Voltage

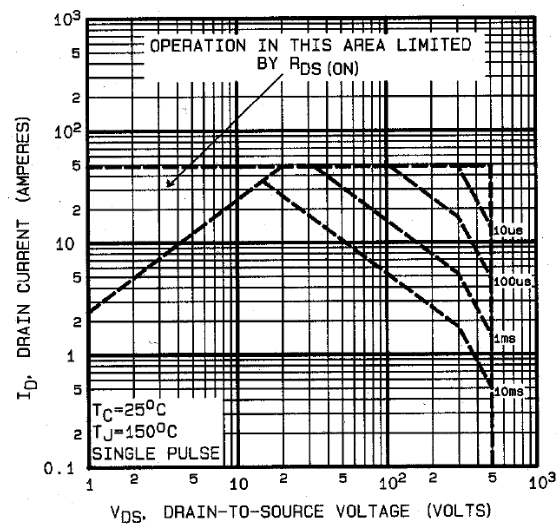


Fig 8. Maximum Safe Operating Area

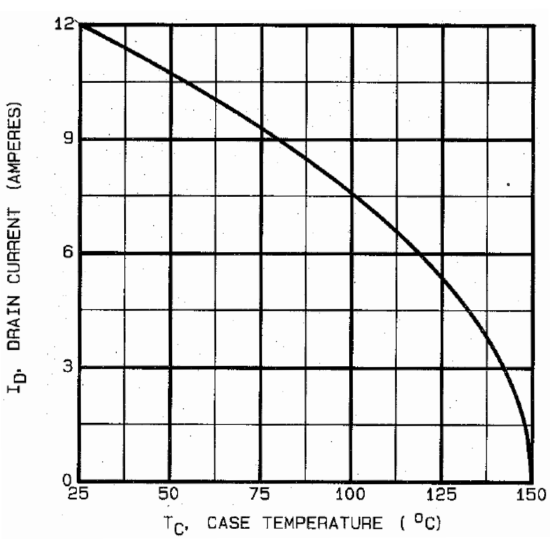


Fig 9. Maximum Drain Current Vs. Case Temperature

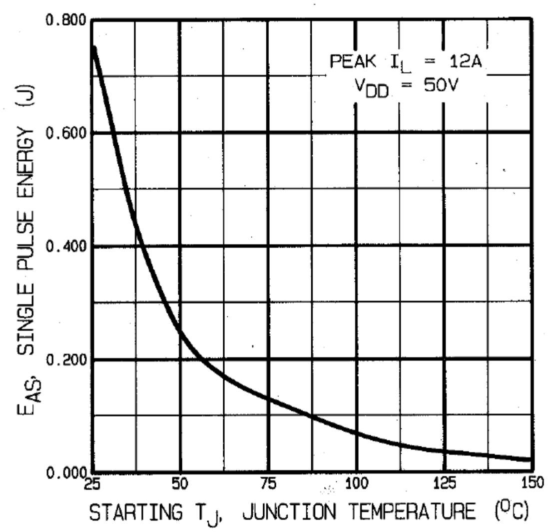


Fig 10. Maximum Avalanche Energy Vs. Drain Current

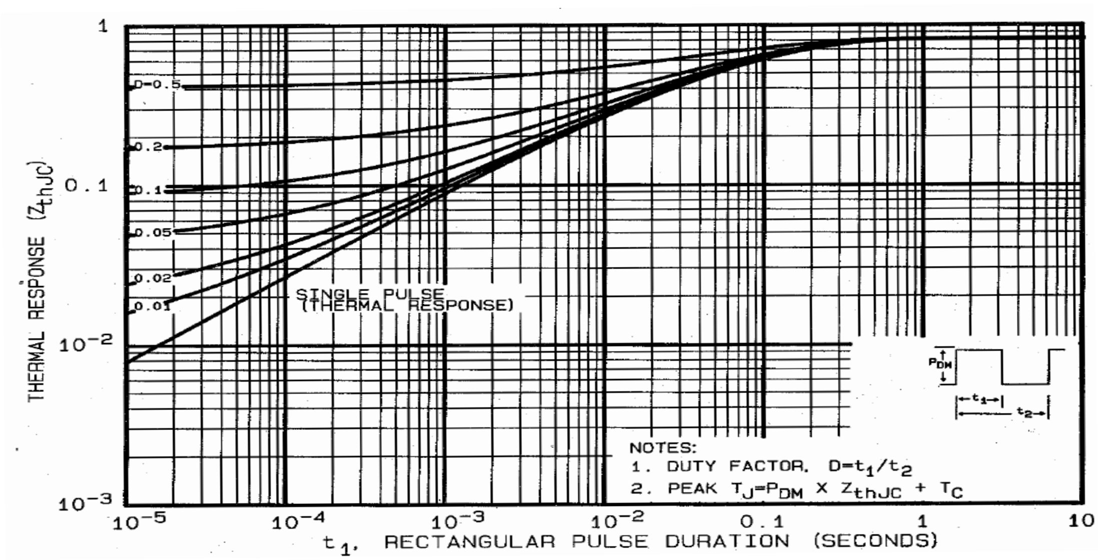


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

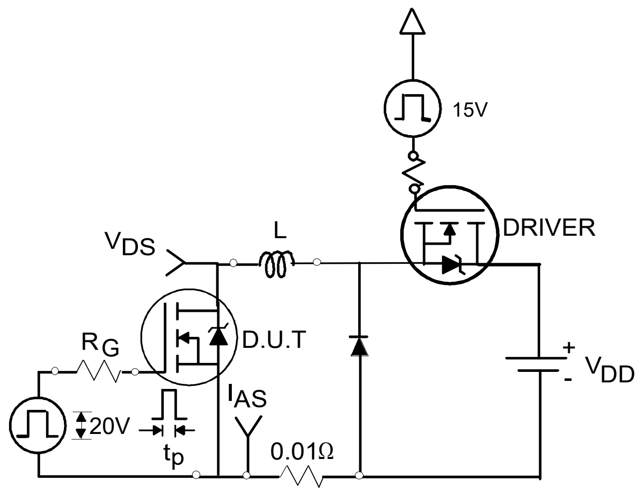


Fig 12a. Unclamped Inductive Test Circuit

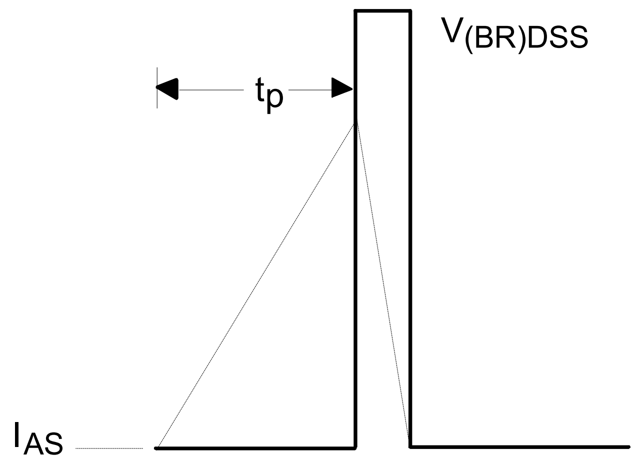


Fig 12b. Unclamped Inductive Waveforms

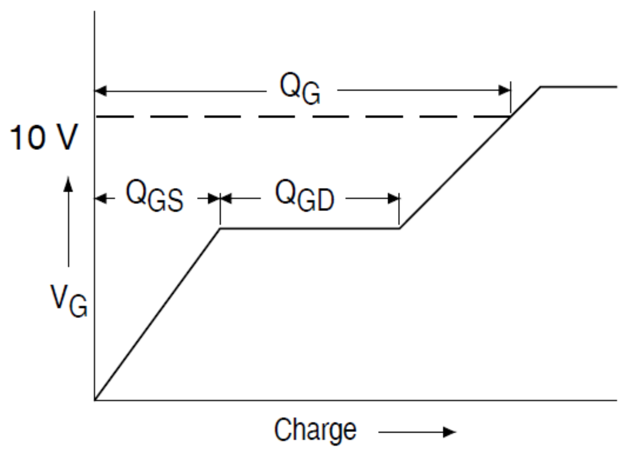


Fig 13a. Gate Charge Waveform

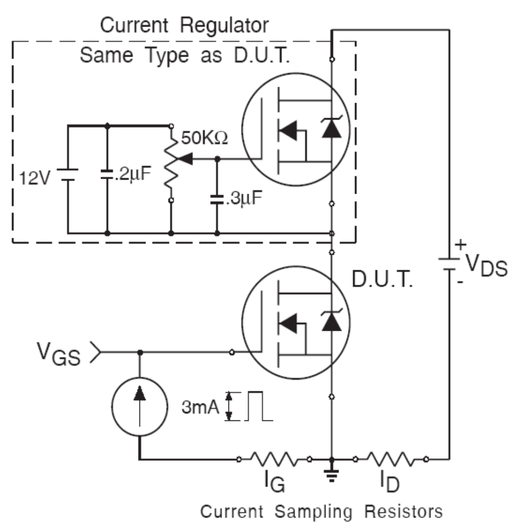


Fig 13b. Gate Charge Test Circuit

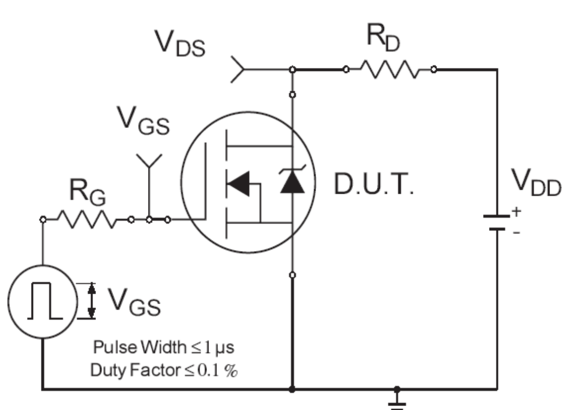


Fig 14a. Switching Time Test Circuit

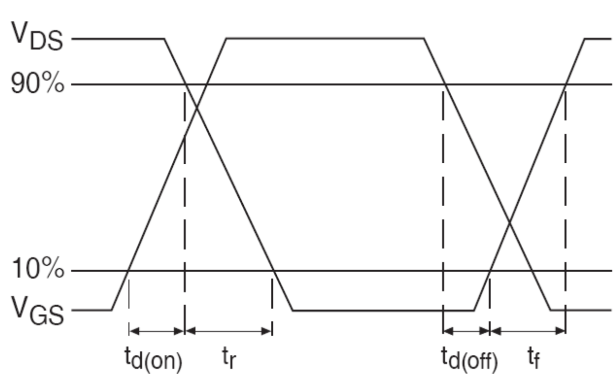
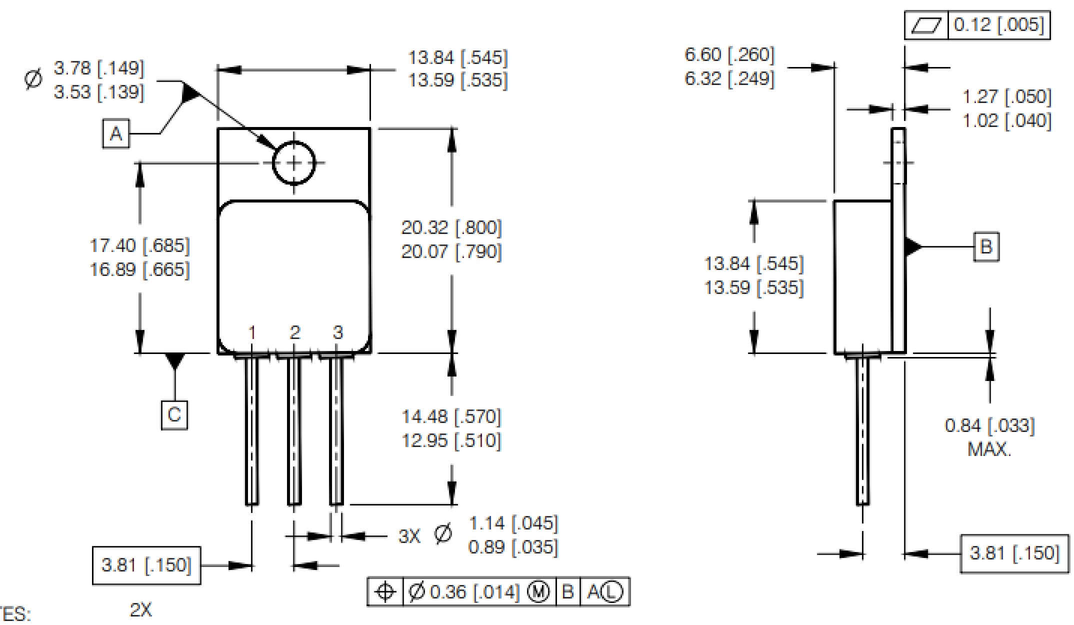


Fig 14b. Switching Time Waveforms

Note: For the most updated package outline, please see the website: TO-254AA

Case Outline and Dimensions - Low-Ohmic TO-254AA

REV.	DESCRIPTION	ECN	DATE
A	INITIAL RELEASE	1120_ER6904	4-3-20



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE TO-254AA.
5. FINAL LEAD FINISH IS SOLDER ALLOY 63%Sn 37%Pb.
6. STANDARD FINAL FINISH ON ALL TERMINALS IS SOLDER ALLOY 63%Sn 37%Pb.

PIN ASSIGNMENTS
1 = DRAIN
2 = SOURCE
3 = GATE

IOR HiRel
An Infineon Technologies Company

TITLE: TO-254AA PACKAGE OUTLINE (STD & LOW OHMIC)
DRAWING NO. D100720G-WEB
REV A

BERYLLIA WARNING PER MIL-PRF-19500

Package containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

IOR HiRel
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Data and specifications subject to change without notice.

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