

# MOSFET – Power, Single, N-Channel, $\mu$ 8FL

**30 V, 4.2 m $\Omega$ , 71 A**

## NVTFS4C06N

### Features

- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- NVTFS4C06NWF – Wettable Flanks Product
- NVT Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

**MAXIMUM RATINGS** ( $T_J = 25^\circ\text{C}$  unless otherwise stated)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		$V_{DSS}$	30	V
Gate-to-Source Voltage		$V_{GS}$	$\pm 20$	V
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 4)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$	21
		$T_A = 100^\circ\text{C}$		15
Power Dissipation $R_{\theta JA}$ (Note 1, 2, 4)		$T_A = 25^\circ\text{C}$	$P_D$	3.1
		$T_A = 100^\circ\text{C}$		1.6
Continuous Drain Current $R_{\theta JC}$ (Note 1, 3, 4)		$T_A = 25^\circ\text{C}$	$I_D$	71
		$T_A = 100^\circ\text{C}$		50
Power Dissipation $R_{\theta JC}$ (Note 1, 3, 4)		$T_A = 25^\circ\text{C}$	$P_D$	37
		$T_A = 100^\circ\text{C}$		18
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	$I_{DM}$	367	A
Operating Junction and Storage Temperature		$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)		$I_S$	33	A
Single Pulse Drain-to-Source Avalanche Energy ( $T_J = 25^\circ\text{C}, I_L = 26 \text{ A}_{pk}, L = 0.1 \text{ mH}$ )		$E_{AS}$	34	mJ
Lead Temperature for Soldering Purposes (1/8" from Case for 10 s)		$T_L$	260	$^\circ\text{C}$

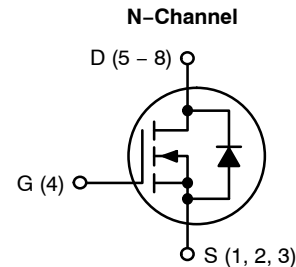
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS

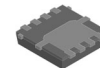
Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Drain) (Notes 1 and 4)	$R_{\theta JC}$	4.1	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Notes 1 and 2)	$R_{\theta JA}$	48	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup> 2 oz. Cu pad.
3. Assumes heat-sink sufficiently large to maintain constant case temperature independent of device power.
4. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
30 V	4.2 m $\Omega$ @ 10 V	71 A
	6.1 m $\Omega$ @ 4.5 V	

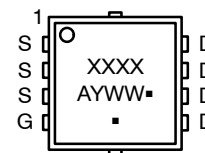


WDFN8 3.3x3.3, 0.65P  
CASE 511AB



WDFNW8 3.3x3.3, 0.65P (Full-Cut  $\mu$ 8FL WF)  
CASE 515AN

### MARKING DIAGRAM



- 4C06 = Specific Device Code for NVMTS4C06N  
 06WF = Specific Device Code of NVTFS4C06NWF  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

# NVTFS4C06N

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
<b>OFF CHARACTERISTICS</b>							
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30	-	-	V	
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$		-	14.4	-	mV/ $^\circ\text{C}$	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$	-	-	1.0	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$	-	-	10	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	-	-	$\pm 100$	nA	

## ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.3	-	2.2	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$		-	3.8	-	mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 30\text{ A}$	-	3.4	4.2	$\text{m}\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 30\text{ A}$	-	4.9	6.1	
Forward Transconductance	$g_{FS}$	$V_{DS} = 1.5\text{ V}, I_D = 15\text{ A}$	-	58	-	S
Gate Resistance	$R_G$	$T_A = 25^\circ\text{C}$	-	1.0	-	$\Omega$

## CHARGES AND CAPACITANCES

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 15\text{ V}$	-	1683	-	$\text{pF}$	
Output Capacitance	$C_{OSS}$		-	841	-		
Reverse Transfer Capacitance	$C_{RSS}$		-	40	-		
Capacitance Ratio	$C_{RSS}/C_{ISS}$	$V_{GS} = 0\text{ V}, V_{DS} = 15\text{ V}, f = 1\text{ MHz}$	-	0.023	-		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}; I_D = 30\text{ A}$	-	11.6	-	$\text{nC}$	
Threshold Gate Charge	$Q_{G(TH)}$		-	2.6	-		
Gate-to-Source Charge	$Q_{GS}$		-	4.7	-		
Gate-to-Drain Charge	$Q_{GD}$		-	4.0	-		
Gate Plateau Voltage	$V_{GP}$		-	3.1	-		V
Total Gate Charge	$Q_{G(TOT)}$		$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}; I_D = 30\text{ A}$	-	26		-

## SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$	-	10	-	ns
Rise Time	$t_r$		-	32	-	
Turn-Off Delay Time	$t_{d(OFF)}$		-	18	-	
Fall Time	$t_f$		-	5.0	-	
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$	-	8.0	-	ns
Rise Time	$t_r$		-	28	-	
Turn-Off Delay Time	$t_{d(OFF)}$		-	24	-	
Fall Time	$t_f$		-	3.0	-	

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 10\text{ A}$	$T_J = 25^\circ\text{C}$	-	0.8	1.1	V
			$T_J = 125^\circ\text{C}$	-	0.63	-	
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 30\text{ A}$	-	34	-	ns	
Charge Time	$t_a$		-	17	-		
Discharge Time	$t_b$		-	17	-		
Reverse Recovery Charge	$Q_{RR}$		-	22	-		$\text{nC}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

6. Switching characteristics are independent of operating junction temperatures.

# NVTFS4C06N

## TYPICAL CHARACTERISTICS

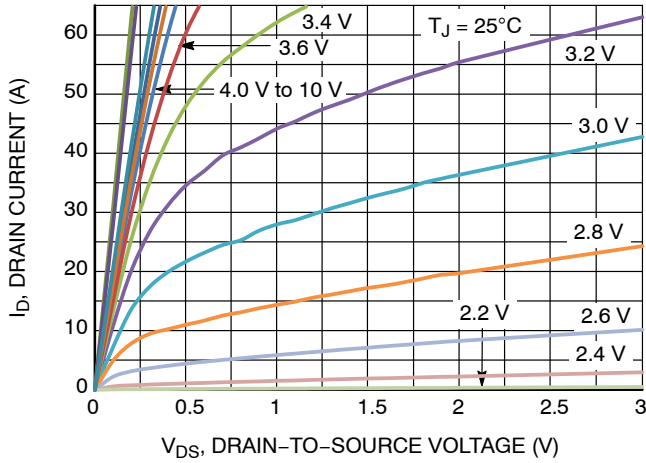


Figure 1. On-Region Characteristics

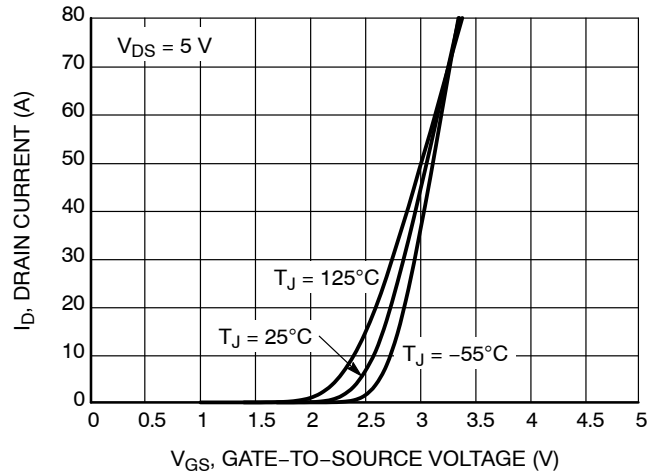


Figure 2. Transfer Characteristics

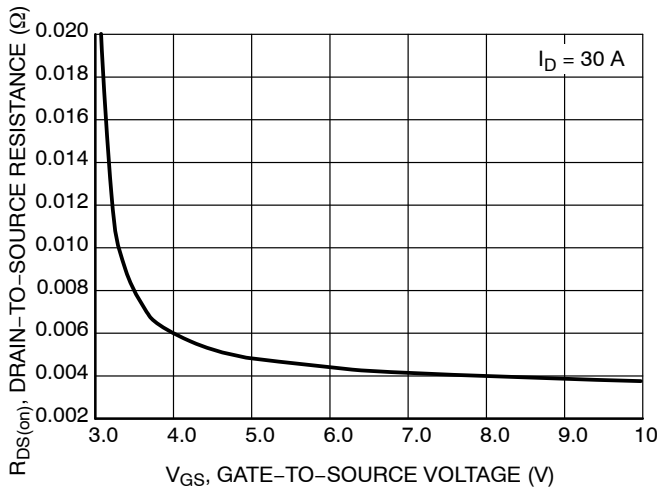


Figure 3. On-Resistance vs.  $V_{GS}$

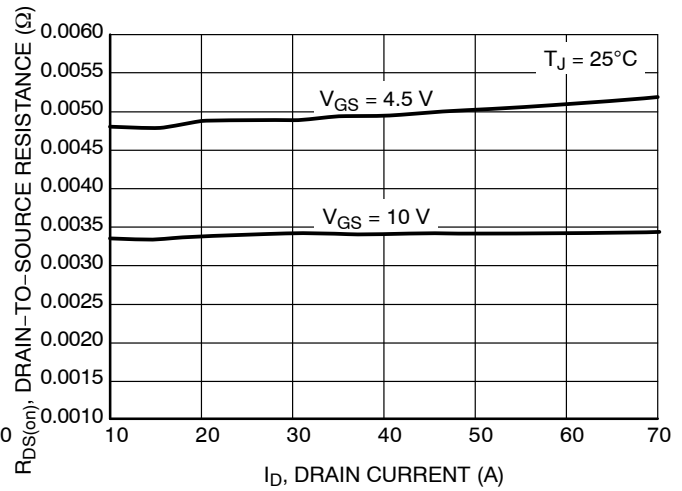


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

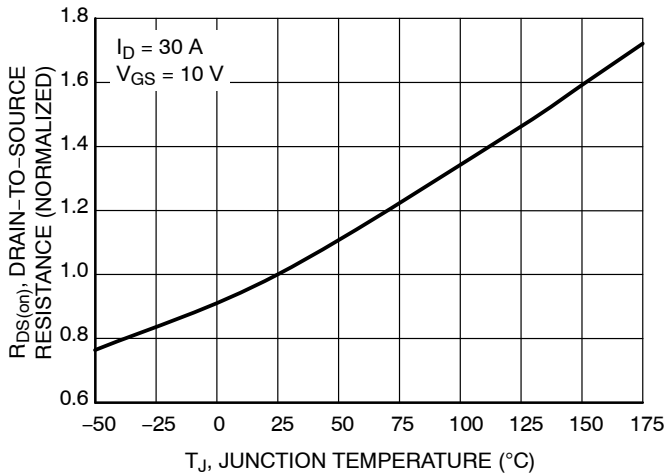


Figure 5. On-Resistance Variation with Temperature

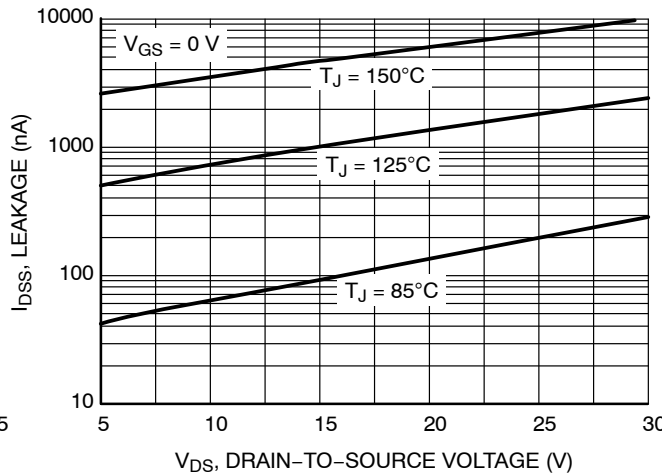


Figure 6. Drain-to-Source Leakage Current vs. Voltage

# NVTFS4C06N

## TYPICAL CHARACTERISTICS

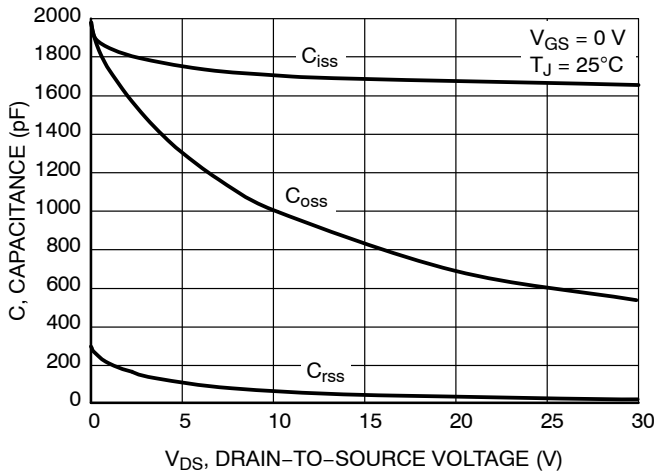


Figure 7. Capacitance Variation

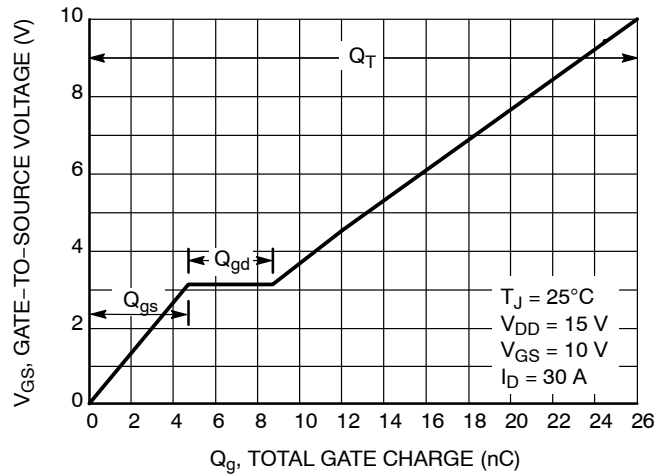


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

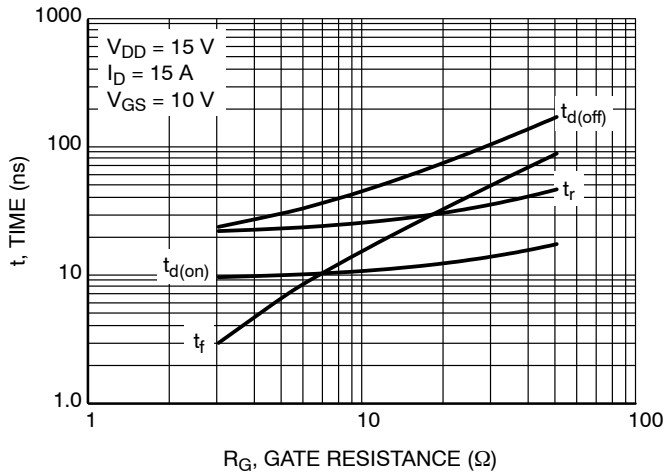


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

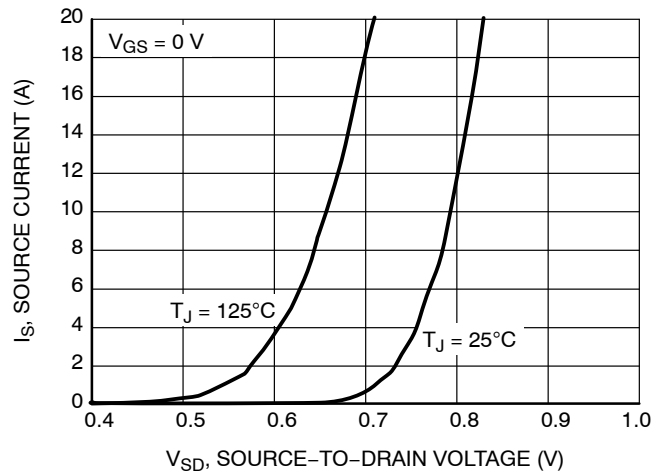


Figure 10. Diode Forward Voltage vs. Current

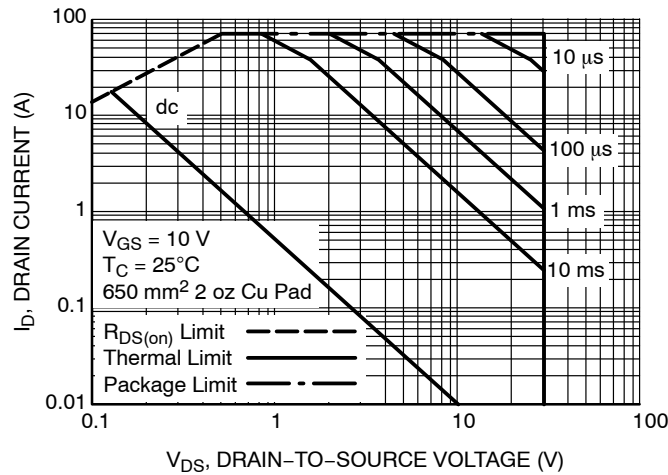


Figure 11. Maximum Rated Forward Biased Safe Operating Area

# NVTFS4C06N

## TYPICAL CHARACTERISTICS

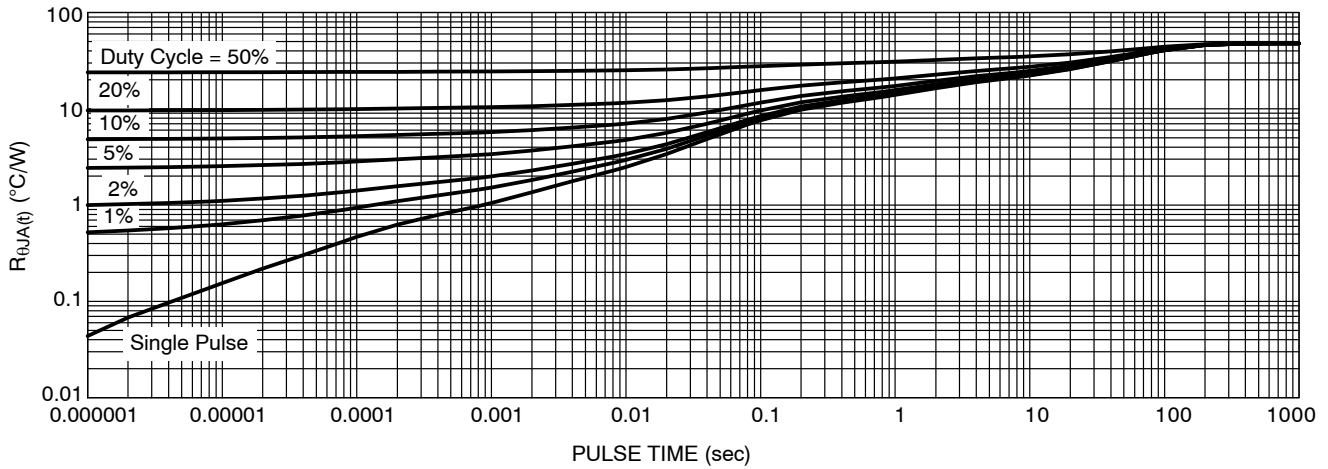


Figure 12. Thermal Response

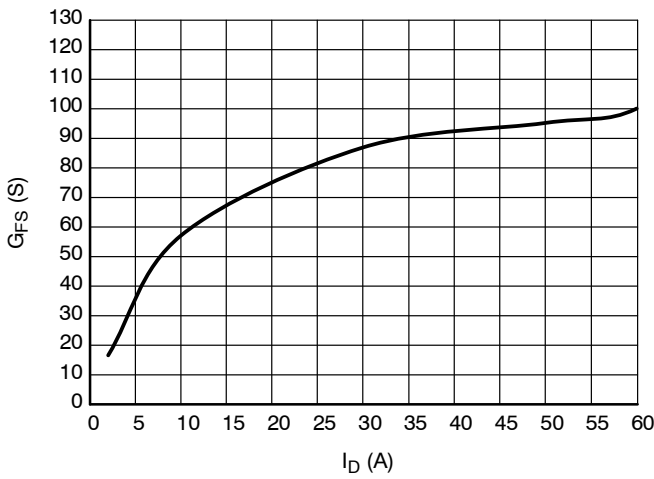


Figure 13.  $G_{FS}$  vs.  $I_D$

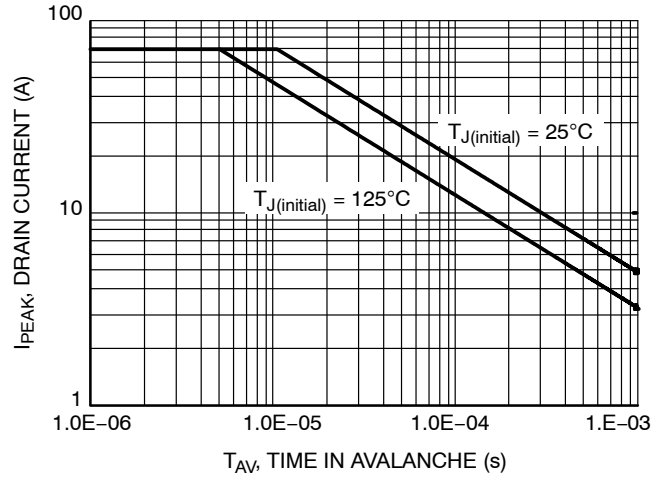


Figure 14. Avalanche Characteristics

### ORDERING INFORMATION

Device	Package	Shipping†
NVTFS4C06NTAG	WDFN8 3.3x3.3, 0.65P (Pb-Free)	1500 / Tape & Reel
NVTFS4C06NWFTAG	WDFNW8 3.3x3.3, 0.65P (Full-Cut $\mu$ 8FL WF) (Pb-Free)	1500 / Tape & Reel
NVTFS4C06NTWG	WDFN8 3.3x3.3, 0.65P (Pb-Free)	5000 / Tape & Reel
NVTFS4C06NWFTWG	WDFNW8 3.3x3.3, 0.65P (Full-Cut $\mu$ 8FL WF) (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

WDFN8 3.3x3.3, 0.65P  
CASE 511AB  
ISSUE D

DATE 23 APR 2012



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	---	0.05	0.000	---	0.002
b	0.23	0.30	0.40	0.009	0.012	0.016
c	0.15	0.20	0.25	0.006	0.008	0.010
D	3.30 BSC			0.130 BSC		
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
E	3.30 BSC			0.130 BSC		
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	0.23	0.30	0.40	0.009	0.012	0.016
e	0.65 BSC			0.026 BSC		
G	0.30	0.41	0.51	0.012	0.016	0.020
K	0.65	0.80	0.95	0.026	0.032	0.037
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
M	1.40	1.50	1.60	0.055	0.059	0.063
θ	0°	---	12°	0°	---	12°



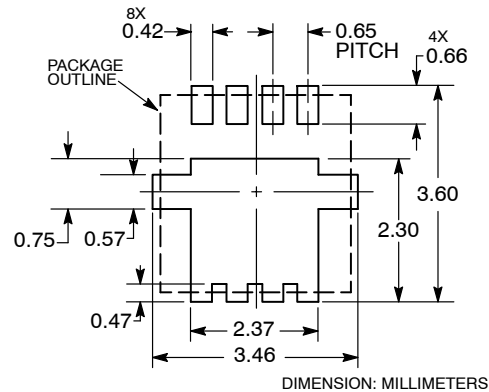
GENERIC MARKING DIAGRAM\*



- XXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	WDFN8 3.3X3.3, 0.65P	PAGE 1 OF 1

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# MECHANICAL CASE OUTLINE

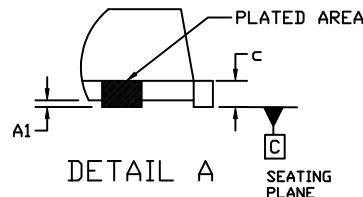
## PACKAGE DIMENSIONS

ON Semiconductor®



### WDFNW8 3.3x3.3, 0.65P (Full-Cut $\mu$ 8FL WF) CASE 515AN ISSUE O

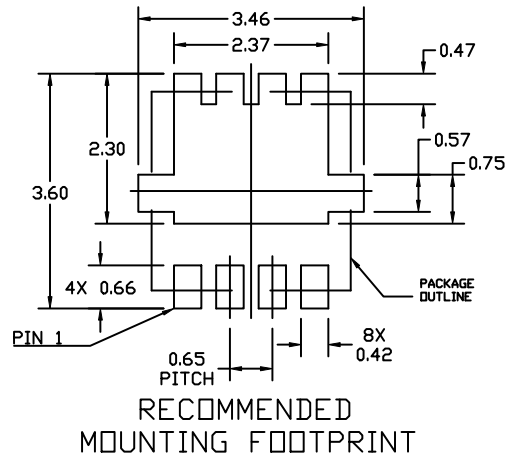
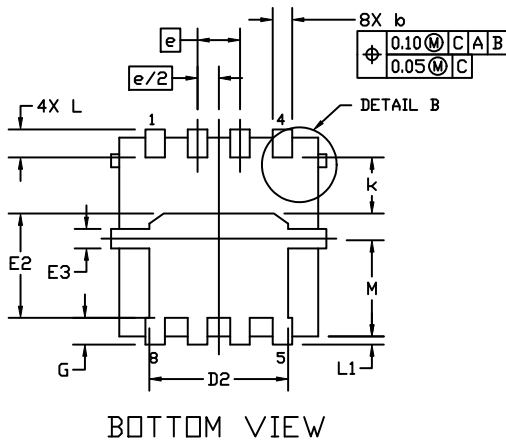
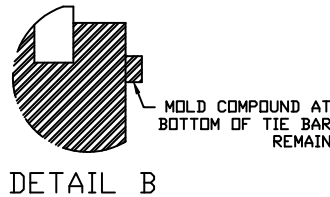
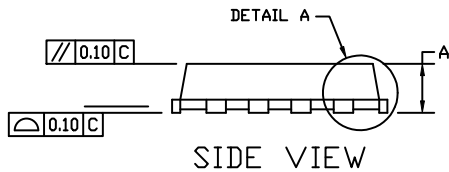
DATE 25 AUG 2020



NOTES:

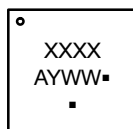
1. DIMENSIONING AND TOLERANCING PER: ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS		
	MIN.	NDM.	MAX.
A	0.70	0.75	0.80
A1	0.00	----	0.05
b	0.23	0.30	0.40
c	0.15	0.20	0.25
D	3.05	3.30	3.55
D1	2.95	3.05	3.15
D2	1.98	2.11	2.24
E	3.05	3.30	3.55
E1	2.95	3.05	3.15
E2	1.47	1.60	1.73
E3	0.23	0.30	0.40
e	0.65 BSC		
G	0.30	0.41	0.51
K	0.65	0.80	0.95
L	0.30	0.43	0.59
L1	0.06	0.13	0.20
M	1.40	1.50	1.60



\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



XXXX = Specific Device Code  
 A = Assembly Location  
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 WW = Work Week  
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\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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