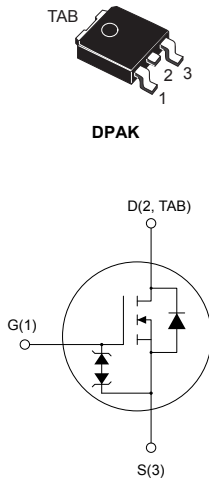


## N-channel 800 V, 2.8 $\Omega$ typ., 2.5 A MDmesh K5 Power MOSFET in a DPAK package



AM01476v1\_tab



### Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$
STD3N80K5	800 V	3.5 $\Omega$	2.5 A

- Industry's lowest  $R_{DS(on)}$  x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

#### Product status link

[STD3N80K5](#)

#### Product summary

<b>Order code</b>	STD3N80K5
<b>Marking</b>	3N80K5
<b>Package</b>	DPAK
<b>Packing</b>	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	2.5	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	1.6	
$I_{DM}^{(1)}$	Drain current (pulsed)	10	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	60	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	V/ns
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating junction temperature range		$^\circ\text{C}$

1. Pulse width is limited by safe operating area.
2.  $I_{SD} \leq 2.5\text{ A}$ ,  $di/dt \leq 100\text{ A}/\mu\text{s}$ ,  $V_{DS} (\text{peak}) \leq V_{(BR)DSS}$ .
3.  $V_{DS} \leq 640\text{ V}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance, junction-to-case	2.08	$^\circ\text{C}/\text{W}$
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	50	$^\circ\text{C}/\text{W}$

1. When mounted on 1 inch<sup>2</sup> FR-4, 2 Oz copper board.

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or non-repetitive (pulse width limited by $T_J$ max.)	1	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	65	mJ

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified.

**Table 4. On/off-state**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	800			V
$I_{DSS}$	Zero gate voltage drain current	$V_{DS} = 800\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 800\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_C = 125\text{ °C}^{(1)}$			50	
$I_{GSS}$	Gate body leakage current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 1\text{ A}$		2.8	3.5	$\Omega$

1. Specified by design, not tested in production.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	130	-	pF
$C_{oss}$	Output capacitance		-	14	-	pF
$C_{rss}$	Reverse transfer capacitance		-	0.6	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0\text{ V}$ , $V_{DS} = 0\text{ to }640\text{ V}$	-	20	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	9	-	pF
$R_g$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	15.5	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 640\text{ V}$ , $I_D = 2.5\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	9.5	-	nC
$Q_{gs}$	Gate-source charge		-	1.5	-	nC
$Q_{gd}$	Gate-drain charge		-	7.5	-	nC

1.  $C_{o(tr)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

2.  $C_{o(er)}$  is a constant capacitance value that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

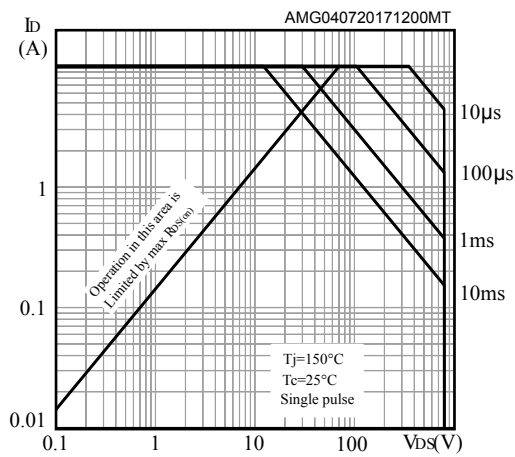
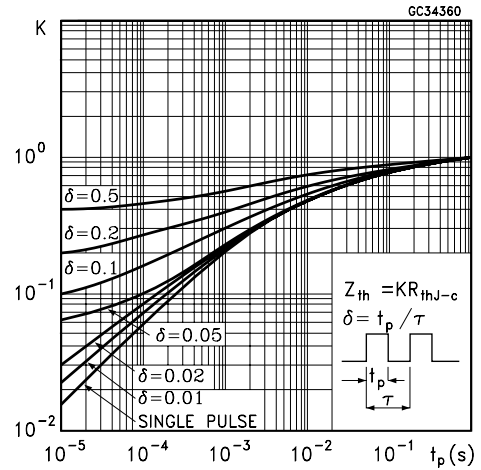
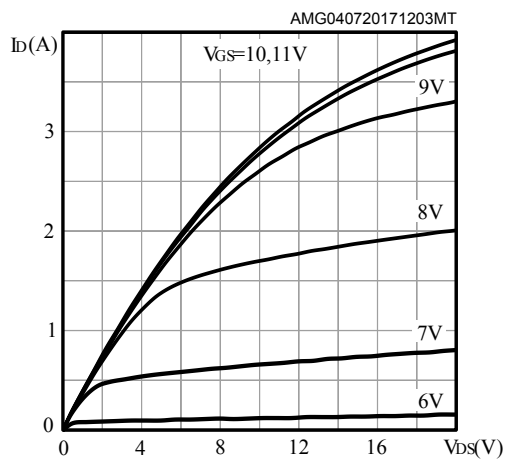
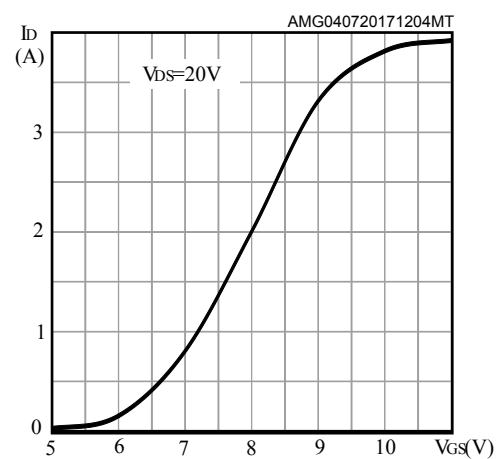
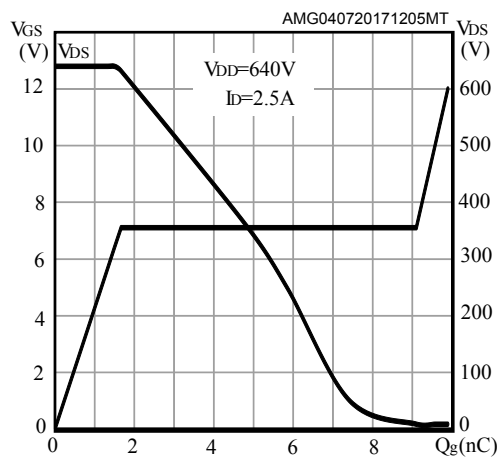
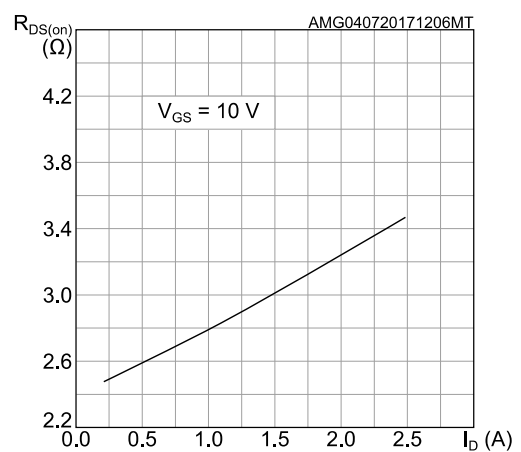
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$ , $I_D = 1.25\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	8.5	-	ns
$t_r$	Rise time		-	10.5	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	20.5	-	ns
$t_f$	Fall time		-	25	-	ns

**Table 7. Source-drain diode**

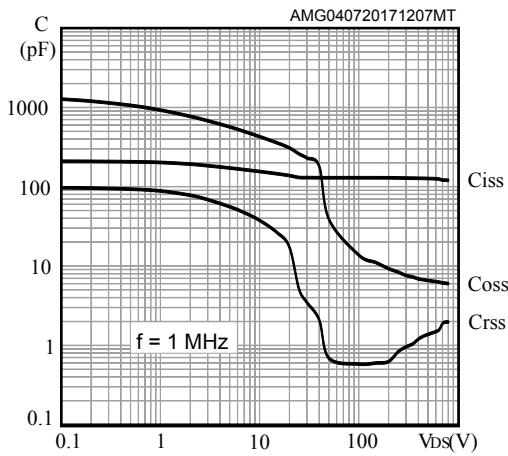
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		2.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		10	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 2.5 \text{ A}, V_{GS} = 0 \text{ V}$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 2.5 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s},$	-	265		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60 \text{ V}$	-	1.2		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	9.2		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 2.5 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s},$	-	430		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60 \text{ V}, T_J = 150 \text{ }^\circ\text{C}$	-	1.9		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	8.8		A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

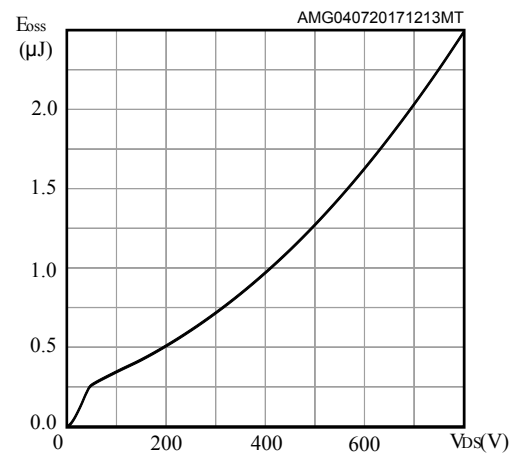
## 2.1 Electrical characteristics (curves)

**Figure 1. Safe operating area**

**Figure 2. Normalized transient thermal impedance**

**Figure 3. Typical output characteristics**

**Figure 4. Typical transfer characteristics**

**Figure 5. Typical gate charge characteristics**

**Figure 6. Typical drain-source on-resistance**


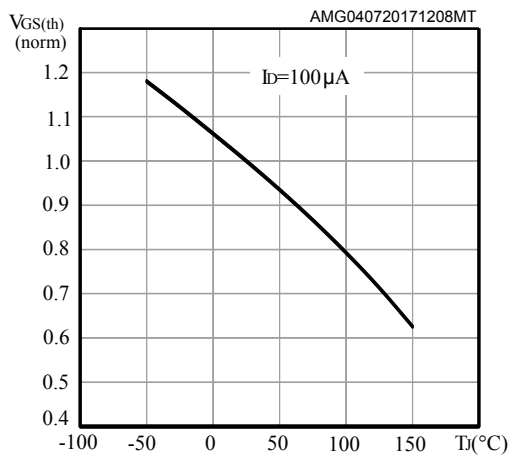
**Figure 7. Typical capacitance characteristics**



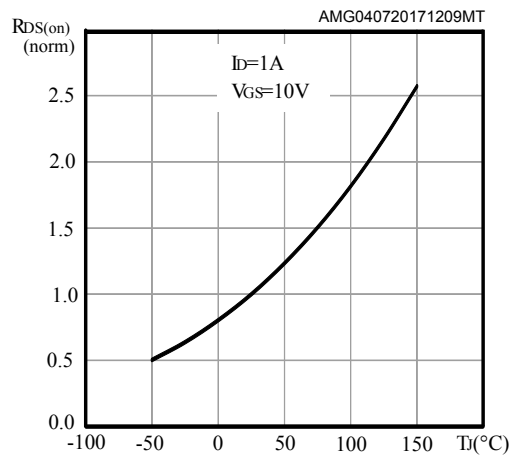
**Figure 8. Output capacitance stored energy**



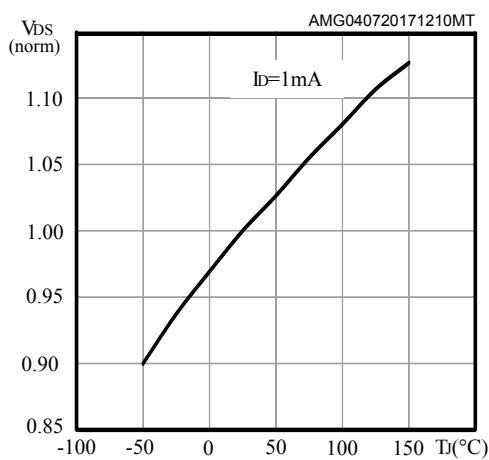
**Figure 9. Normalized gate threshold vs temperature**



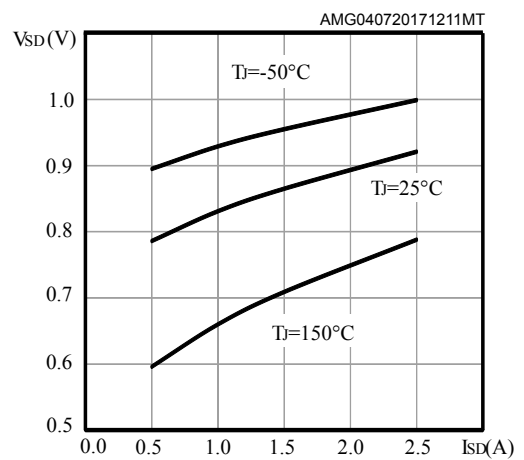
**Figure 10. Normalized on-resistance vs temperature**



**Figure 11. Normalized breakdown voltage vs temperature**



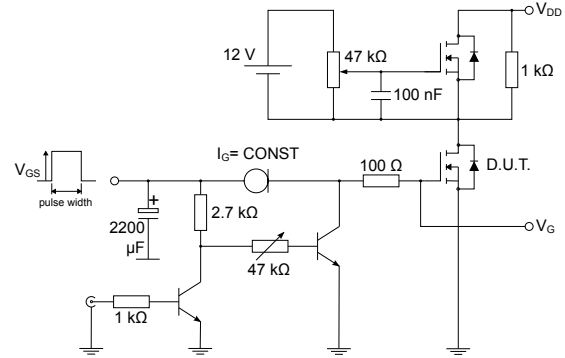
**Figure 12. Typical reverse diode forward characteristics**



### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**


AM01468v1

**Figure 14. Test circuit for gate charge behavior**


AM01469v1

**Figure 15. Test circuit for inductive load switching and diode recovery times**


AM01470v1

**Figure 16. Unclamped inductive load test circuit**


AM01471v1

**Figure 17. Unclamped inductive waveform**


AM01472v1

**Figure 18. Switching time waveform**

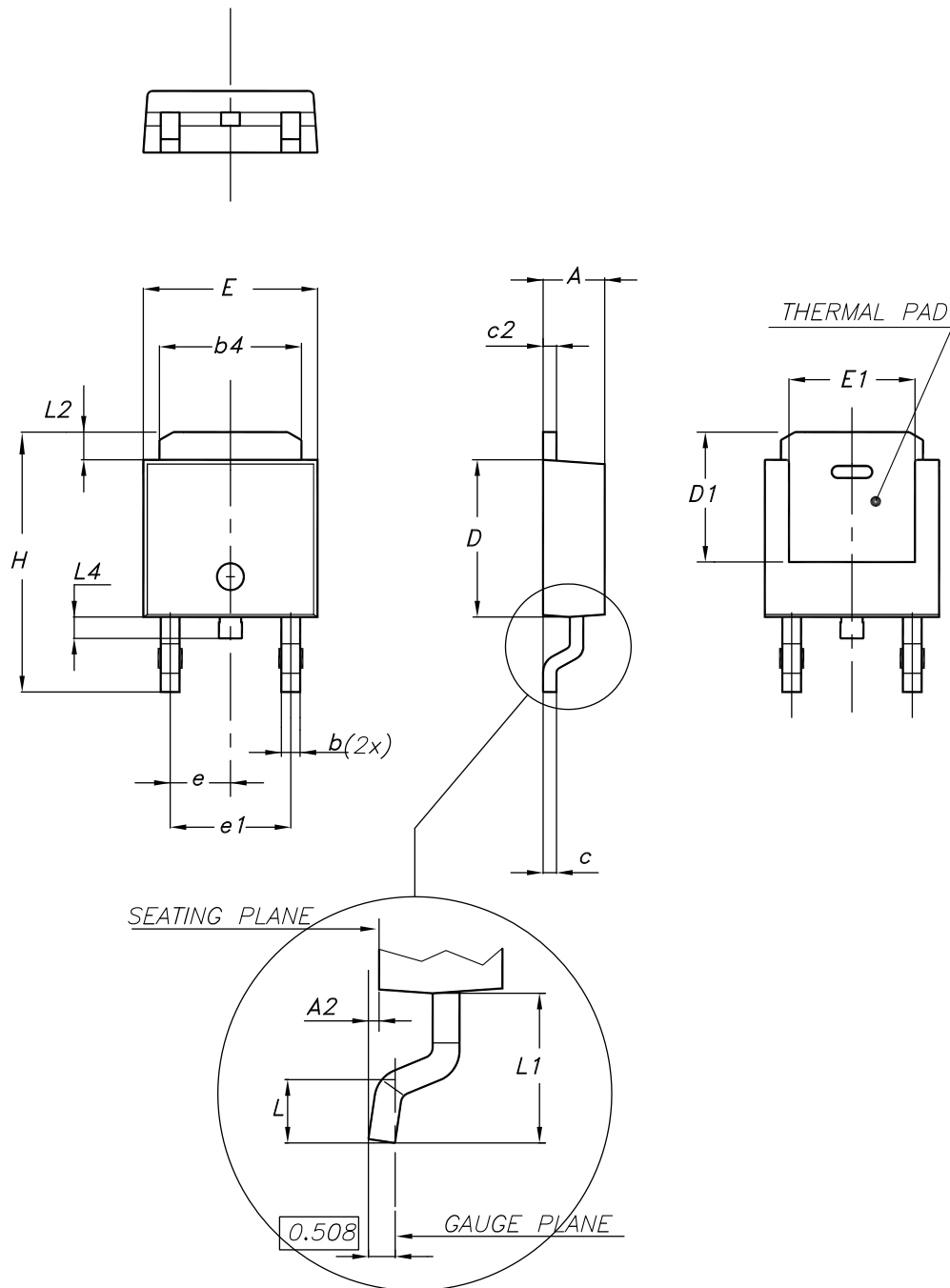

AM01473v1

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 DPAK (TO-252) type E package information

Figure 19. DPAK (TO-252) type E package outline



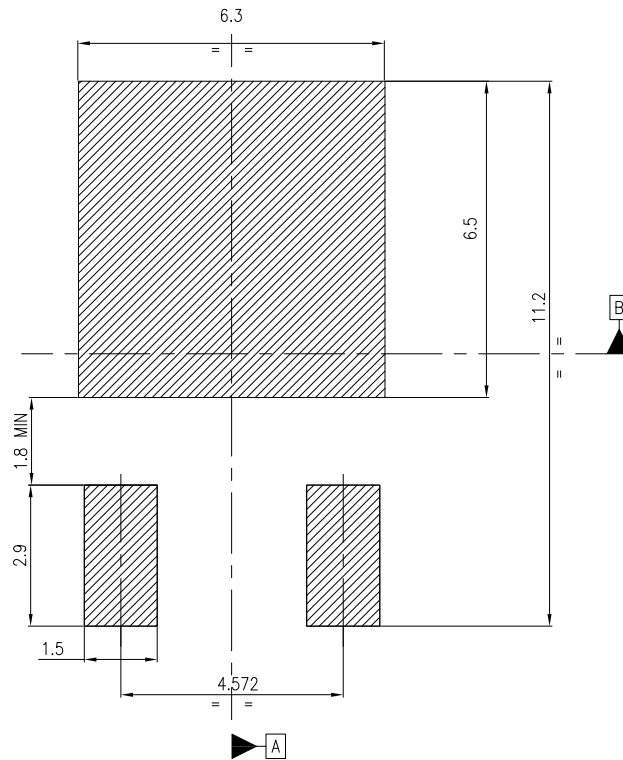
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**Table 8. DPAK (TO-252) type E mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.18		2.39
A2			0.13
b	0.65		0.884
b4	4.95		5.46
c	0.46		0.61
c2	0.46		0.60
D	5.97		6.22
D1	5.21		
E	6.35		6.73
E1	4.32		
e		2.286	
e1		4.572	
H	9.94		10.34
L	1.50		1.78
L1		2.74	
L2	0.89		1.27
L4			1.02

**Figure 20. DPAK (TO-252) recommended footprint (dimensions are in mm)**



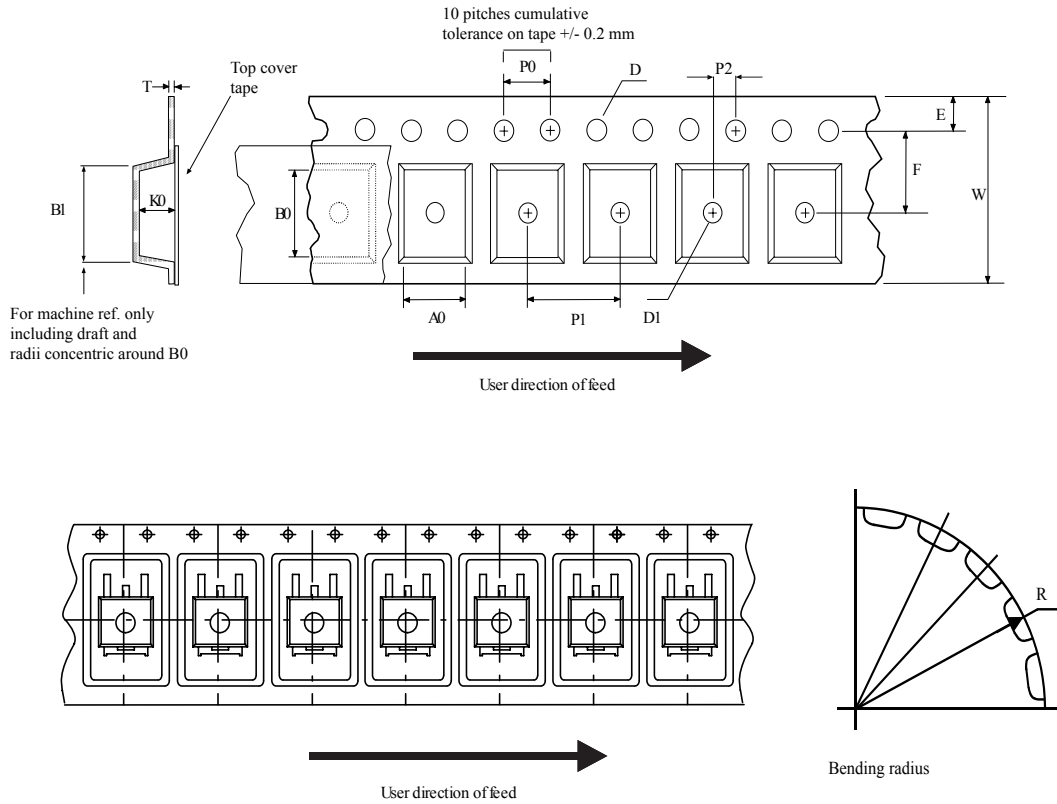
Notes:

- 1) This footprint is able to ensure insulation up to 630 Vrms (according to CEI IEC 664-1)
- 2) The device must be positioned within  $\oplus 0.05$  A B

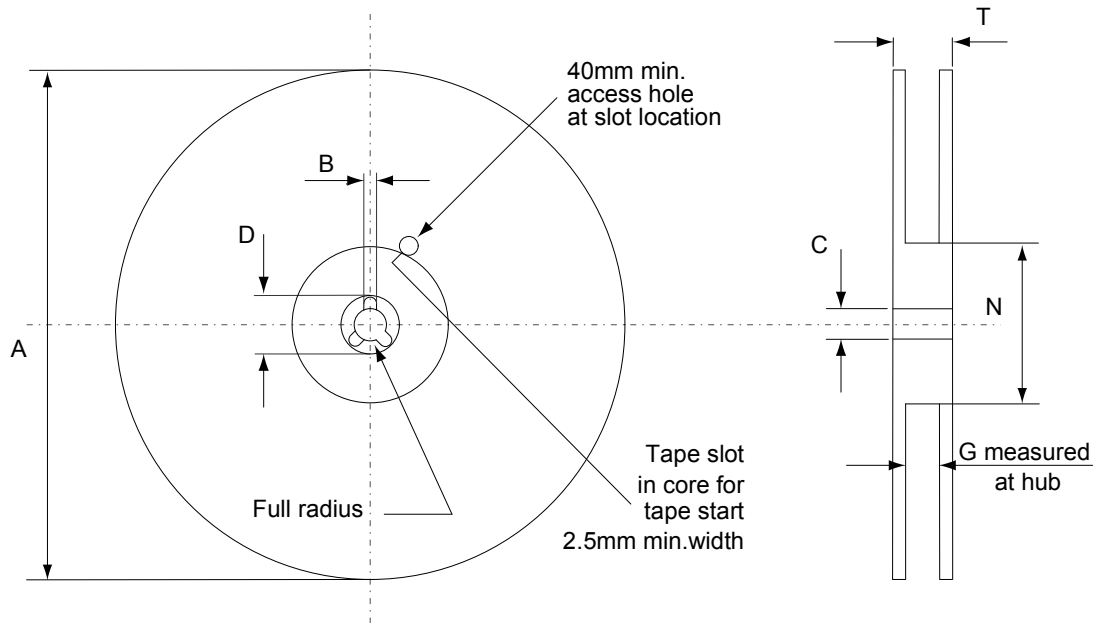
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## 4.2 DPAK (TO-252) packing information

Figure 21. DPAK (TO-252) tape outline



AM08852v1

**Figure 22. DPAK (TO-252) reel outline**


AM06038v1

**Table 9. DPAK (TO-252) tape and reel mechanical data**

Dim.	Tape		Dim.	Reel	
	mm			mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## Revision history

**Table 10. Document revision history**

Date	Revision	Changes
01-Dec-2023	1	First release. Part number STD3N80K5 previously included in datasheet DS9824.

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