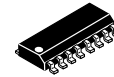


CMOS MSI

Quad R–S Latches

MC14043B, MC14044B



SOIC–16
D SUFFIX
CASE 751B

The MC14043B and MC14044B quad R–S latches are constructed with MOS P–Channel and N–Channel enhancement mode devices in a single monolithic structure. Each latch has an independent Q output and set and reset inputs. The Q outputs are gated through three–state buffers having a common enable input. The outputs are enabled with a logical “1” or high on the enable input; a logical “0” or low disconnects the latch from the Q outputs, resulting in an open circuit at the Q outputs.

Features

- Double Diode Input Protection
- Three–State Outputs with Common Enable
- Outputs Capable of Driving Two Low–power TTL Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
- These Devices are Pb–Free and are RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage Range	–0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage Range (DC or Transient)	–0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P _D	Power Dissipation, per Package (Note 1)	500	mW
T _A	Ambient Temperature Range	–55 to +125	°C
T _{stg}	Storage Temperature Range	–65 to +150	°C
T _L	Lead Temperature (8–Second Soldering)	260	°C

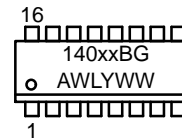
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: “D/DW” Packages: –7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MARKING DIAGRAM



- xx = Specific Device Code
- A = Assembly Location
- WL, L = Wafer Lot
- YY, Y = Year
- WW, W = Work Week
- G = Pb–Free Indicator

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

MC14043B, MC14044B

PIN ASSIGNMENT



NC = NO CONNECTION

Figure 1.

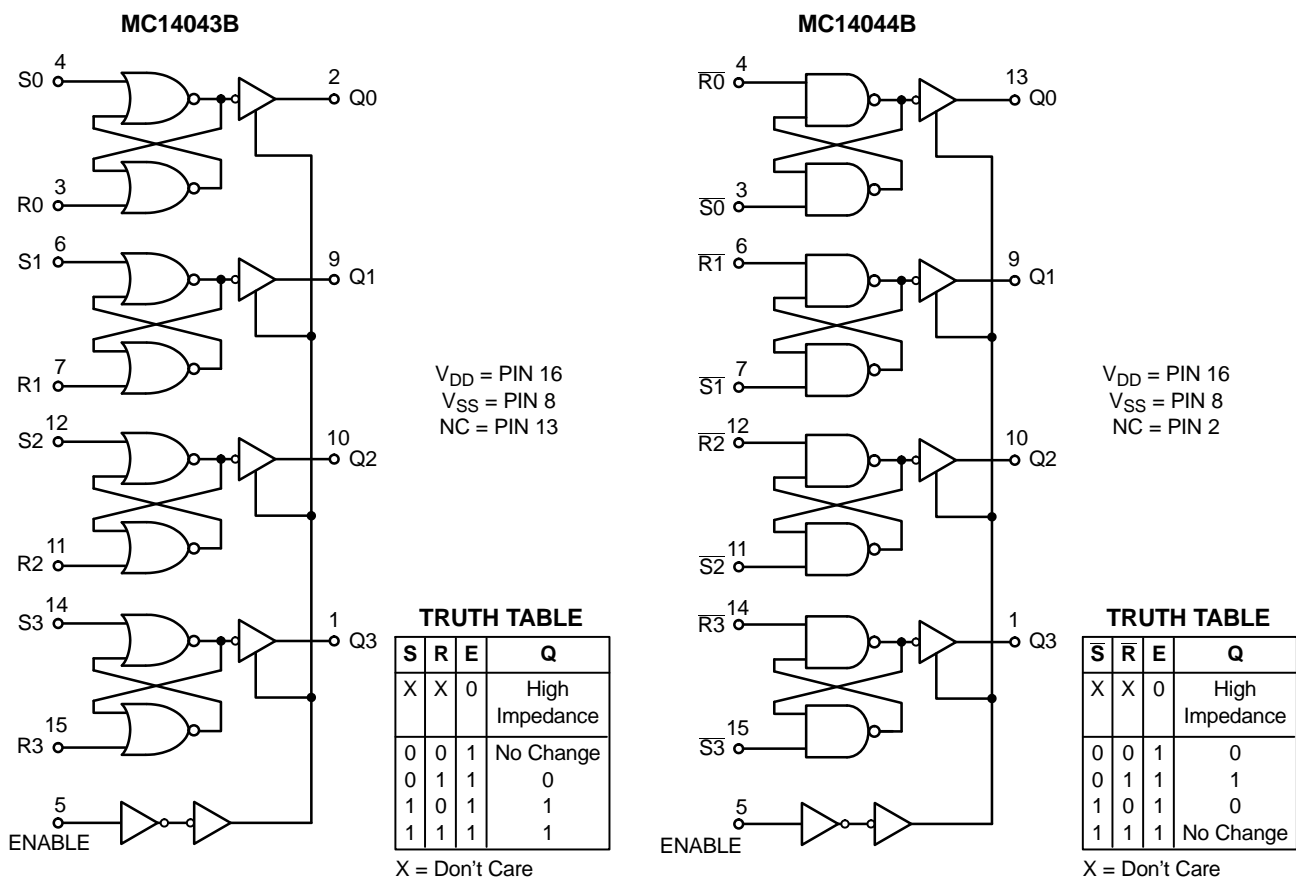


Figure 2.

MC14043B, MC14044B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (Note 2)	Max	Min	Max		
Output Voltage $V_{in} = V_{DD}$ or 0	"0" Level V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc	
		10	–	0.05	–	0	0.05	–	0.05		
		15	–	0.05	–	0	0.05	–	0.05		
	$V_{in} = 0$ or V_{DD}	"1" Level V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
			10	9.95	–	9.95	10	–	9.95	–	
			15	14.95	–	14.95	15	–	14.95	–	
Input Voltage ($V_O = 4.5$ or 0.5 Vdc) ($V_O = 9.0$ or 1.0 Vdc) ($V_O = 13.5$ or 1.5 Vdc)	"0" Level V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc	
		10	–	3.0	–	4.50	3.0	–	3.0		
		15	–	4.0	–	6.75	4.0	–	4.0		
	$V_O = 0.5$ or 4.5 Vdc) ($V_O = 1.0$ or 9.0 Vdc) ($V_O = 1.5$ or 13.5 Vdc)	"1" Level V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
			10	7.0	–	7.0	5.50	–	7.0	–	
			15	11	–	11	8.25	–	11	–	
Output Drive Current ($V_{OH} = 2.5$ Vdc) ($V_{OH} = 4.6$ Vdc) ($V_{OH} = 9.5$ Vdc) ($V_{OH} = 13.5$ Vdc)	Source I_{OH}	5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	mA _{dc}	
		5.0	–0.64	–	–0.51	–0.88	–	–0.36	–		
		10	–1.6	–	–1.3	–2.25	–	–0.9	–		
		15	–4.2	–	–3.4	–8.8	–	–2.4	–		
	Sink I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mA _{dc}	
		10	1.6	–	1.3	2.25	–	0.9	–		
15		4.2	–	3.4	8.8	–	2.4	–			
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μA _{dc}	
Input Capacitance ($V_{in} = 0$)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF	
Quiescent Current (Per Package)	I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	μA _{dc}	
		10	–	2.0	–	0.004	2.0	–	60		
		15	–	4.0	–	0.006	4.0	–	120		
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) ($C_L = 50$ pF on all outputs all buffers switching)	I_T	5.0	$I_T = (0.58 \mu A/kHz) f + I_{DD}$							μA _{dc}	
		10	$I_T = (1.15 \mu A/kHz) f + I_{DD}$								
		15	$I_T = (1.73 \mu A/kHz) f + I_{DD}$								
Three-State Output Leakage Current	I_{TL}	15	–	±0.1	–	±0.0001	±0.1	–	±3.0	μA _{dc}	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.004$.

MC14043B, MC14044B

SWITCHING CHARACTERISTICS (Note 5) ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise Time $t_{TLH} = (1.35 \text{ ns/pF}) C_L + 32.5 \text{ ns}$ $t_{TLH} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$	t_{TLH}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Output Fall Time $t_{THL} = (1.35 \text{ ns/pF}) C_L + 32.5 \text{ ns}$ $t_{THL} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{THL} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$	t_{THL}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Propagation Delay Time $t_{PLH} = (0.90 \text{ ns/pF}) C_L + 130 \text{ ns}$ $t_{PLH} = (0.36 \text{ ns/pF}) C_L + 57 \text{ ns}$ $t_{PLH} = (0.26 \text{ ns/pF}) C_L + 47 \text{ ns}$ $t_{PHL} = (0.90 \text{ ns/pF}) C_L + 130 \text{ ns}$ $t_{PHL} = (0.90 \text{ ns/pF}) C_L + 57 \text{ ns}$ $t_{PHL} = (0.26 \text{ ns/pF}) C_L + 47 \text{ ns}$	t_{PLH} t_{PHL}	5.0 10 15	– – –	175 75 60	350 175 120	ns
Set, $\overline{\text{Set}}$ Pulse Width	t_W	5.0 10 15	200 100 70	80 40 30	– – –	ns
Reset, $\overline{\text{Reset}}$ Pulse Width	t_W	5.0 10 15	200 100 70	80 40 30	– – –	ns
Three-State Enable/Disable Delay	t_{PLZ} , t_{PHZ} , t_{PZL} , t_{PZH}	5.0 10 15	– – –	150 80 55	300 160 110	ns

5. The formulas given are for the typical characteristics only at 25°C .

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

AC WAVEFORMS

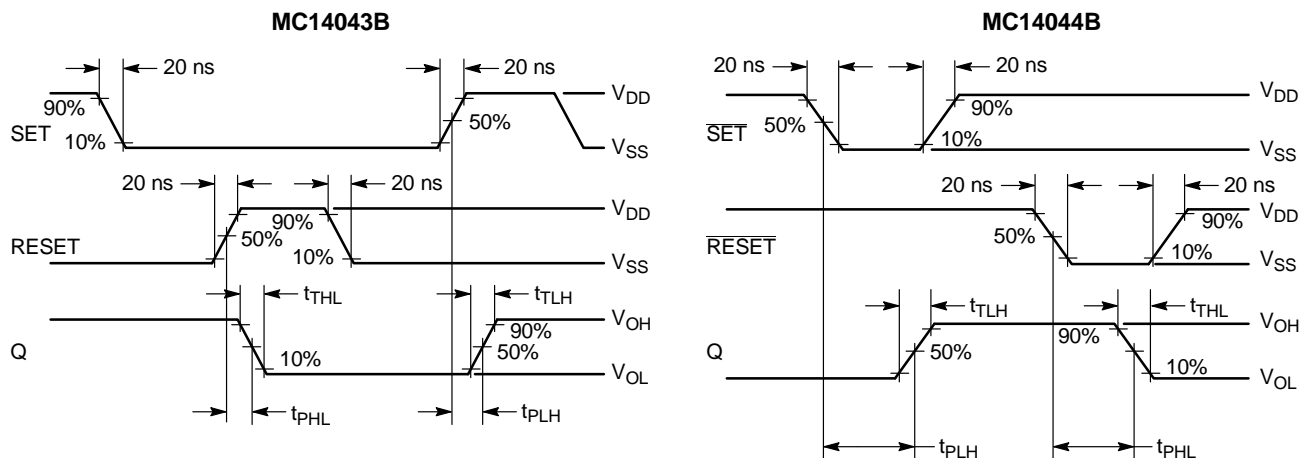


Figure 3.

MC14043B, MC14044B

THREE-STATE ENABLE/DISABLE DELAYS

Set, Reset, Enable, and Switch Conditions for 3-State Tests

Test	Enable	S1	S2	Q	MC14043B		MC14044B	
					S	R	\bar{S}	R
t _{PZH}		Open	Closed	A	V _{DD}	V _{SS}	V _{SS}	V _{DD}
t _{PZL}		Closed	Open	B	V _{SS}	V _{DD}	V _{DD}	V _{SS}
t _{PHZ}		Open	Closed	A	V _{DD}	V _{SS}	V _{SS}	V _{DD}
t _{PLZ}		Closed	Open	B	V _{SS}	V _{DD}	V _{DD}	V _{SS}

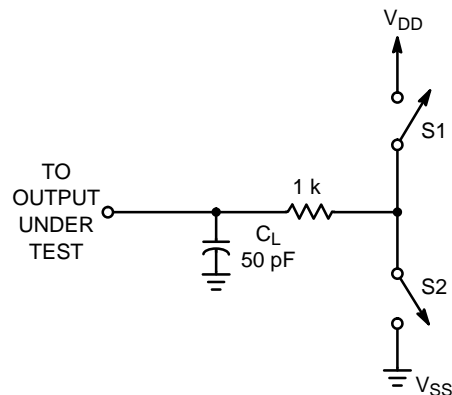


Figure 4.

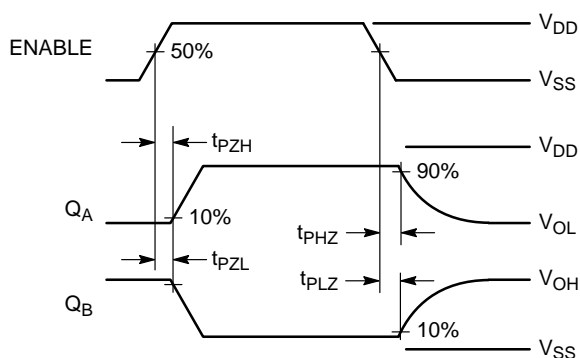


Figure 5.

ORDERING INFORMATION

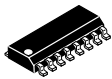
Device	Package	Shipping [†]
MC14043BDG	SOIC-16 (Pb-Free)	48 Units / Rail
NLV14043BDG*	SOIC-16 (Pb-Free)	48 Units / Rail
MC14043BDR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
NLV14043BDR2G*	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel

MC14044BDG	SOIC-16 (Pb-Free)	48 Units / Rail
MC14044BDR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
NLV14044BDR2G*	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

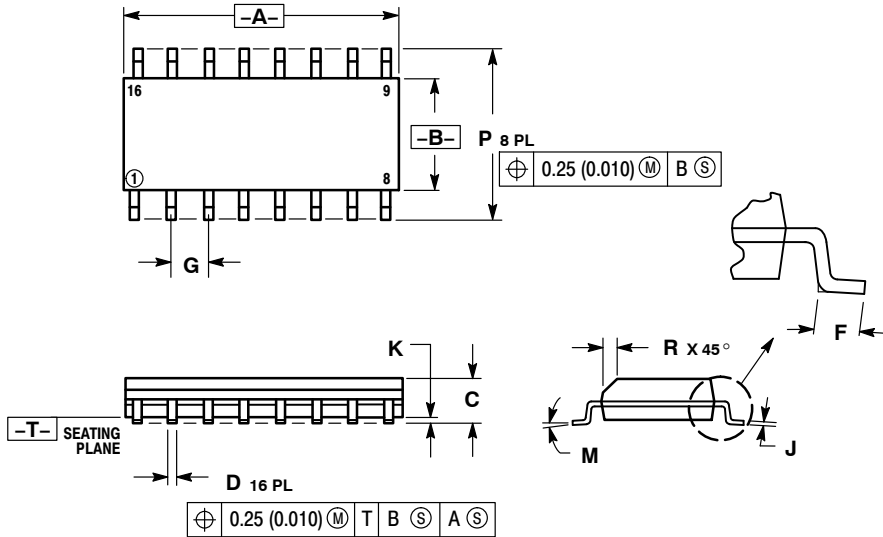
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-16
CASE 751B-05
ISSUE K

DATE 29 DEC 2006



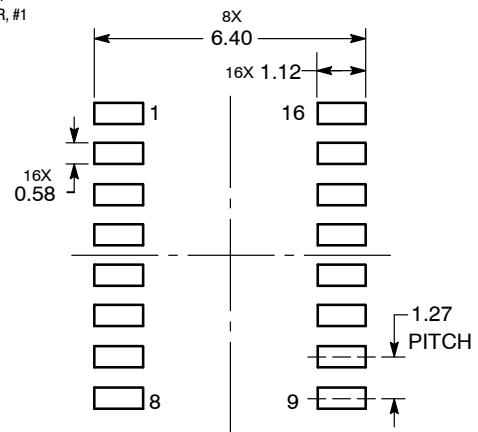
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0° 7°		0° 7°	
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

- | | | | |
|--|--|--|--|
| <p>STYLE 1:</p> <p>PIN 1. COLLECTOR</p> <p>2. BASE</p> <p>3. EMITTER</p> <p>4. NO CONNECTION</p> <p>5. EMITTER</p> <p>6. BASE</p> <p>7. COLLECTOR</p> <p>8. COLLECTOR</p> <p>9. BASE</p> <p>10. EMITTER</p> <p>11. NO CONNECTION</p> <p>12. EMITTER</p> <p>13. BASE</p> <p>14. COLLECTOR</p> <p>15. EMITTER</p> <p>16. COLLECTOR</p> | <p>STYLE 2:</p> <p>PIN 1. CATHODE</p> <p>2. ANODE</p> <p>3. NO CONNECTION</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. NO CONNECTION</p> <p>7. ANODE</p> <p>8. CATHODE</p> <p>9. CATHODE</p> <p>10. ANODE</p> <p>11. NO CONNECTION</p> <p>12. CATHODE</p> <p>13. CATHODE</p> <p>14. NO CONNECTION</p> <p>15. ANODE</p> <p>16. CATHODE</p> | <p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. BASE, #1</p> <p>3. EMITTER, #1</p> <p>4. COLLECTOR, #1</p> <p>5. COLLECTOR, #2</p> <p>6. BASE, #2</p> <p>7. EMITTER, #2</p> <p>8. COLLECTOR, #2</p> <p>9. COLLECTOR, #3</p> <p>10. BASE, #3</p> <p>11. EMITTER, #3</p> <p>12. COLLECTOR, #3</p> <p>13. COLLECTOR, #4</p> <p>14. BASE, #4</p> <p>15. EMITTER, #4</p> <p>16. COLLECTOR, #4</p> | <p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. COLLECTOR, #1</p> <p>3. COLLECTOR, #2</p> <p>4. COLLECTOR, #2</p> <p>5. COLLECTOR, #3</p> <p>6. COLLECTOR, #3</p> <p>7. COLLECTOR, #4</p> <p>8. COLLECTOR, #4</p> <p>9. BASE, #4</p> <p>10. EMITTER, #4</p> <p>11. BASE, #3</p> <p>12. EMITTER, #3</p> <p>13. BASE, #2</p> <p>14. EMITTER, #2</p> <p>15. BASE, #1</p> <p>16. EMITTER, #1</p> |
| <p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1</p> <p>2. DRAIN, #1</p> <p>3. DRAIN, #2</p> <p>4. DRAIN, #2</p> <p>5. DRAIN, #3</p> <p>6. DRAIN, #3</p> <p>7. DRAIN, #4</p> <p>8. DRAIN, #4</p> <p>9. GATE, #4</p> <p>10. SOURCE, #4</p> <p>11. GATE, #3</p> <p>12. SOURCE, #3</p> <p>13. GATE, #2</p> <p>14. SOURCE, #2</p> <p>15. GATE, #1</p> <p>16. SOURCE, #1</p> | <p>STYLE 6:</p> <p>PIN 1. CATHODE</p> <p>2. CATHODE</p> <p>3. CATHODE</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. CATHODE</p> <p>7. CATHODE</p> <p>8. CATHODE</p> <p>9. ANODE</p> <p>10. ANODE</p> <p>11. ANODE</p> <p>12. ANODE</p> <p>13. ANODE</p> <p>14. ANODE</p> <p>15. ANODE</p> <p>16. ANODE</p> | <p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH</p> <p>2. COMMON DRAIN (OUTPUT)</p> <p>3. COMMON DRAIN (OUTPUT)</p> <p>4. GATE P-CH</p> <p>5. COMMON DRAIN (OUTPUT)</p> <p>6. COMMON DRAIN (OUTPUT)</p> <p>7. COMMON DRAIN (OUTPUT)</p> <p>8. SOURCE P-CH</p> <p>9. SOURCE P-CH</p> <p>10. COMMON DRAIN (OUTPUT)</p> <p>11. COMMON DRAIN (OUTPUT)</p> <p>12. COMMON DRAIN (OUTPUT)</p> <p>13. GATE N-CH</p> <p>14. COMMON DRAIN (OUTPUT)</p> <p>15. COMMON DRAIN (OUTPUT)</p> <p>16. SOURCE N-CH</p> | |

RECOMMENDED
SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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