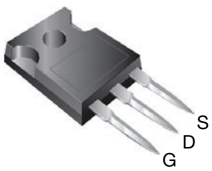
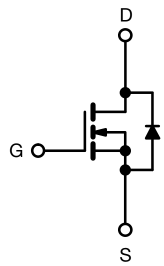
Power MOSFET

TO-247AC





N-Channel MOSFET

FEATURES

- Superfast body diode eliminates the need for external diodes in ZVS applications
- Lower gate charge results in simpler drive requirements
- Enhanced dV/dt capabilities offer improved ruggedness
- Higher gate voltage threshold offers improved noise immunity
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb Available

RoHS* Available

APPLICATIONS

- Zero voltage switching SMPS
- Telecom and server power supplies
- Uninterruptible power supplies
- Motor control applications

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

PRODUCT SUMMARY		
V_{DS} (V)	500	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.190
Q_g max. (nC)	150	
Q_{gs} (nC)	44	
Q_{gd} (nC)	72	
Configuration	Single	

ORDERING INFORMATION	
Package	TO-247AC
Lead (Pb)-free	IRFP23N50LPbF

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	500	V
Gate-source voltage			V_{GS}	± 30	
Continuous drain current	V_{GS} at 10 V	T_C = 25 °C	I_D	23	A
		T_C = 100 °C		15	
Pulsed drain current [a]			I_{DM}	92	
Linear derating factor				2.9	W/°C
Single pulse avalanche energy [b]			E_{AS}	410	mJ
Repetitive avalanche current [a]			I_{AR}	23	A
Repetitive avalanche energy [a]			E_{AR}	37	mJ
Maximum power dissipation	T_C = 25 °C		P_D	370	W
Peak diode recovery dV/dt [c]			dV/dt	21	V/ns
Operating junction and storage temperature range			T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) [d]	for 10 s			300	
Mounting torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

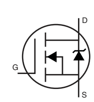
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Starting T_J = 25 °C, L = 1.5 mH, R_g = 25 Ω, I_{AS} = 23 A (see fig. 12)

c. $I_{SD} \leq$ 23 A, dI/dt $\leq$ 650 A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 150 °C

d. 1.6 mm from case

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum junction-to-ambient	R_{thJA}	-	40	°C/W
Case-to-sink, flat, greased surface	R_{thCS}	0.24	-	
Maximum junction-to-case (drain)	R_{thJC}	-	0.34	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	500	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA [d]	-	0.27	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	3.0	-	5.0	V
Gate-source leakage	I_{GSS}	V_{GS} = ± 30 V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V	-	-	50	μA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125 °C	-	-	2.0	mA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 14 A [b]	-	0.190	0.235	Ω
Forward transconductance	g_{fs}	V_{DS} = 50 V, I_D = 14 A [b]	-	9	-	S
Dynamic						
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5	-	3600	-	pF
Output capacitance	C_{oss}		-	380	-	
Reverse transfer capacitance	C_{rss}		-	37	-	
Output capacitance	C_{oss}	V_{GS} = 0 V, V_{DS} = 1.0 V, f = 1.0 MHz	-	4800	-	
		V_{GS} = 0 V, V_{DS} = 400 V, f = 1.0 MHz	-	100	-	
Effective output capacitance	C_{oss} eff.	V_{GS} = 0 V, V_{DS} = 0 V to 400 V [c]	-	220	-	
Effective output capacitance (energy related)	C_{oss} eff. (ER)	V_{GS} = 0 V, V_{DS} = 0 V to 400 V [d]	-	160	-	
Internal gate resistance	R_G	f = 1 MHz, open drain	-	1.2	-	Ω
Total gate charge	Q_g	V_{GS} = 10 V, I_D = 23 A, V_{DS} = 400 V see fig. 6 and 13 [b]	-	-	150	nC
Gate-source charge	Q_{gs}		-	-	44	
Gate-drain charge	Q_{gd}		-	-	72	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 250 V, I_D = 23 A R_g = 6.0, V_{GS} = 10 V see fig. 10 [b]	-	26	-	ns
Rise time	t_r		-	94	-	
Turn-off delay time	$t_{d(off)}$		-	53	-	
Fall time	t_f		-	45	-	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	23	A
Pulsed diode forward current [a]	I_{SM}		-	-	92	
Body diode voltage	V_{SD}	T_J = 25 °C, I_S = 14 A, V_{GS} = 0 V [b]	-	-	1.5	V
Body diode reverse recovery time	t_{rr}	T_J = 25 °C, I_F = 23 A, dI/dt = 100 A/μs [b]	-	170	250	ns
		T_J = 125 °C	-	220	330	
Body diode reverse recovery charge	Q_{rr}	T_J = 25 °C	-	560	840	μC
		T_J =1 25 °C	-	980	1500	
Reverse recovery current	I_{RRM}	T_J = 25 °C	-	7.6	11	A
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %
c. C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 % to 80 % V_{DS}
d. C_{oss} eff. (ER) is a fixed capacitance that stores the same energy time as C_{OSS} while V_{DS} is rising from 0 % to 80 % V_{DS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

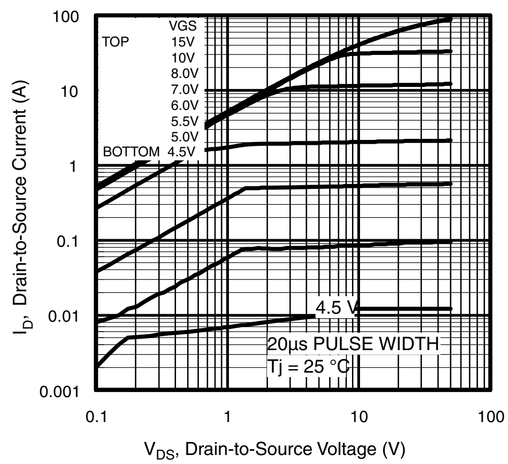


Fig. 1 - Typical Output Characteristics

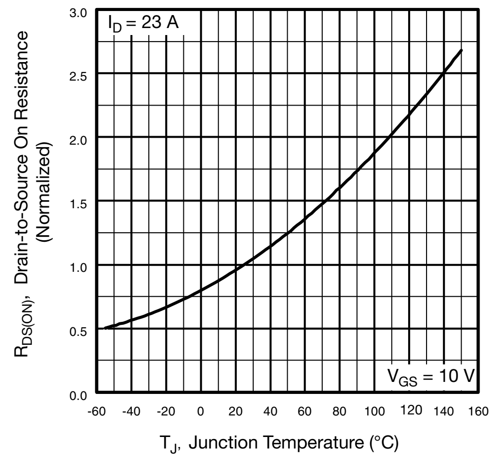


Fig. 4 - Normalized On-Resistance vs. Temperature

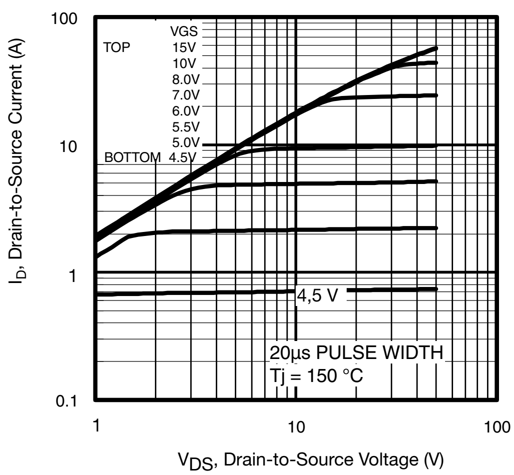


Fig. 2 - Typical Output Characteristics

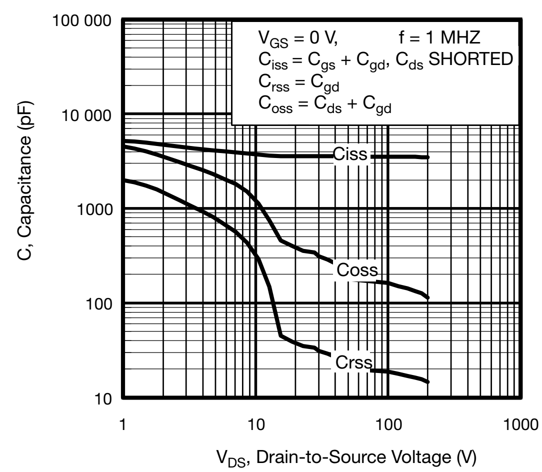


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

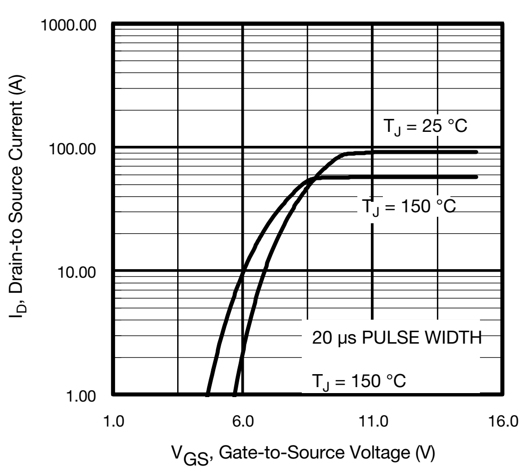


Fig. 3 - Typical Transfer Characteristics

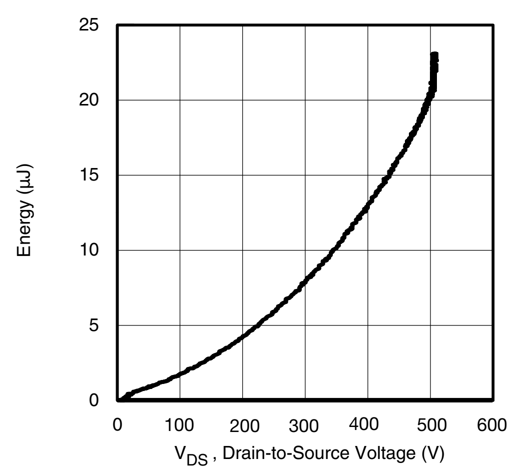


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

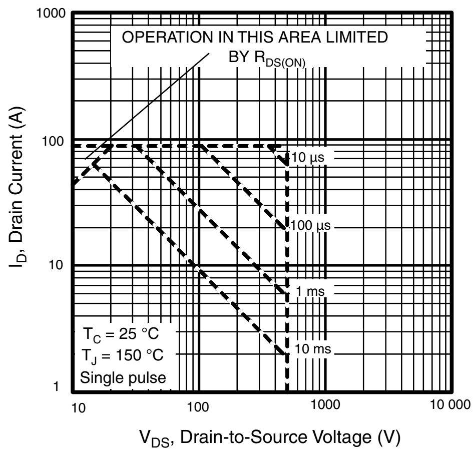


Fig. 7 - Maximum Safe Operating Area

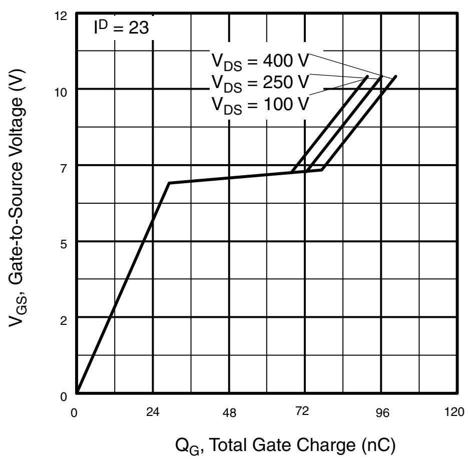


Fig. 8 - Typical Gate Charge vs. Gate-to-Source Voltage

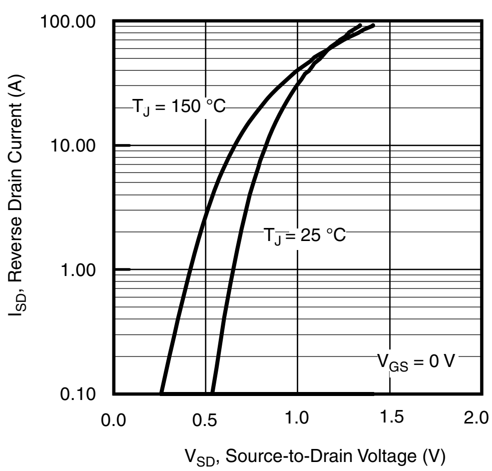


Fig. 9 - Typical Source-Drain Diode Forward Voltage

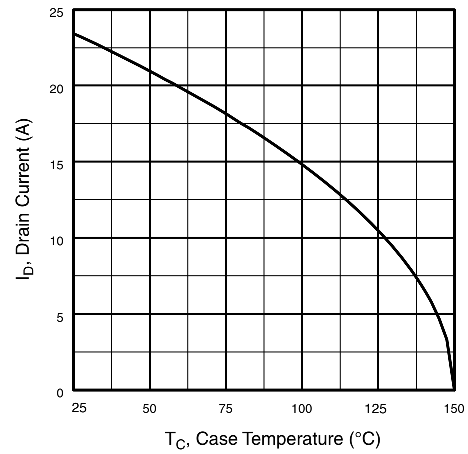


Fig. 10 - Maximum Drain Current vs. Case Temperature

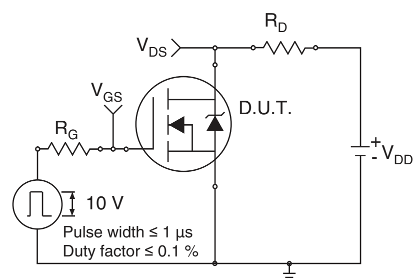


Fig. 11a - Switching Time Test Circuit

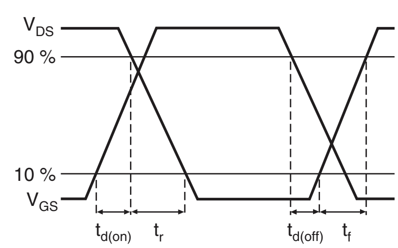


Fig. 11b - Switching Time Waveforms

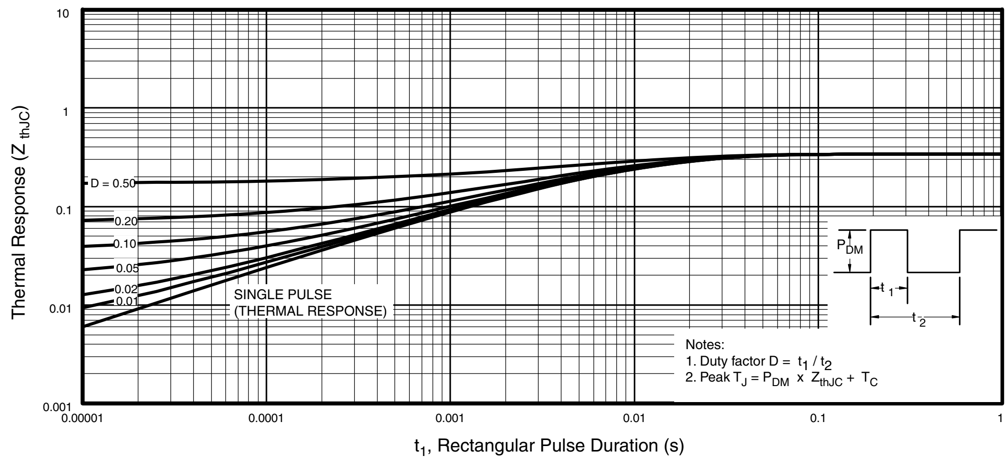


Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

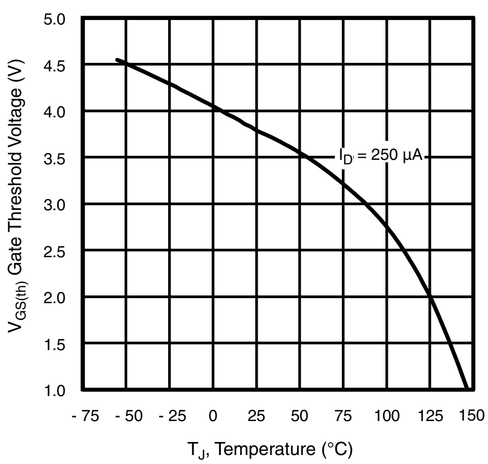


Fig. 13 - Threshold Voltage vs. Temperature

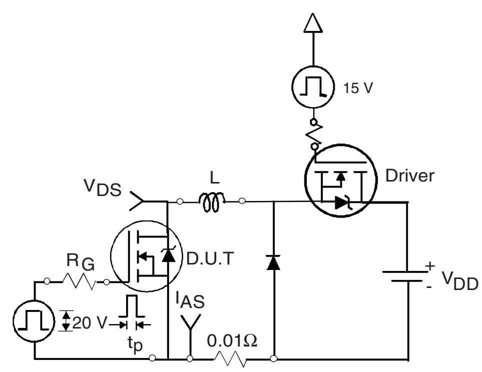


Fig. 15a - Unclamped Inductive Test Circuit

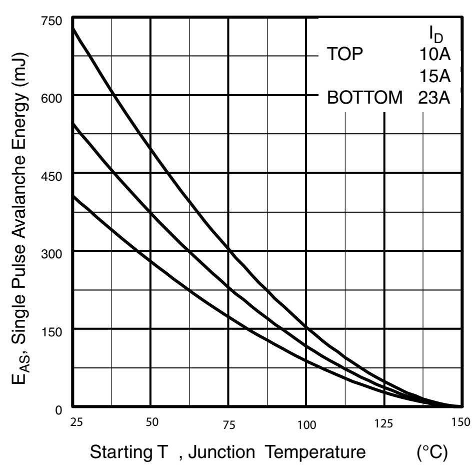


Fig. 14 - Maximum Avalanche Energy s. Drain Current

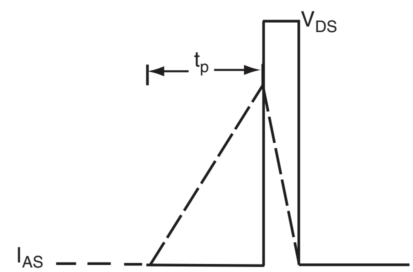


Fig. 15b - Unclamped Inductive Waveforms

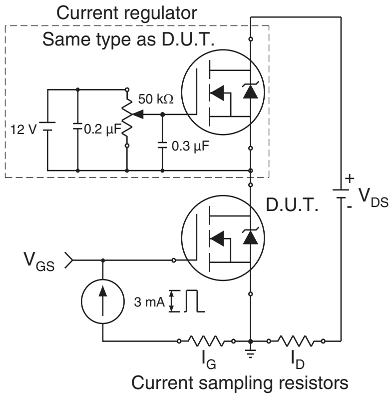


Fig. 16a - Gate Charge Test Circuit

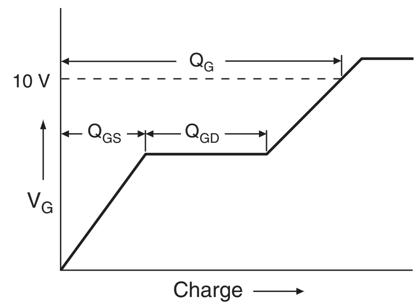
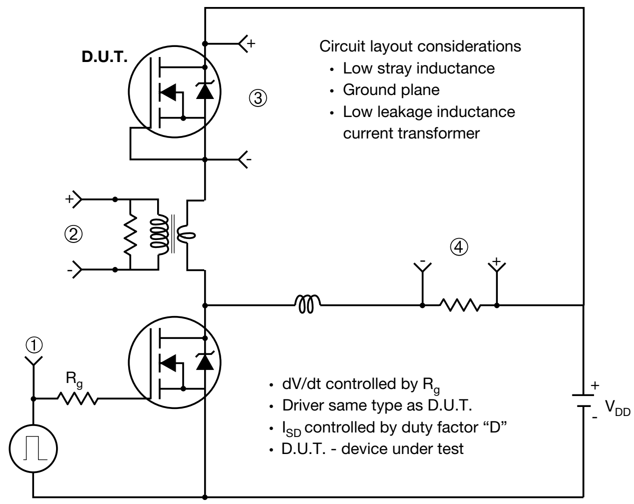
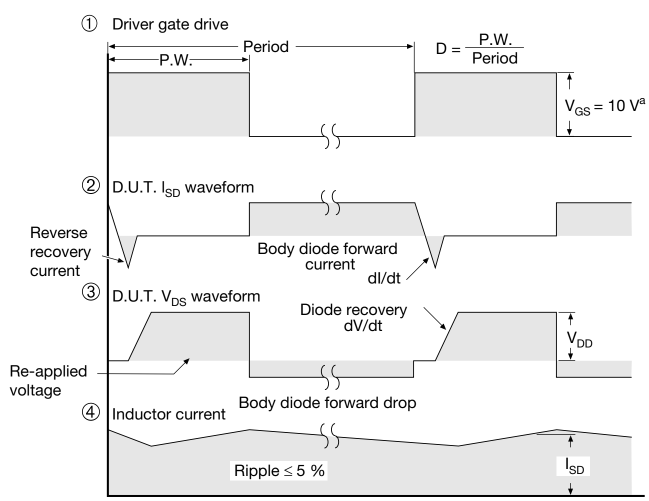


Fig. 16b - Basic Gate Charge Waveform

Peak Diode Recovery dV/dt Test Circuit





Note

a. V_{GS} = 5 V for logic level devices

Fig. 17 - For N-Channel

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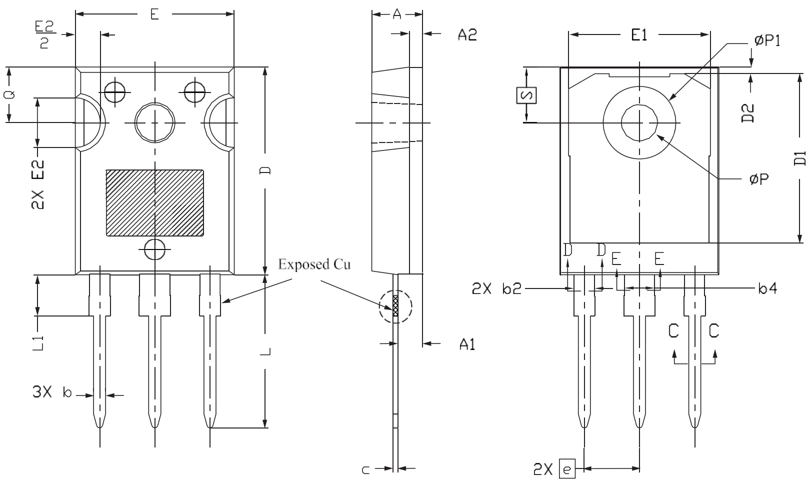
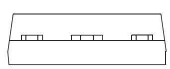
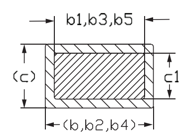
TO-247AC (High Voltage)

VERSION 1: FACILITY CODE = 9







Section C--C,D--D,E--E

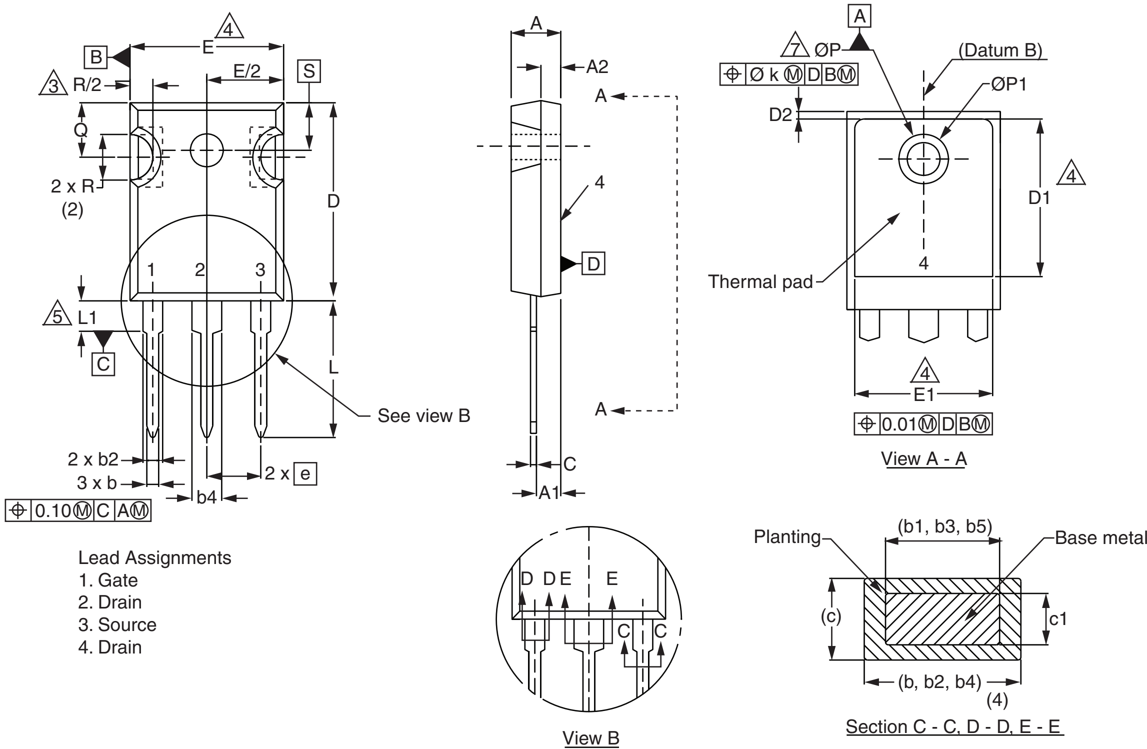
	MILLIMETERS			
DIM.	MIN.	NOM.	MAX.	NOTES
A	4.83	5.02	5.21	
A1	2.29	2.41	2.55	
A2	1.17	1.27	1.37	
b	1.12	1.20	1.33	
b1	1.12	1.20	1.28	
b2	1.91	2.00	2.39	6
b3	1.91	2.00	2.34	
b4	2.87	3.00	3.22	6, 8
b5	2.87	3.00	3.18	
c	0.40	0.50	0.60	6
c1	0.40	0.50	0.56	
D	20.40	20.55	20.70	4

	MILLIMETERS			
DIM.	MIN.	NOM.	MAX.	NOTES
D1	16.46	16.76	17.06	5
D2	0.56	0.66	0.76	
E	15.50	15.70	15.87	4
E1	13.46	14.02	14.16	5
E2	4.52	4.91	5.49	3
e	5.46 BSC			
L	14.90	15.15	15.40	
L1	3.96	4.06	4.16	6
Ø P	3.56	3.61	3.65	7
Ø P1	7.19 ref.			
Q	5.31	5.50	5.69	
S	5.51 BSC			

Notes

(1) Package reference: JEDEC® TO247, variation AC
(2) All dimensions are in mm
(3) Slot required, notch may be rounded
(4) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extremes of the plastic body
(5) Thermal pad contour optional with dimensions D1 and E1
(6) Lead finish uncontrolled in L1
(7) Ø P to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91 mm
(8) Dimension b2 and b4 does not include dambar protrusion. Allowable dambar protrusion shall be 0.1 mm total in excess of b2 and b4 dimension at maximum material condition

VERSION 2: FACILITY CODE = Y



	MILLIMETERS		
DIM.	MIN.	MAX.	NOTES
A	4.58	5.31	
A1	2.21	2.59	
A2	1.17	2.49	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.53	2.39	
b3	1.65	2.37	
b4	2.42	3.43	
b5	2.59	3.38	
c	0.38	0.86	
c1	0.38	0.76	
D	19.71	20.82	
D1	13.08	-	

	MILLIMETERS		
DIM.	MIN.	MAX.	NOTES
D2	0.51	1.30	
E	15.29	15.87	
E1	13.72	-	
e	5.46 BSC		
Ø k	0.254		
L	14.20	16.25	
L1	3.71	4.29	
Ø P	3.51	3.66	
Ø P1	-	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51 BSC		

Notes

(1) Dimensioning and tolerancing per ASME Y14.5M-1994

(2) Contour of slot optional

(3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body

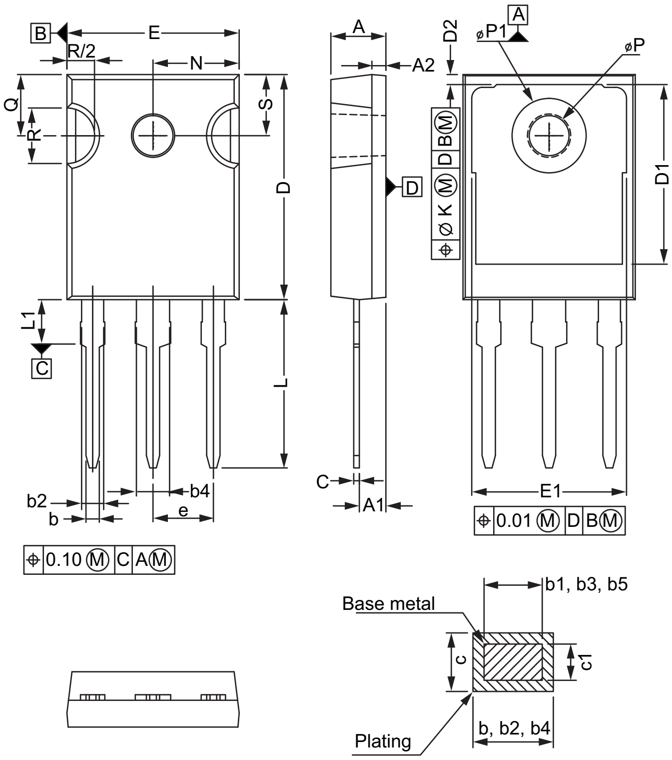
(4) Thermal pad contour optional with dimensions D1 and E1

(5) Lead finish uncontrolled in L1

(6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")

(7) Outline conforms to JEDEC outline TO-247 with exception of dimension c

VERSION 3: FACILITY CODE = N



	MILLIMETERS	
DIM.	MIN.	MAX.
A	4.65	5.31
A1	2.21	2.59
A2	1.17	1.37
b	0.99	1.40
b1	0.99	1.35
b2	1.65	2.39
b3	1.65	2.34
b4	2.59	3.43
b5	2.59	3.38
c	0.38	0.89
c1	0.38	0.84
D	19.71	20.70
D1	13.08	-

	MILLIMETERS	
DIM.	MIN.	MAX.
D2	0.51	1.35
E	15.29	15.87
E1	13.46	-
e	5.46 BSC	
k	0.254	
L	14.20	16.10
L1	3.71	4.29
N	7.62 BSC	
P	3.56	3.66
P1	-	7.39
Q	5.31	5.69
R	4.52	5.49
S	5.51 BSC	

ECN: E22-0452-Rev. G, 31-Oct-2022
DWG: 5971

Notes

(1) Dimensioning and tolerancing per ASME Y14.5M-1994
(2) Contour of slot optional
(3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
(4) Thermal pad contour optional with dimensions D1 and E1
(5) Lead finish uncontrolled in L1
(6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")

For technical questions, contact: hvm@vishay.com

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