1. General-Purpose PLLs in Stratix & Stratix GX Devices

S52001-3.2

Introduction

Stratix® and Stratix GX devices have highly versatile phase-locked loops (PLLs) that provide robust clock management and synthesis for on-chip clock management, external system clock management, and high-speed I/O interfaces. There are two types of PLLs in each Stratix and Stratix GX device: enhanced PLLs and fast PLLs. Each device has up to four enhanced PLLs, which are feature-rich, general-purpose PLLs supporting advanced capabilities such as external feedback, clock switchover, phase and delay control, PLL reconfiguration, spread spectrum clocking, and programmable bandwidth. There are also up to eight fast PLLs per device, which offer general-purpose clock management with multiplication and phase shifting as well as high-speed outputs to manage the high-speed differential I/O interfaces.

The Altera® Quartus® II software enables the PLLs and their features without requiring any external devices.

Tables 1–1 and 1–2 show PLL availability for Stratix and Stratix GX devices, respectively.

Table 1–1. Stratix Device PLL Availability

Device	Fast PLLs								Enhanced PLLs			
	1	2	3	4	7	8	9	10	5 (1)	6 (1)	11 (2)	12 (2)
EP1S10	✓	✓	✓	✓					✓	✓		
EP1S20	✓	✓	✓	✓					✓	✓		
EP1S25	✓	✓	✓	✓					✓	✓		
EP1S30	✓	✓	✓	✓	✓ (3)	✓ (3)	✓ (3)	✓ (3)	✓	✓		
EP1S40	✓	✓	✓	✓	✓ (3)	✓ (3)	✓ (3)	✓ (3)	✓	✓	✓ (3)	✓ (3)
EP1S60	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
EP1S80	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Notes to Table 1–1:

(1) PLLs 5 and 6 each have eight single-ended outputs or four differential outputs.

(2) PLLs 11 and 12 each have one single-ended output.

(3) EP1S30 and EP1S40 devices do not support these PLLs in the 780-pin FineLine BGA® package.

Table 1–2. Stratix GX Device PLL Availability

Device	Fast PLLs				Enhanced PLLs			
	1	2	7	8	5	6	11	12
EP1S10C	✓	✓			✓	✓		
EP1S10D	✓	✓			✓	✓		
EP1S25C	✓	✓			✓	✓		
EP1S25D	✓	✓			✓	✓		
EP1S25F	✓	✓			✓	✓		
EP1S40D	✓	✓	✓	✓	✓	✓	✓	✓
EP1S40G	✓	✓	✓	✓	✓	✓	✓	✓

Table 1–3 shows the enhanced and fast PLL features in Stratix and Stratix GX devices.

Table 1–3. Stratix & Stratix GX PLL Features

Feature	Enhanced PLL	Fast PLL
Clock multiplication and division	*m*/(*n* × post-scale counter) *(1)*	*m*/(post-scale counter) *(2)*
Phase shift	Down to 156.25-ps increments *(3)*, *(4)*	Down to 125-ps increments *(3)*, *(4)*
Clock switchover	✓	
PLL reconfiguration	✓	
Programmable bandwidth	✓	
Spread spectrum clocking	✓	
Programmable duty cycle	✓	✓
Number of internal clock outputs	6	3 *(5)*
Number of external clock outputs	Four differential/eight singled-ended or one single-ended *(6)*	*(7)*
Number of feedback clock inputs	2 *(8)*	

Notes to Table 1–3:

(1) For enhanced PLLs, *m*, *n*, range from 1 to 512 and post-scale counters g, l, e range from 1 to 1024 with 50% duty cycle. With a non-50% duty cycle the post-scale counters g, l, e range from 1 to 512.
(2) For fast PLLs, *m*, *n*, and post-scale counters range from 1 to 32.
(3) The smallest phase shift is determined by the voltage controlled oscillator (VCO) period divided by 8.
(4) For degree increments, Stratix and Stratix GX devices can shift all output frequencies in increments of at least 45° . Smaller degree increments are possible depending on the frequency and divide parameters.
(5) PLLs 7, 8, 9, and 10 have two output ports per PLL. PLLs 1, 2, 3, and 4 have three output ports per PLL. On Stratix GX devices, PLLs 3, 4, 9, and 10 are not available for general-purpose use.
(6) Every Stratix and Stratix GX device has two enhanced PLLs (PLLs 5 and 6) with either eight single-ended outputs or four differential outputs each. Two additional enhanced PLLs (PLLs 11 and 12) in EP1S80, EP1S60, EP1S40 (PLL 11 and 12 not supported for F780 package), and EP1SGX40 devices each have one single-ended output.
(7) Fast PLLs can drive to any I/O pin as an external clock. For high-speed differential I/O pins, the device uses a data channel to generate `txclkout`.
(8) Every Stratix and Stratix GX device has two enhanced PLLs with one single-ended or differential external feedback input per PLL.

Figure 1–1 shows a top-level diagram of the Stratix device and PLL floorplan. Figure 1–2 shows a top-level diagram of the Stratix GX device and PLL floorplan. See "Clocking" on page 1–39 for more detail on PLL connections to global and regional clocks.

Figure 1–1. Stratix PLL Locations

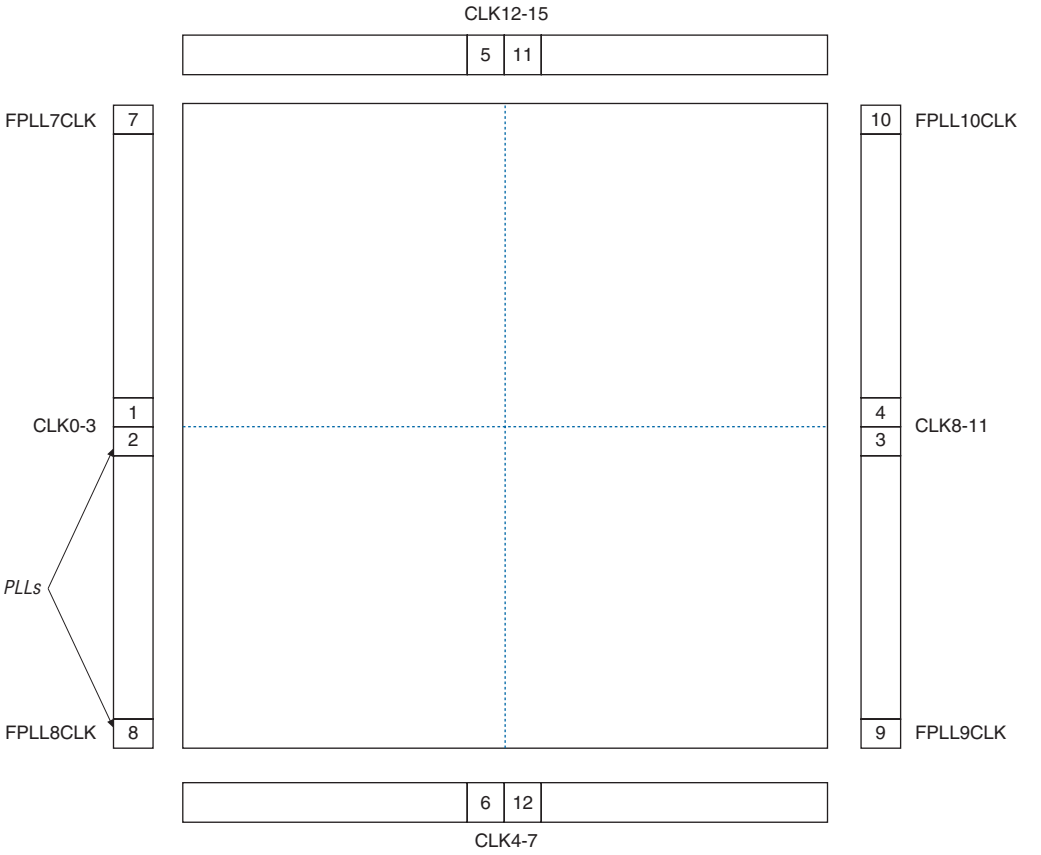
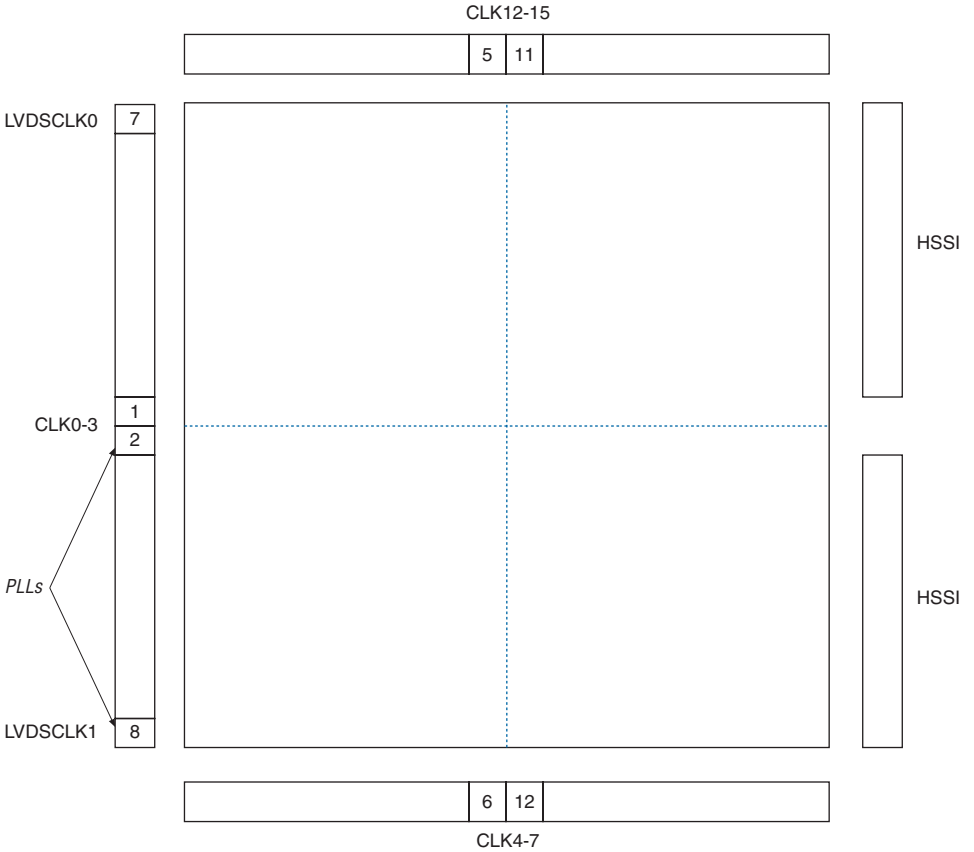


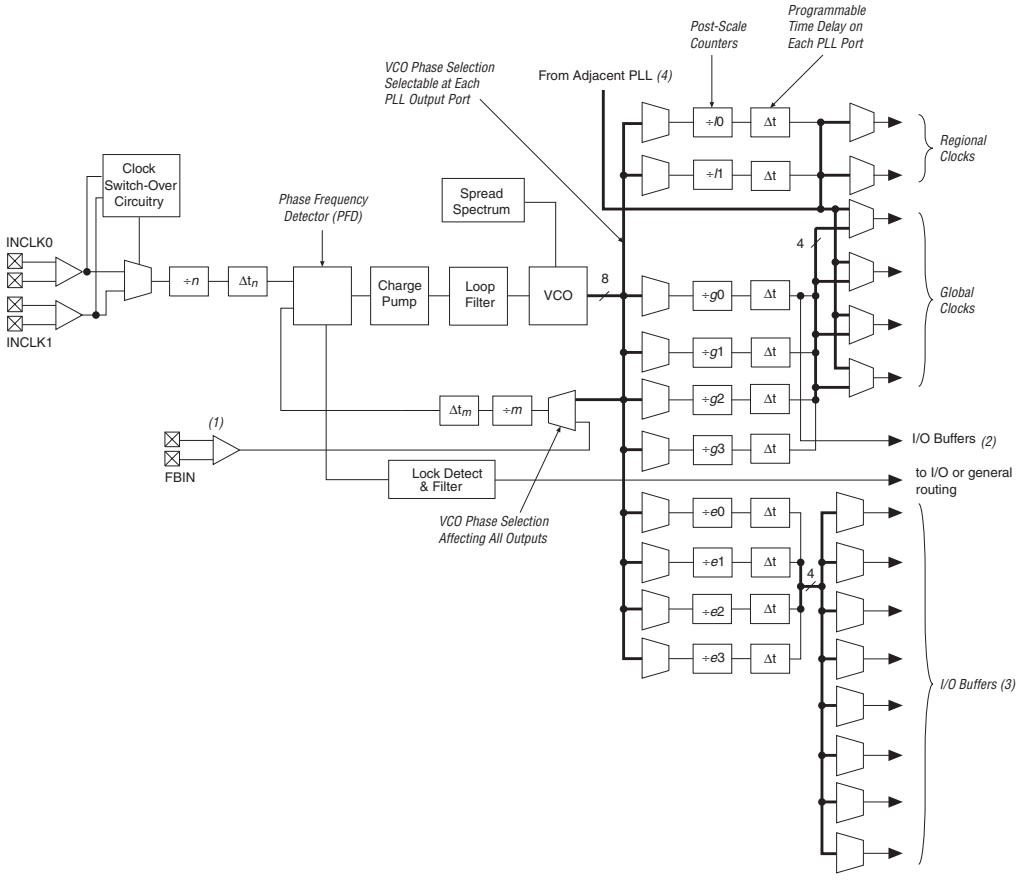
Figure 1–2. Stratix GX PLL Locations



Enhanced PLLs

Stratix and Stratix GX devices contain up to four enhanced PLLs with advanced clock management features. Figure 1–3 shows a diagram of the enhanced PLL.

Figure 1–3. Stratix & Stratix GX Enhanced PLL

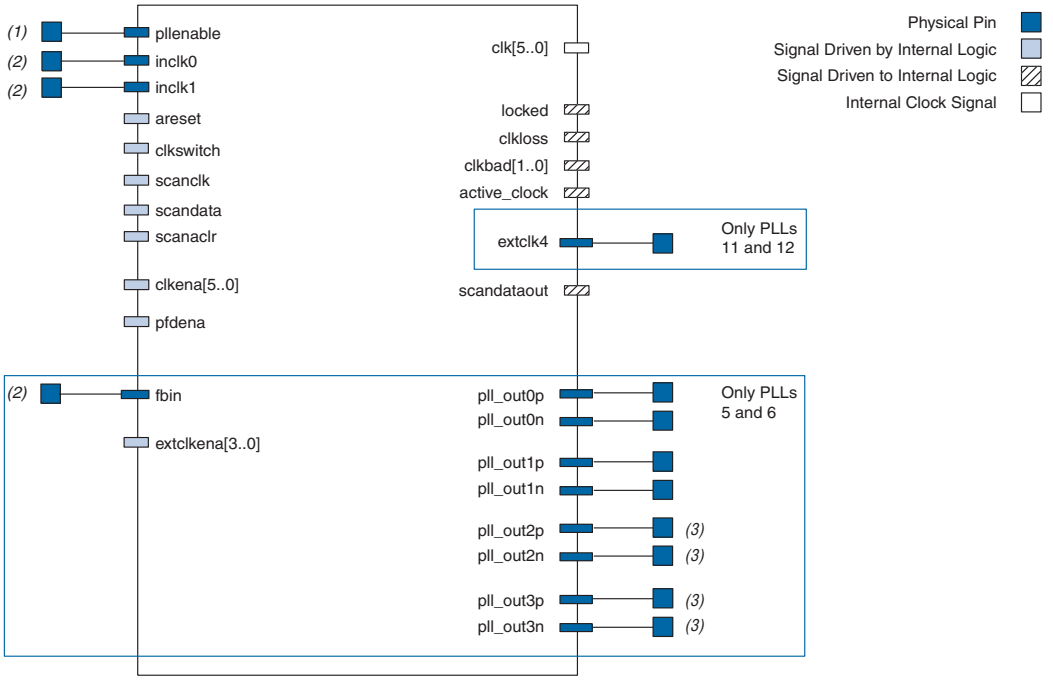


Notes to Figure 1–3:

(1) External feedback is available in PLLs 5 and 6.
(2) This single-ended external output is available from the *g*0 counter for PLLs 11 and 12.
(3) These four counters and external outputs are available in PLLs 5 and 6.
(4) This connection is only available on EP1SGX40 Stratix GX devices and EP1S40 and larger Stratix devices. For example, PLLs 5 and 11 are adjacent and PLLs 6 and 12 are adjacent. The EP1S40 device in the F780 package does not support PLLs 11 and 12.

Figure 1–4 shows all the possible ports of the enhanced PLLs.

Figure 1–4. Enhanced PLL Signals



Notes to Figure 1–4:

(1) This input pin is shared by all enhanced and fast PLLs.

(2) These are either single-ended or differential pins.

(3) EP1S10, EP1S20, and EP1S25 devices in 672-pin ball grid array (BGA) and 484- and 672-pin FineLine BGA packages only have two pairs of external clocks (i.e., `pll_out0p`, `pll_out0n`, `pll_out1p`, and `pll_out1n`).

Tables 1–4 and 1–5 describe all the enhanced PLL ports.

Table 1–4. Enhanced PLL Input Signals

Port	Description	Source	Destination
inclk[1..0]	Primary and secondary reference clock inputs to PLL	Pin	×*n* counter
fbin	External feedback input to the PLL (PLLs 5 and 6 only)	Pin	Phase frequency detector (PFD)
pllena	Enable pin for enabling or disabling all or a set of PLLs—active high	Pin	General PLL control signal
clkswitch	Switchover signal used to initiate external clock switchover control—this signal switches the clock on the rising edge of clkswitch	Logic array	PLL switchover circuit
areset	Signal used to reset the PLL which re-synchronizes all the counter outputs—active high	Logic array	General PLL control signal
clkena[5..0]	Enable clock driving regional or global clock—active high	Logic array	Clock output
extclkena[3..0]	Enable clock driving external clock (PLLs 5 and 6 only)—active high	Logic array	Clock output
pfdena	Enables the outputs from the phase frequency detector—active high	Logic array	PFD
scanclk	Serial clock signal for the real-time PLL control feature	Logic array	Reconfiguration circuit
scandata	Serial input data stream for the real-time PLL control feature	Logic array	Reconfiguration circuit
scanaclr	Serial shift register reset clearing all registers in the serial shift chain—active high	Logic array	Reconfiguration circuit

Table 1–5. Enhanced PLL Output Signals

Port	Description	Source	Destination
clk[5..0]	PLL outputs driving regional or global clock	PLL counter	Internal Clock
pll_out[3..0]p/n	pll_out[3..0] are PLL outputs driving the four differential or eight single-ended external clock output pins for PLLs 5 or 6. p or n are the positive (p) and negative (n) pins for differential pins.	PLL counter	Pin(s)
extclk4	PLL output driving external clock output pin from PLLs 11 and 12	PLL *g*0 counter	Pin
clkloss	Signal indicating the switchover circuit detected a switchover condition	PLL switchover circuit	Logic array
clkbad[1..0]	Signals indicating which reference clock is no longer toggling. clkbad1 indicates inclk1 status, clkbad0 indicates inclk0 status	PLL switchover circuit	Logic array
locked	Lock output from lock detect circuit—active high	PLL lock detect	Logic array
activeclock	Signal to indicate which clock (1 = inclk0 or 0 = inclk1) is driving the PLL.	PLL clock multiplexer	Logic array
scandataout	Output of the last shift register in the scan chain	PLL scan chain	Logic array

Clock Multiplication & Division

Each Stratix and Stratix GX device enhanced PLL provides clock synthesis for PLL output ports using $m/(n \times$ post-scale counter) scaling factors. The input clock is divided by a pre-scale counter, n, and is then multiplied by the m feedback factor. The control loop drives the VCO to match $f_{IN} \times (m/n)$. Each output port has a unique post-scale counter that divides down the high-frequency VCO.

For multiple PLL outputs with different frequencies, the VCO is set to the least common multiple of the output frequencies that meets its frequency specifications. Then, the post-scale counters scale down the output frequency for each output port. For example, if output frequencies required from one PLL are 33 and 66 MHz, then the Quartus II software sets the VCO to 330 MHz (the least common multiple of 33 and 66 MHz within the VCO range).

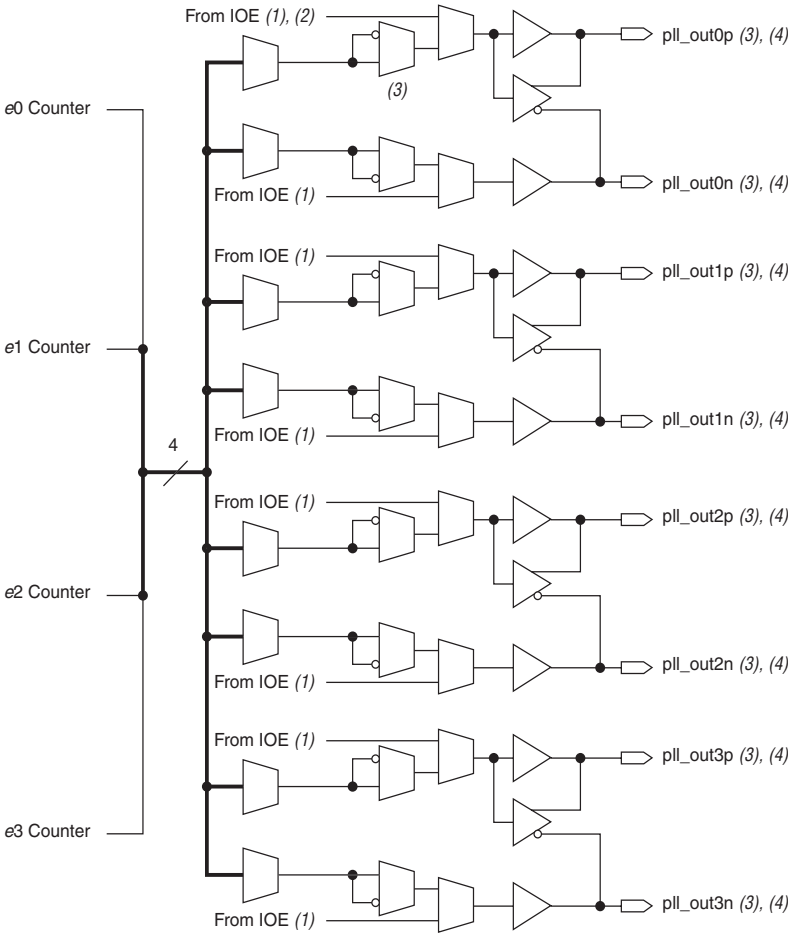
There is one pre-scale counter, n, and one multiply counter, m, per PLL, with a range of 1 to 512 on each. There are two post-scale counters (l) for regional clock output ports, four counters (g) for global clock output ports, and up to four counters (e) for external clock outputs, all ranging from 1 to 1024 with a 50% duty cycle setting. The post-scale counters

range from 1 to 512 with any non-50% duty cycle setting. The Quartus II software automatically chooses the appropriate scaling factors according to the input frequency, multiplication, and division values entered into the `altpll` MegaWizard Plug-In Manager.

External Clock Outputs

Enhanced PLLs 5 and 6 each support up to eight single-ended clock outputs (or four differential pairs). See Figure 1–5.

Figure 1–5. External Clock Outputs for PLLs 5 & 6



Notes to Figure 1–5:

(1) LE: logic element.

(2) The design can use each external clock output pin as a general-purpose output pin from the logic array. These pins are multiplexed with IOE outputs.

(3) Two single-ended outputs are possible per output counter—either two outputs of the same frequency and phase or one shifted 180° .

(4) EP1S10, EP1S20, and EP1S25 devices in 672-pin ball grid array (BGA) and 484- and 672-pin FineLine BGA packages only have two pairs of external clocks (i.e., `pll_out0p`, `pll_out0n`, `pll_out1p`, and `pll_out1n`).

Any of the four external output counters can drive the single-ended or differential clock outputs for PLLs 5 and 6. This means one counter or frequency can drive all output pins available from PLL 5 or PLL 6. Each

pair of output pins (four pins total) has dedicated VCC and GND pins to reduce the output clock's overall jitter by providing improved isolation from switching I/O pins.

For PLLs 5 and 6, each pin of a single-ended output pair can either be in phase or 180° out of phase. The Quartus II software transfers the NOT gate in the design into the IOE to implement 180° phase with respect to the other pin in the pair. The clock output pin pairs support the same I/O standards as standard output pins (in the top and bottom banks) as well as LVDS, LVPECL, PCML, HyperTransport™ technology, differential HSTL, and differential SSTL. Table 1–6 shows which I/O standards the enhanced PLL clock pins support. When in single-ended or differential mode, one power pin supports two differential or four single-ended pins. Both outputs use the same standards in single-ended mode to maintain performance. You can also use the external clock output pins as user output pins if external enhanced PLL clocking is not needed.

The enhanced PLL can also drive out to any regular I/O pin through the global or regional clock network. The jitter on the output clock is not guaranteed for this case.

Table 1–6. I/O Standards Supported for Enhanced PLL Pins (Part 1 of 2)

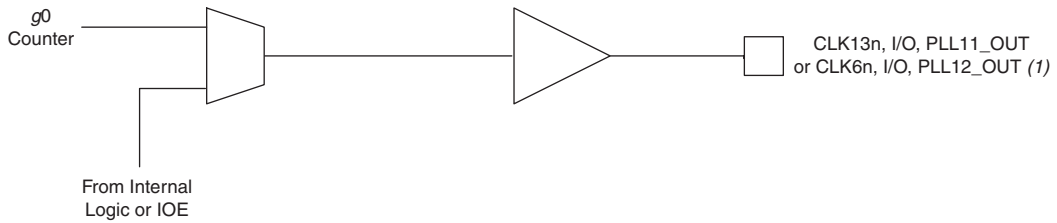
I/O Standard	Input			Output
	INCLK	FBIN	PLLENABLE	EXTCLK
LVTTL	✓	✓	✓	✓
LVCMOS	✓	✓	✓	✓
2.5 V	✓	✓		✓
1.8 V	✓	✓		✓
1.5 V	✓	✓		✓
3.3-V PCI	✓	✓		✓
3.3-V PCI-X 1.0	✓	✓		✓
LVPECL	✓	✓		✓
PCML	✓	✓		✓
LVDS	✓	✓		✓
HyperTransport technology	✓	✓		✓
Differential HSTL	✓			✓
Differential SSTL				✓
3.3-V GTL	✓	✓		✓

Table 1–6. I/O Standards Supported for Enhanced PLL Pins (Part 2 of 2)

I/O Standard	Input			Output
	INCLK	FBIN	PLLENABLE	EXTCLK
3.3-V GTL+	✓	✓		✓
1.5-V HSTL Class I	✓	✓		✓
1.5-V HSTL Class II	✓	✓		✓
1.8-V HSTL Class I	✓	✓		✓
1.8-V HSTL Class II	✓	✓		✓
SSTL-18 Class I	✓	✓		✓
SSTL-18 Class II	✓	✓		✓
SSTL-2 Class I	✓	✓		✓
SSTL-2 Class II	✓	✓		✓
SSTL-3 Class I	✓	✓		✓
SSTL-3 Class II	✓	✓		✓
AGP (1× and 2×)	✓	✓		✓
CTT	✓	✓		✓

Enhanced PLLs 11 and 12 support one single-ended output each (see Figure 1–6). These outputs do not have their own VCC and GND signals. Therefore, to minimize jitter, do not place switching I/O pins next to this output pin.

Figure 1–6. External Clock Outputs for Enhanced PLLs 11 & 12



Note to Figure 1–6:
(1) For PLL11, this pin is CLK13n; for PLL 12 this pin is CLK6n.

Stratix and Stratix GX devices can drive any enhanced PLL driven through the global clock or regional clock network to any general I/O pin as an external output clock. The jitter on the output clock is not guaranteed for these cases.

Clock Feedback

The following three feedback modes in Stratix and Stratix GX device enhanced PLLs allow multiplication and/or phase shifting:

- Zero delay buffer: The external clock output pin is phase-aligned with the clock input pin for zero delay. Altera recommends using the same I/O standard on the input clock and the output clocks for optimum performance.
- External feedback: The external feedback input pin, FBIN, is phase-aligned with the clock input, CLK, pin. Aligning these clocks allows you to remove clock delay and skew between devices. This mode is only possible for PLLs 5 and 6. PLLs 5 and 6 each support feedback for one of the dedicated external outputs, either one single-ended or one differential pair. In this mode, one encounter feeds back to the PLL FBIN input, becoming part of the feedback loop.
- Normal mode: If an internal clock is used in this mode, it is phase-aligned to the input clock pin. The external clock output pin has a phase delay relative to the clock input pin if connected in this mode.
- No compensation: In this mode, the PLL does not compensate for any clock networks or external clock outputs.

Table 1–7 shows which modes are supported by which PLL type.

Table 1–7. Clock Feedback Mode Availability

Clock Feedback Mode	Mode Available in	
	Enhanced PLLs	Fast PLLs
No compensation mode	Yes	Yes
Normal Mode	Yes	Yes
Zero delay buffer mode	Yes	No
External feedback mode	Yes	No

Phase Shifting

Stratix and Stratix GX device enhanced PLLs provide advanced programmable phase shifting. You set these parameters in the Quartus II software.

Phase Delay

The Quartus II software automatically sets the phase taps and counter settings according to the phase shift entry. You enter a desired phase shift and the Quartus II software automatically sets the closest setting achievable. This type of phase shift is not reconfigurable during system operation. For phase shifting, enter a phase shift (in degrees or time units) for each PLL clock output port or for all outputs together in one shift.

You can select phase-shifting values in time units with a resolution of 156.25 to 416.66 ps. This resolution is a function of frequency input and the multiplication and division factors (that is, it is a function of the VCO period), with the finest step being equal to an eighth (×0.125) of the VCO period. Each clock output counter can choose a different phase of the VCO period from up to eight taps for individual fine-step selection. Also, each clock output counter can use a unique initial count setting to achieve individual coarse-shift selection in steps of one VCO period. The combination of coarse and fine shifts allows phase shifting for the entire input clock period.

The equation to determine the precision of the phase shifting in degrees is: 45° ÷ post-scale counter value. Therefore, the maximum step size is 45°, and smaller steps are possible depending on the multiplication and division ratio necessary on the output counter port.

This type of phase shift provides the highest precision since it is the least sensitive to process, supply, and temperature variation.

Lock Detect

The lock output indicates that there is a stable clock output signal in phase with the reference clock. Without any additional circuitry, the lock signal may toggle as the PLL begins tracking the reference clock. You may need to gate the lock signal for use as a system control. The lock signal from the locked port can drive the logic array or an output pin.

Whenever the PLL loses lock for any reason (be it excessive `inclk` jitter, clock switchover, PLL reconfiguration, power supply noise, etc.), the PLL must be reset with the `areset` signal to guarantee correct phase relationship between the PLL output clocks. If the phase relationship between the input clock versus output clock, and between different output clocks from the PLL is not important in your design, the PLL need not be reset.

See the *Stratix FPGA Errata Sheet* for more information on implementing the gated lock signal in your design.

Programmable Duty Cycle

The programmable duty cycle allows enhanced PLLs to generate clock outputs with a variable duty cycle. This feature is supported on each enhanced PLL post-scale counter (*g*0..*g*3, *l*0..*l*3, *e*0..*e*3). The duty cycle setting is achieved by a low and high time count setting for the post-scale counters. The Quartus II software uses the frequency input and the required multiply or divide rate to determine the duty cycle choices. The precision of the duty cycle is determined by the post-scale counter value chosen on an output. The precision is defined by 50% divided by the post-scale counter value. The closest value to 100% is not achievable for a given counter value. For example, if the *g*0 counter is 10, then steps of 5% are possible for duty cycle choices between 5 to 90%.

If the device uses external feedback, you must set the duty cycle for the counter driving off the device to 50%.

General Advanced Clear & Enable Control

There are several control signals for clearing and enabling PLLs and PLL outputs. You can use these signals to control PLL resynchronization and gate PLL output clocks for low-power applications.

The `pllenable` pin is a dedicated pin that enables/disables PLLs. When the `pllenable` pin is low, the clock output ports are driven by `GND` and all the PLLs go out of lock. When the `pllenable` pin goes high again, the PLLs relock and resynchronize to the input clocks. You can choose which PLLs are controlled by the `pllenable` signal by connecting the `pllenable` input port of the `altpll` megafunction to the common `pllenable` input pin.

The `areset` signals are reset/resynchronization inputs for each PLL. The `areset` signal should be asserted every time the PLL loses lock to guarantee correct phase relationship between the PLL output clocks. Users should include the `areset` signal in designs if any of the following conditions are true:

- PLL reconfiguration or clock switchover enables in the design
- Phase relationships between output clocks need to be maintained after a loss of lock condition

The device input pins or logic elements (LEs) can drive these input signals. When driven high, the PLL counters reset, clearing the PLL output and placing the PLL out of lock. The VCO sets back to its nominal setting (~700 MHz). When driven low again, the PLL resynchronizes to its input as it relocks. If the target VCO frequency is below this nominal

frequency, then the output frequency starts at a higher value than desired as the PLL locks. If the system cannot tolerate this, the clkena signal can disable the output clocks until the PLL locks.

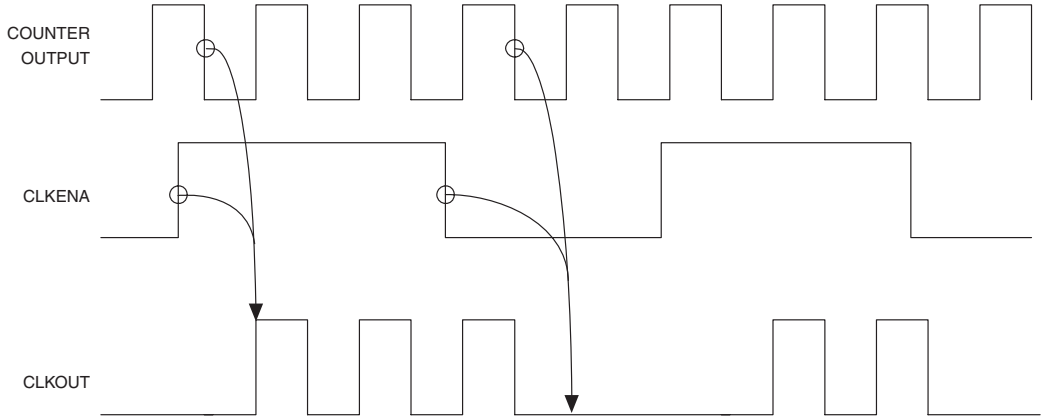
The pfdena signals control the phase frequency detector (PFD) output with a programmable gate. If you disable the PFD, the VCO operates at its last set value of control voltage and frequency with some long-term drift to a lower frequency. The system continues running when the PLL goes out of lock or the input clock is disabled. By maintaining the last locked frequency, the system has time to store its current settings before shutting down. You can either use your own control signal or a clkloss status signal to trigger pdfena.

The clkena signals control the enhanced PLL regional and global outputs. Each regional and global output port has its own clkena signal. The clkena signals synchronously disable or enable the clock at the PLL output port by gating the outputs of the *g* and *l* counters. The clkena signals are registered on the falling edge of the counter output clock to enable or disable the clock without glitches.

Figure 1–7 shows the waveform example for a PLL clock port enable. The PLL can remain locked independent of the clkena signals since the loop-related counters are not affected. This feature is useful for applications that require a low power or sleep mode. Upon re-enabling, the PLL does not need a resynchronization or relock period. The clkena signal can also disable clock outputs if the system is not tolerant to frequency overshoot during resynchronization.

The extclkena signals work in the same way as the clkena signals, but they control the external clock output counters (*e*0, *e*1, *e*2, and *e*3). Upon re-enabling, the PLL does not need a resynchronization or relock period unless the PLL is using external feedback mode. In order to lock in external feedback mode, the external output must drive the board trace back to the FBIN pin.

Figure 1–7. extclkena Signals



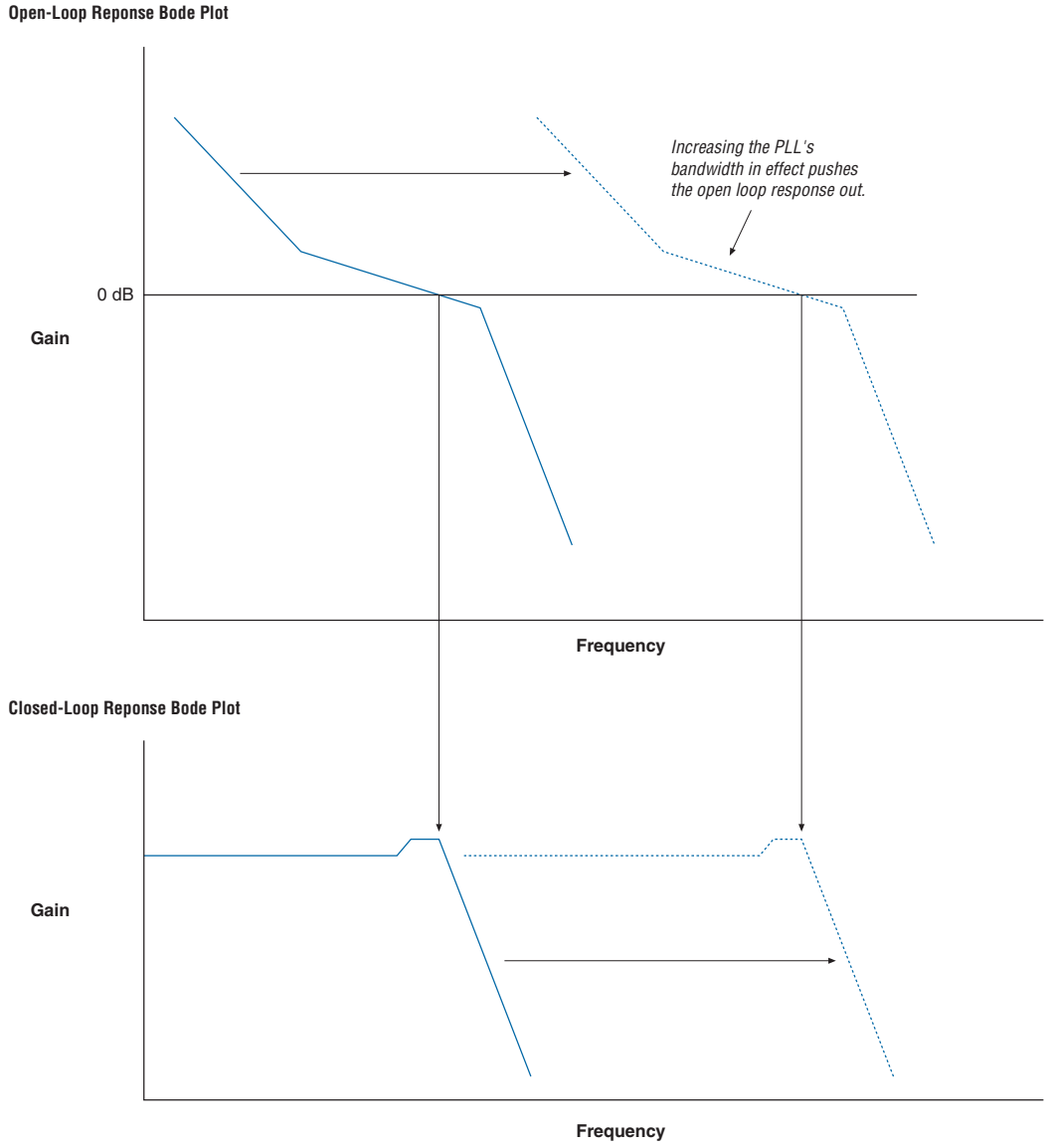
Programmable Bandwidth

Enhanced PLLs provide advanced control of the PLL bandwidth using the programmable characteristics of the PLL loop, including loop filter and charge pump.

Background

The PLL bandwidth is the measure of the PLLs ability to track the input clock and jitter. It is determined by the -3-dB frequency of the closed-loop gain in the PLL or approximately the unity gain point for open loop PLL response. As Figure 1–8 shows, these points correspond to approximately the same frequency.

Figure 1–8. Open- & Closed-Loop Response Bode Plots



A high-bandwidth PLL provides a fast lock time and tracks jitter on the reference clock source, passing it through to the PLL output. A low-bandwidth PLL filters out reference clock jitter, but increases lock time. Stratix device enhanced PLLs allow you to control the bandwidth over a

finite range to customize the PLL characteristics for a particular application. Applications that require clock switchover (such as TDMA, frequency hopping wireless, and redundant clocking) can benefit from the programmable bandwidth feature of the Stratix and Stratix GX PLLs.

The bandwidth and stability of such a system is determined by a number of factors including the charge pump current, the loop filter resistor value, the high-frequency capacitor value (in the loop filter), and the *m*-counter value. You can use the Quartus II software to control these factors and to set the bandwidth to the desired value within a given range.

You can set the bandwidth to the appropriate value to balance the need for jitter filtering and lock time. Figures 1–9 and 1–10 show the output of a low- and high-bandwidth PLL, respectively, as it locks onto the input clock.

Figure 1–9. Low-Bandwidth PLL Lock Time

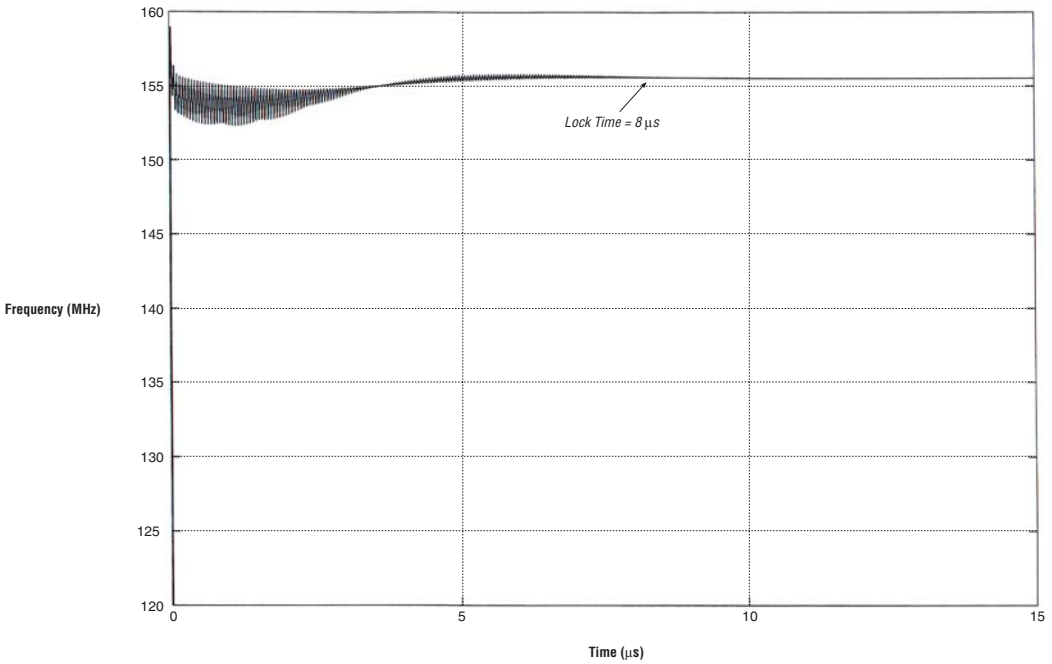
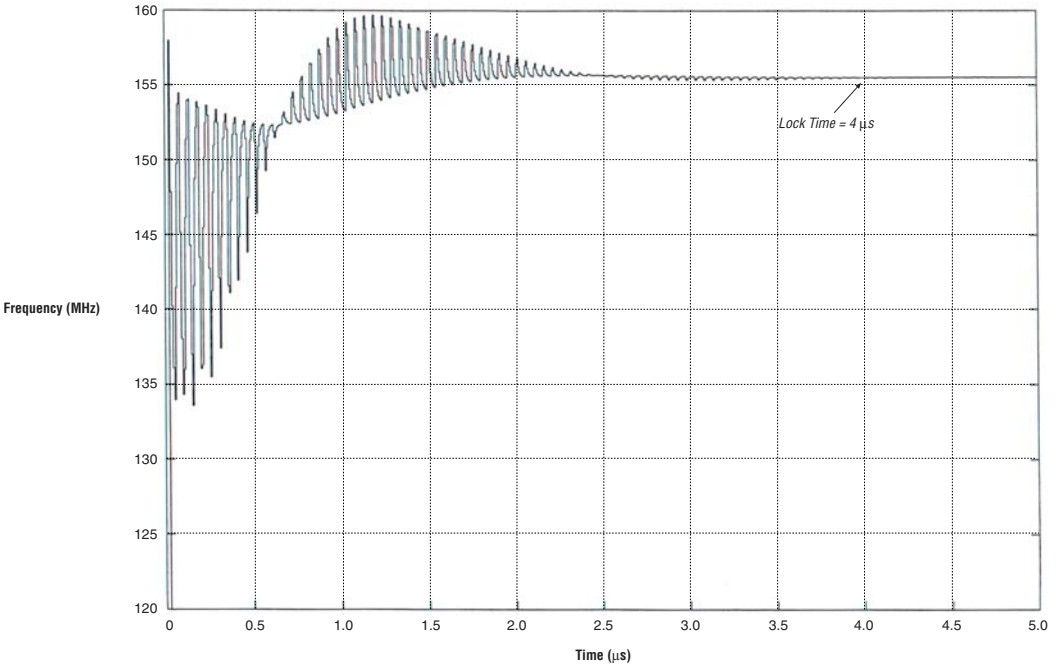


Figure 1–10. High-Bandwidth PLL Lock Time



A high-bandwidth PLL may benefit a system with two cascaded PLLs. If the first PLL uses spread spectrum (as user-induced jitter), the second PLL needs a high bandwidth so it can track the jitter that is feeding it. A low-bandwidth PLL may, in this case, lose lock due to the spread spectrum-induced jitter on the input clock.

A low-bandwidth PLL may benefit a system using clock switchover. When the clock switchover happens, the PLL input temporarily stops. A low-bandwidth PLL would react more slowly to changes to its input clock and take longer to drift to a lower frequency (caused by the input stopping) than a high-bandwidth PLL. Figures 1–11 and 1–12 demonstrate this property.

The two plots show the effects of clock switchover with a low- or high-bandwidth PLL. When the clock switchover happens, the output of the low-bandwidth PLL (see Figure 1–11) drifts to lower frequency much slower than the high-bandwidth PLL output (see Figures 1–12).

Figure 1–11. Effect of Low Bandwidth on Clock Switchover

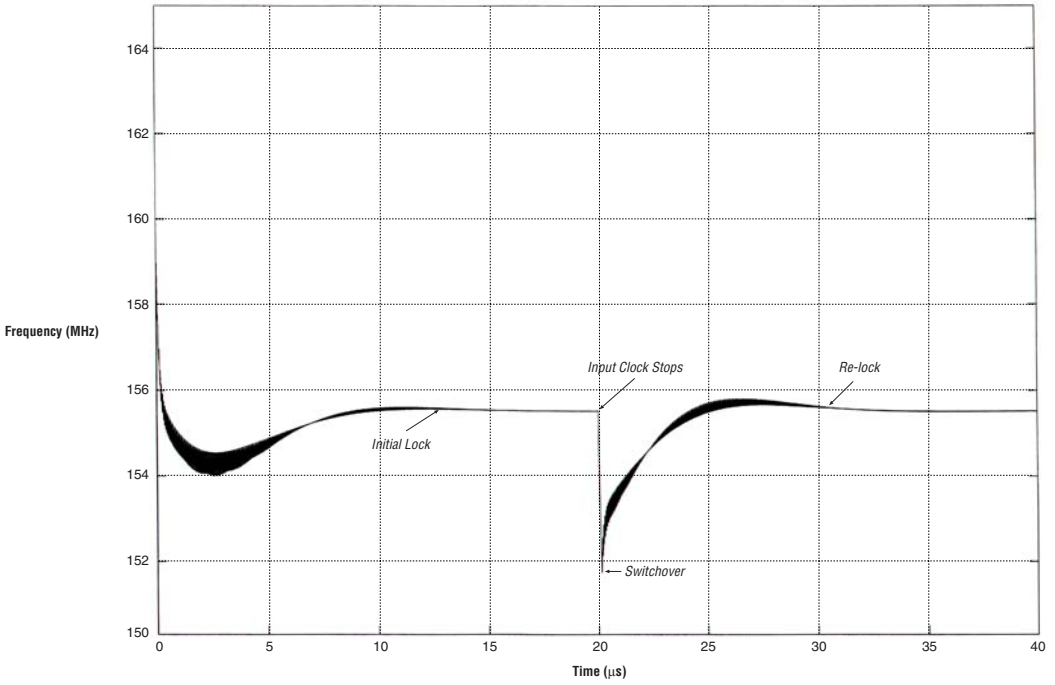
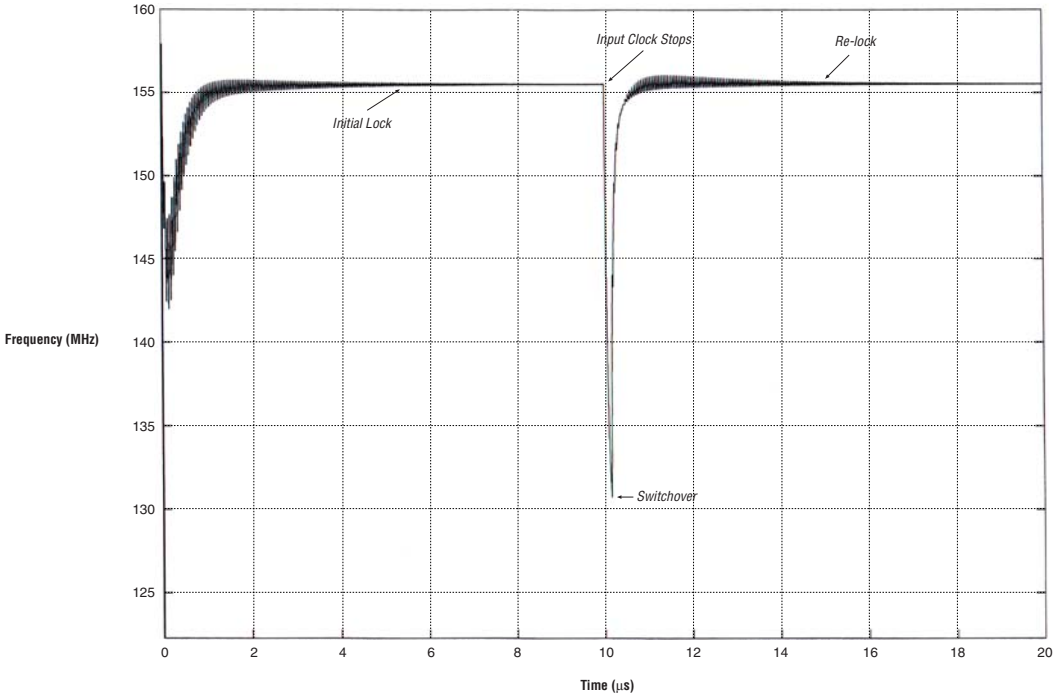


Figure 1–12. Effect of High Bandwidth on Clock Switchover



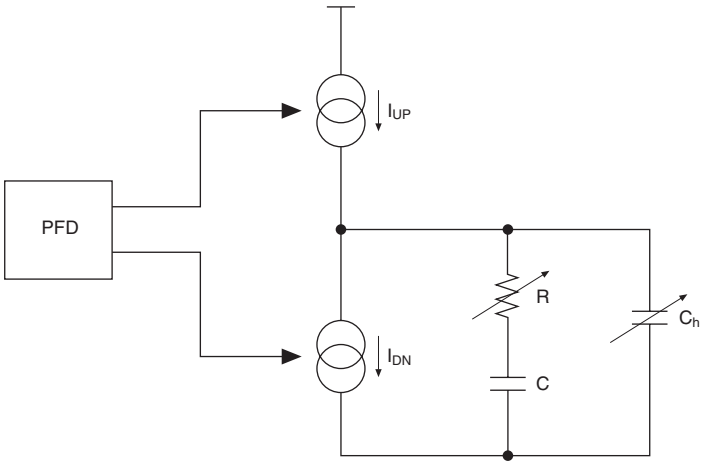
Implementation

Traditionally, external components such as the VCO or loop filter control a PLL's bandwidth. Most loop filters are made up of passive components, such as resistors and capacitors, which take up unnecessary board space and increase cost. With Stratix and Stratix GX device enhanced PLLs, all the components are contained within the device to increase performance and decrease cost.

Stratix and Stratix GX device enhanced PLLs implement programmable bandwidth by giving you control of the charge pump current and loop filter resistor (R) and high-frequency capacitor (C_h) values (see Table 1–8). The Stratix and Stratix GX device enhanced PLL bandwidth ranges from approximately 150 kHz to 2 MHz.

The charge pump current directly affects the PLL bandwidth. The higher the charge pump current, the higher the PLL bandwidth. You can choose from a fixed set of values for the charge pump current. Figure 1–13 shows the loop filter and the components that you can set via the Quartus II software.

Figure 1–13. Loop Filter Programmable Components



Software Support

The Quartus II software provides two levels of programmable bandwidth control. The first level allows you to enter a value for the desired bandwidth directly into the Quartus II software using the MegaWizard® Plug-In Manager. Alternatively, you can set the `bandwidth` parameter in the `altpll` function to the desired bandwidth. The Quartus II software then chooses each individual bandwidth parameter to achieve the desired setting. If designs cannot achieve the desired bandwidth setting, the Quartus II software selects the closest achievable value. For preset low, medium, and high bandwidth settings, the Quartus II software sets the bandwidth as follows:

- Low bandwidth is set at 150 KHz
- Medium bandwidth is set at 800 KHz
- High bandwidth is set at 2 Mhz

If you choose Auto bandwidth, the Quartus II software chooses the PLL settings and you can get a bandwidth setting outside the 150-Khz to 2-Mhz range.

An advanced level of control is also possible for precise control of the loop filter parameters. This level allows you to specifically select the charge pump current, loop filter resistor value, and loop filter (high frequency) capacitor value. These parameters are: charge_pump_current, loop_filter_r, and loop_filter_c. Each parameter supports the specific range of values listed in Table 1–8.

Table 1–8. Advanced Loop Filter Parameters

Parameter	Values
Resistor values (kΩ)	1, 2, 3, 4, 7, 8, 9, 10
High-frequency capacitance values (pF)	5, 10, 15, 20
Charge pump current settings (µA)	10, 15, 20, 24, 30, 35, 40, 45, 50, 55, 60, 65, 70, 75, 80, 85, 90, 100, 112, 135, 148, 164, 212

For more information on PLL software support in the Quartus II software, see the *altpll Megafunction User Guide*.

Clock Switchover

For more information on implementing clock switchover, see *AN 313: Implementing Clock Switchover in Stratix & Stratix GX Devices.*

Spread-Spectrum Clocking

Digital clocks are generally square waves with short rise times and a 50% duty cycle. These high-speed digital clocks concentrate a significant amount of energy in a narrow bandwidth at the target frequency and at the higher frequency harmonics. This results in high energy peaks and increased electromagnetic interference (EMI). The radiated noise from the energy peaks travels in free air and, if not minimized, can lead to corrupted data and intermittent system errors, which can jeopardize system reliability.

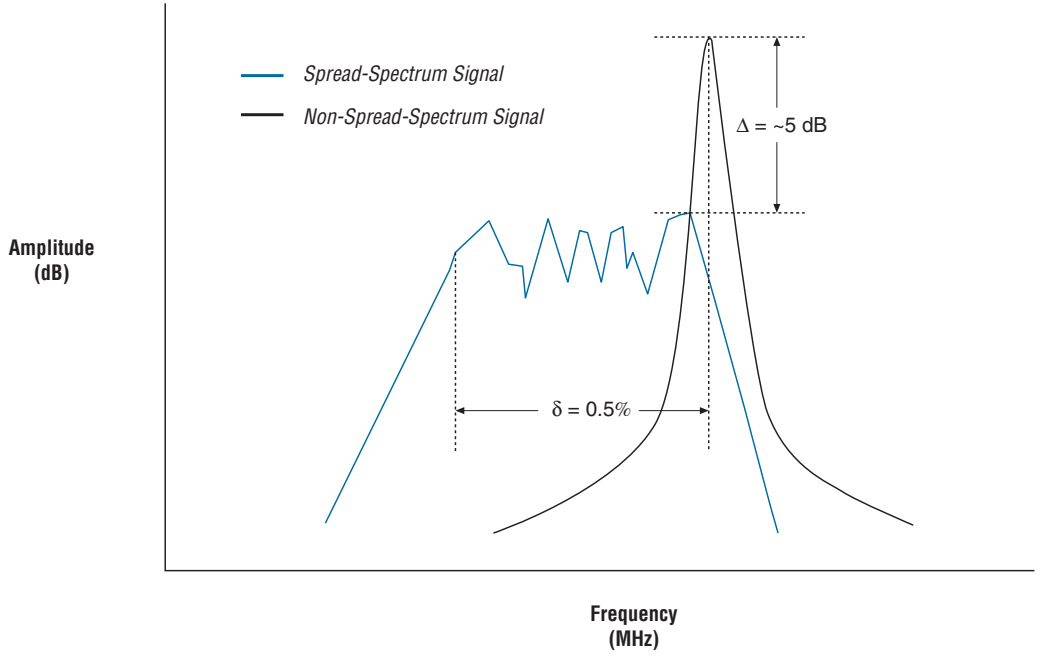
Background

Traditional methods for limiting EMI include shielding, filtering, and multi-layer printed circuit boards (PCBs). However, these methods significantly increase the overall system cost and sometimes are not enough to meet EMI compliance. Spread-spectrum technology provides a simple and effective technique for reducing EMI emissions without additional cost and the trouble of re-designing a board.

Spread-spectrum technology modulates the target frequency over a small range. For example, if a 100-MHz signal has a 0.5% down-spread modulation, then the frequency is swept from 99.5 to 100 MHz. Figure 1–14 gives a graphical representation of the energy present in a spread-spectrum signal as opposed to a non-spread-spectrum signal. It is apparent that instead of concentrating the energy at the target frequency, the energy is re-distributed across a wider band of frequencies, which reduces peak energy.

Not only is there a reduction in the fundamental peak EMI components, but there is also a reduction in EMI of the higher order harmonics. Since some regulations focus on peak EMI emissions, rather than average EMI emissions, spread-spectrum technology is a valuable method of EMI reduction.

Figure 1–14. Spread-Spectrum Signal Energy versus Non-Spread-Spectrum Signal Energy



Spread-spectrum technology would benefit a design with high EMI emissions and/or strict EMI requirements. Device-generated EMI is dependent on frequency, output voltage swing amplitude, and slew rate. For example, a design using LVDS already has low EMI emissions

because of the low-voltage swing. The differential LVDS signal also allows for EMI rejection within the signal. Therefore, this situation may not require spread-spectrum technology.

Description

Stratix and Stratix GX device enhanced PLLs feature spread-spectrum technology to reduce the EMI emitted from the device. The enhanced PLL provides up to a 0.5% down spread (–0.5%) using a triangular, also known as linear, modulation profile. The modulation frequency is programmable and ranges from approximately 30 to 150 kHz. The spread percentage is based on the clock input to the PLL and the *m* and *n* settings. Spread-spectrum technology reduces the peak energy by 2 to 5 dB at the target frequency. However, this number is dependent on bandwidth and the *m* and *n* counter values and can vary from design to design.

Spread percentage, also known as modulation width, is defined as the percentage that the design modulates the target frequency. A negative (–) percentage indicates a down spread, a positive (+) percentage indicates an up spread, and a (±) indicates a center spread. Modulation frequency is the frequency of the spreading signal or how fast the signal sweeps from the minimum to the maximum frequency. Down-spread modulation shifts the target frequency down by half the spread percentage, centering the modulated waveforms on a new target frequency.

The *m* and *n* counter values are toggled at the same time between two fixed values. The loop filter then slowly changes the VCO frequency to provide the spreading effect, which results in a triangular modulation. An additional spread-spectrum counter (shown in Figure 1–15) sets the modulation frequency. Figure 1–15 shows how spread-spectrum technology is implemented in the Stratix device enhanced PLL.

Figure 1–15. Spread-Spectrum Circuit Block Diagram

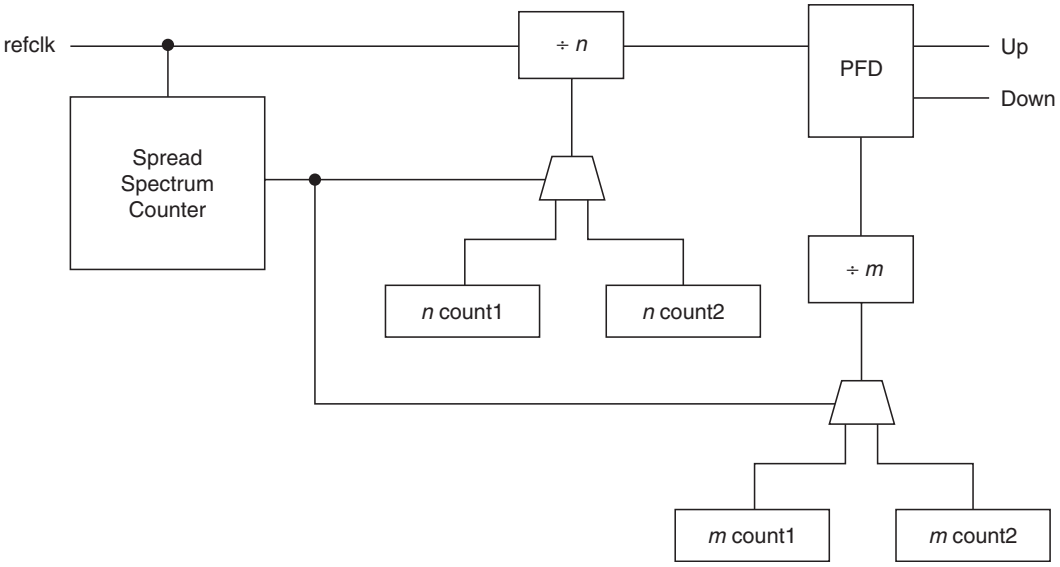


Figure 1–16 shows a VCO frequency waveform when toggling between different counter values. Since the enhanced PLL switches between two different m and n values, the result is a straight line between two frequencies, which gives a linear modulation. The magnitude of modulation is determined by the ratio of two m/n sets. The percent spread is determined by:

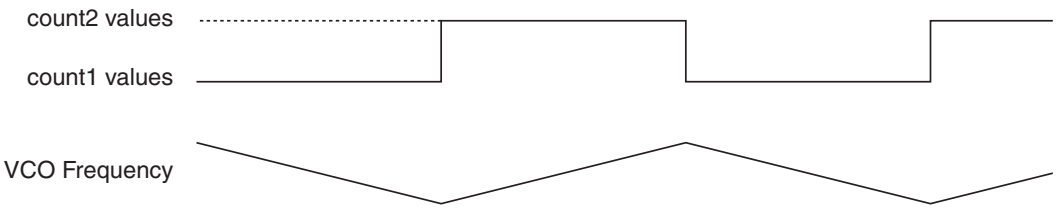
$$\text{percent spread} = (f_{VCOmax} - f_{VCOmin})/f_{VCOmax} = 1 - [(m_2 \times n_1)/(m_1 \times n_2)]$$

The maximum and minimum VCO frequency is defined as:

$$f_{VCOmax} = (m_1/n_1) \times f_{ref}$$

$$f_{VCOmin} = (m_2/n_2) \times f_{ref}$$

Figure 1–16. VCO Frequency Modulation Waveforms



Software Support

You can enter the desired down-spread percentage and modulation frequency in the MegaWizard Plug-In Manager through the Quartus II software. Alternatively, the MegaWizard Plug-In Manager can set the `downspread` parameter in the `altpll` megafunction to the desired down-spread percentage. Timing analysis ensures the design operates at the maximum spread frequency and meets all timing requirements.

For more information on PLL software support in the Quartus II software, see the *altpll Megafunction User Guide*.

Guidelines

If the design cascades PLLs, the source, or upstream PLL should have a low bandwidth setting, while the destination, or downstream PLL should have a high bandwidth setting. The upstream PLL must have a low bandwidth setting because a PLL does not generate jitter higher than its bandwidth. The downstream PLL must have a high bandwidth setting to track the jitter. The design must use the spread-spectrum feature in a low-bandwidth PLL and, therefore, the Quartus II software automatically sets the spread-spectrum PLL's bandwidth to low.

Designs cannot use spread-spectrum PLLs with the programmable bandwidth feature.

Stratix and Stratix GX devices can accept a spread-spectrum input with typical modulation frequencies. However, the device cannot automatically detect that the input is a spread-spectrum signal. Instead, the input signal looks like deterministic jitter at the input of the downstream PLL.

Spread spectrum should only have a minor effect on period jitter, but period jitter increases. Period jitter is the deviation of a clock's cycle time from its previous cycle position. Period jitter measures the variation of a clock's output transition from its ideal position over consecutive edges.

With down-spread modulation, the peak of the modulated waveform is the actual target frequency. Therefore, the system never exceeds the maximum clock speed. To maintain reliable communication, the entire system/subsystem should use the Stratix or Stratix GX device as the clock source. Communication could fail if the Stratix or Stratix GX logic array is clocked by the spread-spectrum clock, but the data it receives from another device is not.

Since spread spectrum affects the *m* counter values, all spread-spectrum PLL outputs are affected. Therefore, if only one spread-spectrum signal is needed, the clock signal should use a separate PLL without other outputs from that PLL.

No special considerations are needed when using spread spectrum with the clock switchover feature. This is because the clock switchover feature does not affect the *m* and *n* counter values, which are the counter values that are switching when using spread spectrum.

PLL Reconfiguration

See *AN 282: Implementing PLL Reconfiguration in Stratix & Stratix GX Devices* for information on PLL reconfiguration.

Enhanced PLL Pins

Table 1–9 shows the physical pins and their purpose for the Enhanced PLLs. For `inclk` port connections to pins see "Clocking" on page 1–39.

Table 1–9. Enhanced PLL Pins (Part 1 of 2)

Pin	Description
CLK4p/n	Single-ended or differential pins that can drive the `inclk` port for PLL 6.
CLK5p/n	Single-ended or differential pins that can drive the `inclk` port for PLL 6.
CLK6p/n	Single-ended or differential pins that can drive the `inclk` port for PLL 12.
CLK7p/n	Single-ended or differential pins that can drive the `inclk` port for PLL 12.
CLK12p/n	Single-ended or differential pins that can drive the `inclk` port for PLL 11.
CLK13p/n	Single-ended or differential pins that can drive the `inclk` port for PLL 11.
CLK14p/n	Single-ended or differential pins that can drive the `inclk` port for PLL 5.
CLK15p/n	Single-ended or differential pins that can drive the `inclk` port for PLL 5.
PLL5_FBp/n	Single-ended or differential pins that can drive the `fbin` port for PLL 5.
PLL6_FBp/n	Single-ended or differential pins that can drive the `fbin` port for PLL 6.
PLLENABLE	Dedicated input pin that drives the `pllena` port of all or a set of PLLs. If you do not use this pin, connect it to ground.

Table 1–9. Enhanced PLL Pins (Part 2 of 2)

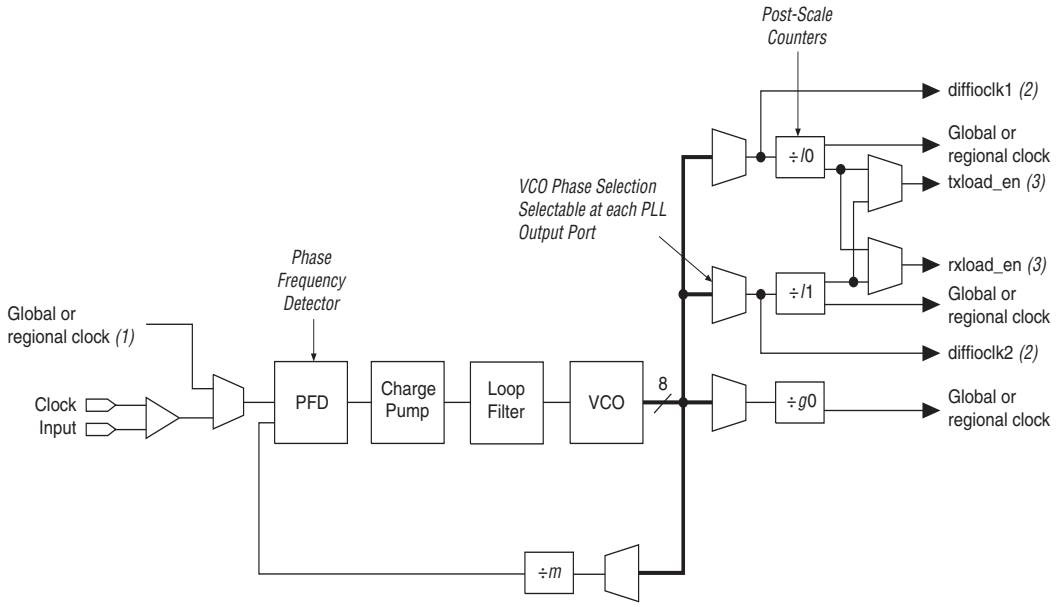
Pin	Description
PLL5_OUT[3..0]p/n	Single-ended or differential pins driven by extclk[3..0] ports from PLL 5.
PLL6_OUT[3..0]p/n	Single-ended or differential pins driven by extclk[3..0] ports from PLL 6.
PLL11_OUT, CLK13n	Single-ended output pin driven by clk0 port from PLL 11.
PLL12_OUT, CLK6n	Single-ended output pin driven by clk0 port from PLL 12.
VCCA_PLL5	Analog power for PLL 5. Connect this pin to 1.5 V, even if the PLL is not used.
VCCG_PLL5	Guard ring power for PLL 5. Connect this pin to 1.5 V, even if the PLL is not used.
GNDA_PLL5	Analog ground for PLL 5. You can connect this pin to the GND plane on the board.
GNDG_PLL5	Guard ring ground for PLL 5. You can connect this pin to the GND plane on the board.
VCCA_PLL6	Analog power for PLL 6. Connect this pin to 1.5 V, even if the PLL is not used.
VCCG_PLL6	Guard ring power for PLL 6. Connect this pin to 1.5 V, even if the PLL is not used.
GNDA_PLL6	Analog ground for PLL 6. You can connect this pin to the GND plane on the board.
GNDG_PLL6	Guard ring ground for PLL 6. You can connect this pin to the GND plane on the board.
VCCA_PLL11	Analog power for PLL 11. Connect this pin to 1.5 V, even if the PLL is not used.
VCCG_PLL11	Guard ring power for PLL 11. Connect this pin to 1.5 V, even if the PLL is not used.
GNDA_PLL11	Analog ground for PLL 11. You can connect this pin to the GND plane on the board.
GNDG_PLL11	Guard ring ground for PLL 11.You can connect this pin to the GND plane on the board.
VCCA_PLL12	Analog power for PLL 12. Connect this pin to 1.5 V, even if the PLL is not used.
VCCG_PLL12	Guard ring power for PLL 12. Connect this pin to 1.5 V, even if the PLL is not used.
GNDA_PLL12	Analog ground for PLL 12. You can connect this pin to the GND plane on the board.
GNDG_PLL12	Guard ring ground for PLL 12. You can connect this pin to the GND plane on the board.
VCC_PLL5_OUTA	External clock output V_{CCIO} power for PLL5_OUT0p, PLL5_OUT0n, PLL5_OUT1p, and PLL5_OUT1n outputs from PLL 5.
VCC_PLL5_OUTB	External clock output V_{CCIO} power for PLL5_OUT2p, PLL5_OUT2n, PLL5_OUT3p, and PLL5_OUT3n outputs from PLL 5.
VCC_PLL6_OUTA	External clock output V_{CCIO} power for PLL5_OUT0p, PLL5_OUT0n, PLL5_OUT1p, and PLL5_OUT1n outputs from PLL 6.
VCC_PLL6_OUTB	External clock output V_{CCIO} power for PLL5_OUT2p, PLL5_OUT2n, PLL5_OUT3p, and PLL5_OUT3n outputs from PLL 6.

Fast PLLs

Stratix devices contain up to eight fast PLLs and Stratix GX devices contain up to four fast PLLs. Both device PLLs have high-speed differential I/O interface ability along with general-purpose features. Figure 1–17 shows a diagram of the fast PLL. This section discusses the

general purpose abilities of the Fast PLL. For information on the high-speed differential I/O interface capabilities, see the *High-Speed Differential I/O Interfaces in Stratix Devices* chapter.

Figure 1–17. Stratix & Stratix GX Fast PLL Block Diagram



Notes to Figure 1–17:

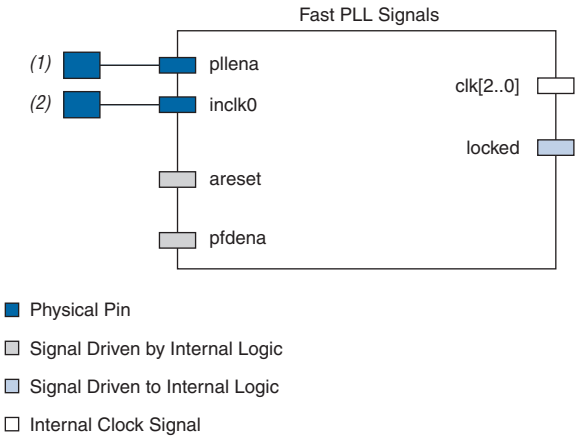
(1) The global or regional clock input can be driven by an output from another PLL or any dedicated CLK or FCLK pin. It cannot be driven by internally-generated global signals.

(2) In high-speed differential I/O support mode, this high-speed PLL clock feeds the SERDES. Stratix and Stratix GX devices only support one rate of data transfer per fast PLL in high-speed differential I/O support mode.

(3) This signal is a high-speed differential I/O support SERDES control signal.

Figure 1–18 shows all possible ports related to fast PLLs.

Figure 1–18. Fast PLL Ports & Physical Destinations



Notes to Figure 1–18:
(1) This input pin is shared by all enhanced and fast PLLs.
(2) This input pin is either single-ended or differential.

Tables 1–10 and 1–11 show the description of all fast PLL ports.

Table 1–10. Fast PLL Input Signals

Name	Description	Source	Destination
inclk1	Reference clock input to PLL	Pin	PFD
pllena	Enable pin for enabling or disabling all or a set of PLLs – active high	Pin	PLL control signal
areset	Signal used to reset the PLL which re-synchronizes all the counter outputs—active high	Logic array	PLL control signal
pfdena	Enables the up/down outputs from the phase-frequency detector—active high	Logic array	PFD

Table 1–11. Fast PLL Output Signals

Name	Description	Source	Destination
clk[2..0]	PLL outputs driving regional or global clock	PLL counter	Internal clock
locked	Lock output from lock detect circuit—active high	PLL lock detect	Logic array

Clock Multiplication & Division

Stratix and Stratix GX device fast PLLs provide clock synthesis for PLL output ports using *m*/(post scaler) scaling factors. The input clock is multiplied by the *m* feedback factor. Each output port has a unique post scale counter to divide down the high-frequency VCO. There is one multiply counter, *m*, per fast PLL with a range of 1 to 32. There are three post-scale counters (*g*0, *l*0, and *l*1) for the regional and global clock output ports. All post-scale counters range from 1 to 32. If the design uses a high-speed serial interface, you can set the output counter to 1 to allow the high-speed VCO frequency to drive the SERDES.

External Clock Outputs

Each fast PLL supports differential or single-ended outputs for source-synchronous transmitters or for general-purpose external clocks. There are no dedicated external clock output pins. The fast PLL global or regional outputs can drive any I/O pin as an external clock output pin. The I/O standards supported by any particular bank determines what standards are possible for an external clock output driven by the fast PLL in that bank. See the *Selectable I/O Standards in Stratix & Stratix GX Devices* chapter in the *Stratix Device Handbook, Volume 2* or the *Stratix GX Device Handbook, Volume 2* for output standard support.

Table 1–12 shows the I/O standards supported by fast PLL input pins.

Table 1–12. Fast PLL Port I/O Standards (Part 1 of 2)

I/O Standard	Input	
	INCLK	PLLENABLE
LVTTL	✓	✓
LVCMOS	✓	✓
2.5 V	✓	
1.8 V	✓	
1.5 V	✓	
3.3-V PCI		
3.3-V PCI-X 1.0		
LVPECL	✓	
PCML	✓	
LVDS	✓	
HyperTransport technology	✓	
Differential HSTL	✓	

Table 1–12. Fast PLL Port I/O Standards (Part 2 of 2)

I/O Standard	Input	
	INCLK	PLLENABLE
Differential SSTL		
3.3-V GTL		
3.3-V GTL+	✓	
1.5-V HSTL Class I	✓	
1.5-V HSTL Class II		
1.8-V HSTL Class I	✓	
1.8-V HSTL Class II		
SSTL-18 Class I	✓	
SSTL-18 Class II		
SSTL-2 Class I	✓	
SSTL-2 Class II	✓	
SSTL-3 Class I	✓	
SSTL-3 Class II	✓	
AGP (1× and 2×)		
CTT	✓	

Phase Shifting

Stratix and Stratix GX device fast PLLs have advanced clock shift ability to provide programmable phase shift. These parameters are set in the Quartus II software.

The Quartus II software automatically sets the phase taps and counter settings according to the phase shift entry. Enter a desired phase shift and the Quartus II software automatically sets the closest setting achievable. This type of phase shift is not reconfigurable during system operation. You can enter a phase shift (in degrees or time units) for each PLL clock output port or for all outputs together in one shift. You can perform phase shifting in time units with a resolution range of 125 to 416.66 ps to create a function of frequency input and the multiplication and division factors (that is, it is a function of the VCO period), with the finest step being equal to an eighth (×0.125) of the VCO period. Each clock output counter can choose a different phase of the VCO period from up to eight taps for individual fine-step selection. Also, each clock output counter can use a unique initial count setting to achieve individual coarse shift selection in steps of one VCO period. The combination of coarse and grain shifts allows phase shifting for the entire input clock period.

The equation to determine the precision of phase in degrees is: 45° ÷ post-scale counter value. Therefore, the maximum step size is 45°, and smaller steps are possible depending on the multiplication and division ratio necessary on the output counter port.

This type of phase shift provides the highest precision since it is the least sensitive to process, supply, and temperature variation.

Programmable Duty Cycle

The programmable duty cycle allows the fast PLL to generate clock outputs with a variable duty cycle. This feature is supported on each fast PLL post-scale counter. *g*0, *l*0, and *l*1 all support programmable duty. You use a low- and high-time count setting for the post-scale counters to set the duty cycle.

The Quartus II software uses the frequency input and multiply/divide rate desired to select the post-scale counter, which determines the possible choices for each duty cycle. The precision of the duty cycle is determined by the post-scale counter value chosen on an output. The precision is defined by 50% divided by the post-scale counter value. The closest value to 100% is not achievable for a given counter value. For example, if the *g*0 counter is 10, then steps of 5% are possible for duty cycle choices between 5 to 90%.

If the device uses external feedback, you must set the duty cycle for the counter driving off the device to 50%.

Control Signals

The lock output indicates a stable clock output signal in phase with the reference clock. Unlike enhanced PLLs, fast PLLs do not have a lock filter counter.

The `pllenable` pin is a dedicated pin that enables/disables both PLLs. When the `pllenable` pin is low, the clock output ports are driven by `GND` and all the PLLs go out of lock. When the `pllenable` pin goes high again, the PLLs relock and resynchronize to the input clocks. You can choose which PLLs are controlled by the `pllenable` by connecting the `pllenable` input port of the `altpll` megafunction to the common `pllenable` input pin.

The `areset` signals are reset/resynchronization inputs for each fast PLL. The Stratix and Stratix GX devices can drive these input signals from an input pin or from LEs. When driven high, the PLL counters reset, clearing the PLL output and placing the PLL out of lock. The VCO sets back to its nominal setting (~700 MHz). When driven low again, the PLL

resynchronizes to its input clock as it relocks. If the target VCO frequency is below this nominal frequency, then the output frequency starts at a higher value then desired as it locks.

The pfdena signals control the PFD output with a programmable gate. If you disable the PFD, the VCO operates at its last set value of control voltage and frequency with some long-term drift to a lower frequency. The system continues running when the PLL goes out of lock or the input clock disables. By maintaining the last locked frequency, the system has time to store its current settings before shutting down.

If the PLL loses lock for any reason (for example, because of excessive inclk jitter, clock switchover, PLL reconfiguration, or power supply noise), the PLL must be reset with the areset signal to guarantee correct phase relationship between the PLL output clocks. If the phase relationship between the input clock and the output clock and between different output clocks from the PLL is not important in your design, it is not necessary to reset the PLL.

Pins

Table 1–13 shows the physical pins and their purpose for the Fast PLLs. For inclk port connections to pins see "Clocking" on page 1–39.

Table 1–13. Fast PLL Pins (Part 1 of 3)

Pin	Description
CLK0p/n	Single-ended or differential pins that can drive the inclk port for PLL 1 or 7.
CLK1p/n	Single-ended or differential pins that can drive the inclk port for PLL 1.
CLK2p/n	Single-ended or differential pins that can drive the inclk port for PLL 2 or 8.
CLK3p/n	Single-ended or differential pins that can drive the inclk port for PLL 2.
CLK8p/n	Single-ended or differential pins that can drive the inclk port for PLL 3 or 9. *(1)*
CLK9p/n	Single-ended or differential pins that can drive the inclk port for PLL 3. *(1)*
CLK10p/n	Single-ended or differential pins that can drive the inclk port for PLL 4 or 10. *(1)*
CLK11p/n	Single-ended or differential pins that can drive the inclk port for PLL 4. *(1)*
FPLL7CLKp/n	Single-ended or differential pins that can drive the inclk port for PLL 7.
FPLL8CLKp/n	Single-ended or differential pins that can drive the inclk port for PLL 8.
FPLL9CLKp/n	Single-ended or differential pins that can drive the inclk port for PLL 9. *(1)*
FPLL10CLKp/n	Single-ended or differential pins that can drive the inclk port for PLL 10. *(1)*
PLLENABLE	Dedicated input pin that drives the pllena port of all or a set of PLLs. If you do not use this pin, connect it to ground.
VCCA_PLL1	Analog power for PLL 1. Connect this pin to 1.5 V, even if the PLL is not used.

Table 1–13. Fast PLL Pins (Part 2 of 3)

Pin	Description
VCCG_PLL1	Guard ring power for PLL 1. Connect this pin to 1.5 V, even if the PLL is not used.
GNDA_PLL1	Analog ground for PLL 1. You can connect this pin to the GND plane on the board.
GNDG_PLL1	Guard ring ground for PLL 1. You can connect this pin to the GND plane on the board.
VCCA_PLL2	Analog power for PLL 2. Connect this pin to 1.5 V, even if the PLL is not used.
VCCG_PLL2	Guard ring power for PLL 2. Connect this pin to1.5 V, even if the PLL is not used.
GNDA_PLL2	Analog ground for PLL 2. You can connect this pin to the GND plane on the board.
GNDG_PLL2	Guard ring ground for PLL 2. You can connect this pin to the GND plane on the board.
VCCA_PLL3	Analog power for PLL 3. Connect this pin to 1.5 V, even if the PLL is not used. *(1)*
VCCG_PLL3	Guard ring power for PLL 3. Connect this pin to 1.5 V, even if the PLL is not used. *(1)*
GNDA_PLL3	Analog ground for PLL 3. You can connect this pin to the GND plane on the board. *(1)*
GNDG_PLL3	Guard ring ground for PLL 3. You can connect this pin to the GND plane on the board. *(1)*
VCCA_PLL4	Analog power for PLL 4. Connect this pin to 1.5 V, even if the PLL is not used. *(1)*
VCCG_PLL4	Guard ring power for PLL 4. Connect this pin to 1.5 V, even if the PLL is not used. *(1)*
GNDA_PLL4	Analog ground for PLL 4. You can connect this pin to the GND plane on the board. *(1)*
GNDG_PLL4	Guard ring ground for PLL 4. You can connect this pin to the GND plane on the board. *(1)*
VCCA_PLL7	Analog power for PLL 7. Connect this pin to 1.5 V, even if the PLL is not used.
VCCG_PLL7	Guard ring power for PLL 7. Connect this pin to 1.5 V, even if the PLL is not used.
GNDA_PLL7	Analog ground for PLL 7. You can connect this pin to the GND plane on the board.
GNDG_PLL7	Guard ring ground for PLL 7. You can connect this pin to the GND plane on the board.
VCCA_PLL8	Analog power for PLL 8. Connect this pin to 1.5 V, even if the PLL is not used.
VCCG_PLL8	Guard ring power for PLL 8. Connect this pin to 1.5 V, even if the PLL is not used.
GNDA_PLL8	Analog ground for PLL 8. You can connect this pin to the GND plane on the board.
GNDG_PLL8	Guard ring ground for PLL 8. You can connect this pin to the GND plane on the board.
VCCA_PLL9	Analog power for PLL 9. Connect this pin to 1.5 V, even if the PLL is not used. *(1)*
VCCG_PLL9	Guard ring power for PLL 9. Connect this pin to 1.5 V, even if the PLL is not used. *(1)*

Table 1–13. Fast PLL Pins (Part 3 of 3)

Pin	Description
GNDA_PLL9	Analog ground for PLL 9. You can connect this pin to the GND plane on the board. *(1)*
GNDG_PLL9	Guard ring ground for PLL 9. You can connect this pin to the GND plane on the board. *(1)*
VCCA_PLL10	Analog power for PLL 10. Connect this pin to 1.5 V, even if the PLL is not used. *(1)*
VCCG_PLL10	Guard ring power for PLL 10. Connect this pin to 1.5 V, even if the PLL is not used. *(1)*
GNDA_PLL10	Analog ground for PLL 10. Connect this pin to the GND plane on the board. *(1)*
GNDG_PLL10	Guard ring ground for PLL 10. You can connect this pin to the GND plane on the board. *(1)*

Note to Table 1–13:

(1) PLLs 3, 4, 9, and 10 are not available on Stratix GX devices for general-purpose configuration. These PLLs are part of the HSSI block. See *AN 236: Using Source-Synchronous Signaling with DPA in Stratix GX Devices* for more information.

Clocking

Stratix and Stratix GX devices provide a hierarchical clock structure and multiple PLLs with advanced features. The large number of clocking resources in combination with the clock synthesis precision provided by enhanced and fast PLLs provides a complete clock management solution.

Global & Hierarchical Clocking

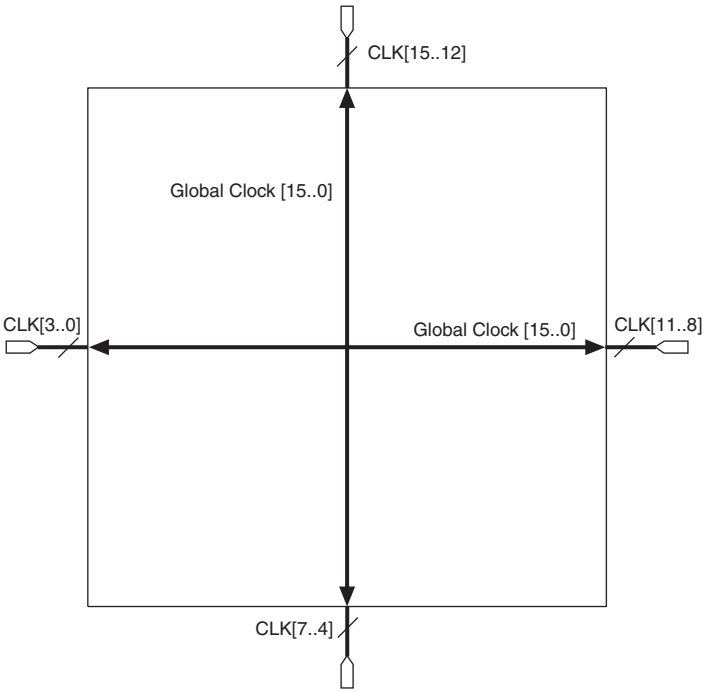
Stratix and Stratix GX devices provide 16 dedicated global clock networks, 16 regional clock networks (4 per device quadrant), and 8 dedicated fast regional clock networks. These clocks are organized into a hierarchical clock structure that allows for up to 22 clocks per device region with low skew and delay. This hierarchical clocking scheme provides up to 48 unique clock domains within Stratix and Stratix GX devices.

There are 16 dedicated clock pins (CLK[15..0]) on Stratix devices and 12 dedicated clock pins (CLK[11..0]) on Stratix GX devices to drive either the global or regional clock networks. Four clock pins drive each side of the Stratix device, as shown in Figures 1–19 and 1–20. On Stratix GX devices, four clock pins drive the top, left, and bottom sides of the device. The clocks on the right side of the device are not available for general-purpose PLLs. Enhanced and fast PLL outputs can also drive the global and regional clock networks.

Global Clock Network

These clocks drive throughout the entire device, feeding all device quadrants. All resources within the device—IOEs, LEs, DSP blocks, and all memory blocks—can use the global clock networks as clock sources. These resources can also be used for control signals, such as clock enables and synchronous or asynchronous clears fed from the external pin. Internal logic can also drive the global clock networks for internally generated global clocks and asynchronous clears, clock enables, or other control signals with large fanout. Figure 1–19 shows the 16 dedicated CLK pins driving global clock networks.

Figure 1–19. Global Clocking

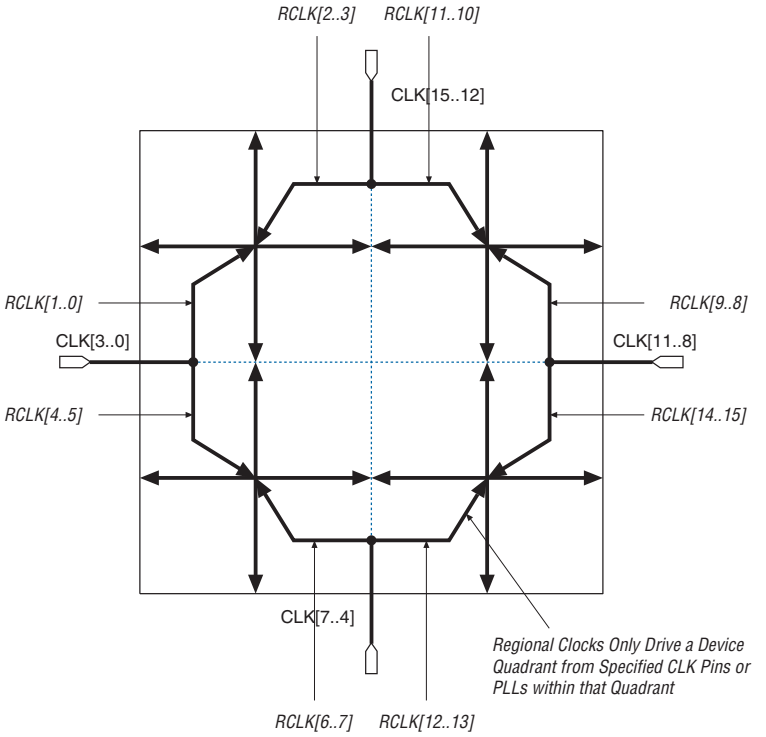


Regional Clock Network

There are four regional clock networks within each quadrant of the Stratix or Stratix GX device that are driven by the same dedicated CLK[15..0] input pins or from PLL outputs. From a top view of the silicon, RCLK[0..3] are in the top-left quadrant, RCLK[8..11] are in the top-right quadrant, RCLK[4..7] are in the bottom-left quadrant, and

RCLK[12..15] are in the bottom-right quadrant. The regional clock networks only pertain to the quadrant they drive into. The regional clock networks provide the lowest clock delay and skew for logic contained within a single quadrant. RCLK clock networks cannot be driven by internal logic. The CLK clock pins symmetrically drive the RCLK networks within a particular quadrant, as shown in Figure 1–20. See Figures 1–21 and 1–22 for RCLK connections from PLLs and CLK pins.

Figure 1–20. Regional Clocks



Clock Input Connections

Two CLK pins drive each enhanced PLL. You can use either one or both pins for clock switchover inputs into the PLL. Either pin can be the primary clock source for clock switchover, which is controlled in the Quartus II software. Enhanced PLLs 5 and 6 also have feedback input pins as shown in Table 1–14.

Input clocks for fast PLLs 1, 2, 3, and 4 come from CLK pins. Stratix GX devices use PLLs 3 and 4 in the HSSI block only. A multiplexer chooses one of two possible CLK pins to drive each PLL. This multiplexer is not a clock switchover multiplexer and is only used for clock input connectivity.

Either a FPLLCLK input pin or a CLK pin can drive the fast PLLs in the corners (7, 8, 9, and 10) when used for general purpose. CLK pins cannot drive these fast PLLs in high-speed differential I/O mode. PLLs 9 and 10 are used for the HSSI block in Stratix GX devices and are not available.

Table 1–14 shows which PLLs are available for each Stratix device and which input clock pin drives which PLLs.

Table 1–14. Stratix Clock Input Sources For Enhanced & Fast PLLs (Part 1 of 2)

Clock Input Pins	All Stratix Devices						EP1S30, EP1S40, EP1S60 & EP1S80 Devices Only				EP1S40 (3), EP1S60 & EP1S80 Devices Only	
	PLL 1 (1)	PLL 2 (1)	PLL 3 (1)	PLL 4 (1)	PLL 5 (2)	PLL 6 (2)	PLL 7 (1)	PLL 8 (1)	PLL 9 (1)	PLL 10 (1)	PLL 11 (2)	PLL 12 (2)
CLK0p/n	✓						✓					
CLK1p/n	✓											
CLK2p/n		✓						✓				
CLK3p/n		✓										
CLK4p/n						✓						
CLK5p/n						✓						
CLK6p/n												✓
CLK7p/n												✓
CLK8p/n			✓						✓			
CLK9p/n			✓									
CLK10p/n				✓						✓		
CLK11p/n				✓								
CLK12p/n											✓	
CLK13p/n											✓	
CLK14p/n					✓							
CLK15p/n					✓							

Table 1–14. Stratix Clock Input Sources For Enhanced & Fast PLLs (Part 2 of 2)

Clock Input Pins	All Stratix Devices						EP1S30, EP1S40, EP1S60 & EP1S80 Devices Only				EP1S40 (3), EP1S60 & EP1S80 Devices Only	
	PLL 1 (1)	PLL 2 (1)	PLL 3 (1)	PLL 4 (1)	PLL 5 (2)	PLL 6 (2)	PLL 7 (1)	PLL 8 (1)	PLL 9 (1)	PLL 10 (1)	PLL 11 (2)	PLL 12 (2)
FPll7clk							✓					
FPll8clk								✓				
FPll9clk									✓			
FPll10clk										✓		
Clock Feedback Input Pins												
Pll5_fbp/n					✓							
Pll6_fbp/n						✓						

Notes to Table 1–14:

(1) This is a fast PLL. The global or regional clocks in a fast PLL's quadrant can drive the fast PLL input. A pin or other PLL must drive the global or regional source. The source cannot be driven by internally generated logic before driving the fast PLL.

(2) This is an enhanced PLL.

(3) The EP1S40 device in the F780 package does not support PLLs 11 and 12.

Clock Output Connections

Enhanced PLLs have outputs for two regional clock outputs and four global outputs. There is line sharing between clock pins, global and regional clock networks and all PLL outputs. Check Tables 1–15 and 1–16 and Figures 1–21 and 1–22 to make sure that the clocking scheme is valid. The Quartus II software automatically maps to regional and global clocks to avoid any restrictions. Enhanced PLLs 5 and 6 drive out to single-ended pins as shown in Table 1–15. PLLs 11 and 12 drive out to single-ended pins.

You can connect each fast PLL 1, 2, 3, or 4 outputs (*g*0, *l*0, and *l*1) to either a global or a regional clock. (PLLs 3 and 4 are not available on Stratix GX devices.) There is line sharing between clock pins, FPLLCLK pins, global and regional clock networks and all PLL outputs. Check Figures 1–21 and 1–22 to make sure that the clocking is valid. The Quartus II software automatically maps to regional and global clocks to avoid any restrictions.

Table 1–15 shows the global and regional clocks that each PLL drives outputs to for Stratix devices. Table 1–16 shows the global and regional clock network each of the CLK and FPLLCLK pins drive when bypassing the PLL.

Table 1–15. Stratix Global & Regional Clock Output Line Sharing for Enhanced & Fast PLLs (Part 1 of 2)

Clock Network	All Devices						EP1S30, EP1S40, EP1S60 & EP1S80 Devices Only				EP1S40 (5), EP1S60 & EP1S80 Devices Only	
	PLL 1 (1)	PLL 2 (1)	PLL 3 (1)	PLL 4 (1)	PLL 5 (2)	PLL 6 (2)	PLL 7 (1)	PLL 8 (1)	PLL 9 (1)	PLL 10 (1)	PLL 11 (2)	PLL 12 (2)
GCLK0	✓	✓					✓	✓				
GCLK1	✓	✓					✓	✓				
GCLK2	✓	✓					✓	✓				
GCLK3	✓	✓					✓	✓				
GCLK4						✓						✓
GCLK5						✓						✓
GCLK6						✓						✓
GCLK7						✓						✓
GCLK8			✓	✓					✓	✓		
GCLK9			✓	✓					✓	✓		
GCLK10			✓	✓					✓	✓		
GCLK11			✓	✓					✓	✓		
GCLK12					✓						✓	
GCLK13					✓						✓	
GCLK14					✓						✓	
GCLK15					✓						✓	
RCLK0	✓	✓					✓					
RCLK1	✓	✓					✓					
RCLK2					✓						✓	
RCLK3					✓						✓	
RCLK4	✓	✓						✓				
RCLK5	✓	✓						✓				

Table 1–15. Stratix Global & Regional Clock Output Line Sharing for Enhanced & Fast PLLs (Part 2 of 2)

Clock Network	All Devices						EP1S30, EP1S40, EP1S60 & EP1S80 Devices Only				EP1S40 (5), EP1S60 & EP1S80 Devices Only	
	PLL 1 (1)	PLL 2 (1)	PLL 3 (1)	PLL 4 (1)	PLL 5 (2)	PLL 6 (2)	PLL 7 (1)	PLL 8 (1)	PLL 9 (1)	PLL 10 (1)	PLL 11 (2)	PLL 12 (2)
RCLK6						✓						✓
RCLK7						✓						✓
RCLK8			✓	✓						✓		
RCLK9			✓	✓						✓		
RCLK10					✓						✓	
RCLK11					✓						✓	
RCLK12						✓						✓
RCLK13						✓						✓
RCLK14			✓	✓					✓			
RCLK15			✓	✓					✓			
External Clock Output												
PLL5_OUT[3..0]p/n					✓							
PLL6_OUT[3..0]p/n						✓						
PLL11_OUT (3)											✓	
PLL12_OUT (4)												✓

Notes to Table 1–15:

(1) This is a fast PLL.
(2) This is an enhanced PLL.
(3) This pin is a tri-purpose pin; it can be an I/O pin, CLK13n, or used for PLL 11 output.
(4) This pin is a tri-purpose pin; it can be an I/O pin, CLK7n, or used for PLL 12 output.
(5) The EP1S40 device in the F780 package does not support PLLs 11 and 12.

Table 1–16. Stratix CLK & FPLLCLK Input Pin Connections to Global & Regional Clock Networks Note (1)

Clock Network	CLK Pins															FPLLCLK (2)			
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	7	8	9	10
GCLK0	✓																✓	✓		
GCLK1		✓															✓	✓		
GCLK2			✓														✓	✓		
GCLK3				✓													✓	✓		
GCLK4					✓															
GCLK5						✓														
GCLK6							✓													
GCLK7								✓												
GCLK8									✓										✓	✓
GCLK9										✓									✓	✓
GCLK10											✓								✓	✓
GCLK11												✓							✓	✓
GCLK12													✓							
GCLK13														✓						
GCLK14															✓					
GCLK15																✓				
RCLK0	✓																✓			
RCLK1		✓															✓			
RCLK2															✓			✓		
RCLK3																✓		✓		
RCLK4			✓																	
RCLK5				✓																
RCLK6					✓															
RCLK7						✓														
RCLK8											✓								✓	
RCLK9												✓							✓	
RCLK10													✓							✓
RCLK11														✓						✓
RCLK12							✓													

Table 1–16. Stratix CLK & FPLLCLK Input Pin Connections to Global & Regional Clock Networks Note (1)

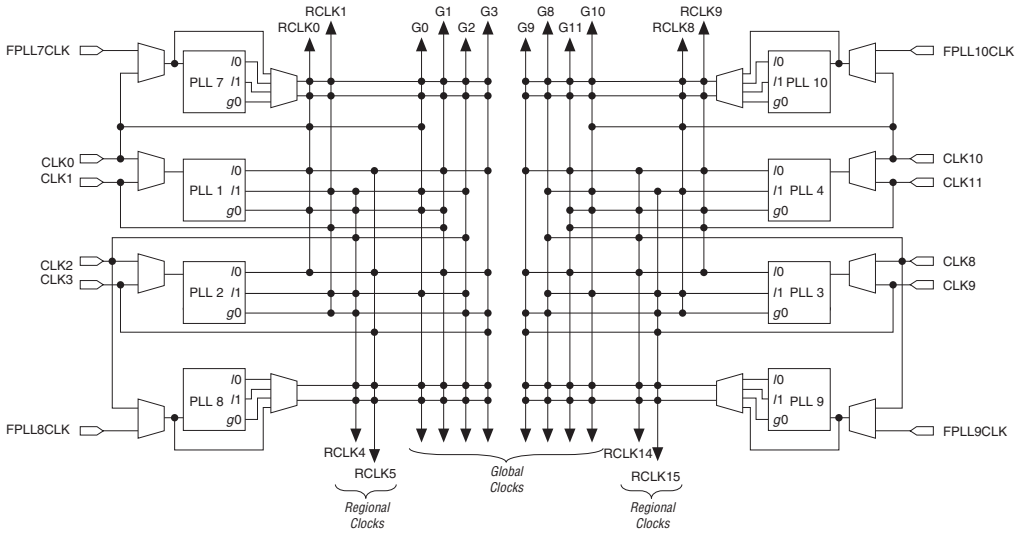
Clock Network	CLK Pins															FPLLCLK (2)			
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	7	8	9	10
RCLK13								✓												
RCLK14									✓											
RCLK15										✓										

Notes to Table 1–16:
(1) The CLK and FPLLCLK pins cannot drive.
(2) The FPLLCLK pin is only available in EP1S80, EP1S60, EP1S40, and EP1S30 devices.

The fast PLLs also drive high-speed SERDES clocks for differential I/O interfacing. For information on these FPLLCLK pins, see the *High-Speed Differential I/O Interfaces in Stratix Devices* chapter.

Figure 1–21 shows the global and regional clock input and output connections from the enhanced. Figure 1–21 shows graphically the same information as Tables 1–15 and 1–16 but with the added detail of where each specific PLL output port drives to.

Figure 1–21. Global & Regional Clock Connections from Side Clock Pins & Fast PLL Outputs



Notes to Figures 1–21:

(1) The global or regional clocks in a fast PLL's quadrant can drive the fast PLL input. A dedicated pin or other PLL must drive the global or regional source. The source cannot be driven by internally generated logic before driving the fast PLL.

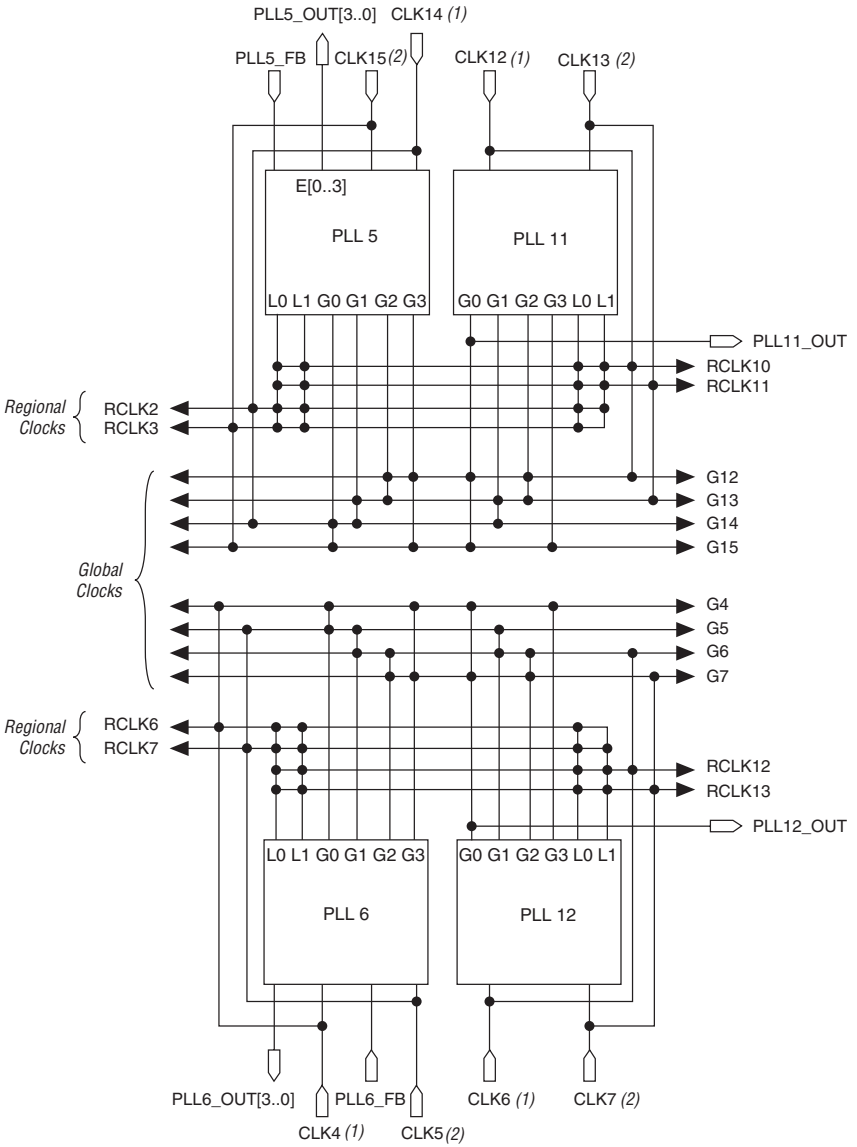
(2) PLLs 3, 4, 9, and 10 are used for the HSSI block in Stratix GX devices and are not available for this use.

When using a fast PLL to compensate for clock delays to drive logic on the chip, the clock delay from the input pin to the clock input port of the PLL is compensated only if the clock is fed by the dedicated input pin closest to the PLL. If the fast PLL gets its input clock from a global or regional clock or from another dedicated clock pin, which does not directly feed the fast PLL, the clock signal is first routed onto a global clock network. The signal then drives into the PLL. In this case, the clock delay is not fully compensated and the delay compensation is equal to the clock delay from the dedicated clock pin closest to the PLL to the clock input port of the PLL.

For example, if you use `CLK0` to feed PLL 7, the input clock path delay is not fully compensated, but if `FPLL7CLK` feeds PLL 7, the input clock path delay is fully compensated.

Figure 1–22 shows the global and regional clock input and output connections from the fast PLLs. Figure 1–22 shows graphically the same information as Tables 1–15 and 1–16 but with the added detail of where each specific PLL output port drives to.

Figure 1–22. Global & Regional Clock Connections from Top Clock Pins & Enhanced PLL Outputs



Notes to Figures 1–22:

(1) CLK4, CLK6, CLK12, and CLK14 feed the corresponding PLL's inclk0 port.

(2) CLK5, CLK7, CLK13, and CLK15 feed the corresponding PLL's inclk1 port.

Board Layout

The enhanced and fast PLL circuits in Stratix and Stratix GX devices contain analog components embedded in a digital device. These analog components have separate power and ground pins to minimize noise generated by the digital components. Both Stratix and Stratix GX enhanced and fast PLLs use separate VCC and ground pins to isolate circuitry and improve noise resistance.

VCCA & GNDA

Each enhanced and fast PLL uses separate VCC and ground pin pairs for their analog circuitry. The analog circuit power and ground pin for each PLL is called PLL<*PLL number*>_VCCA and PLL<*PLL number*>_GNDA. Connect the VCCA power pin to a 1.5-V power supply, even if you do not use the PLL. Isolate the power connected to VCCA from the power to the rest of the Stratix and Stratix GX device or any other digital device on the board. You can use one of three different methods of isolating the VCCA pin: separate V_{CCA} power planes, a partitioned V_{CCA} island within the V_{CCINT} plane, and thick V_{CCA} traces.

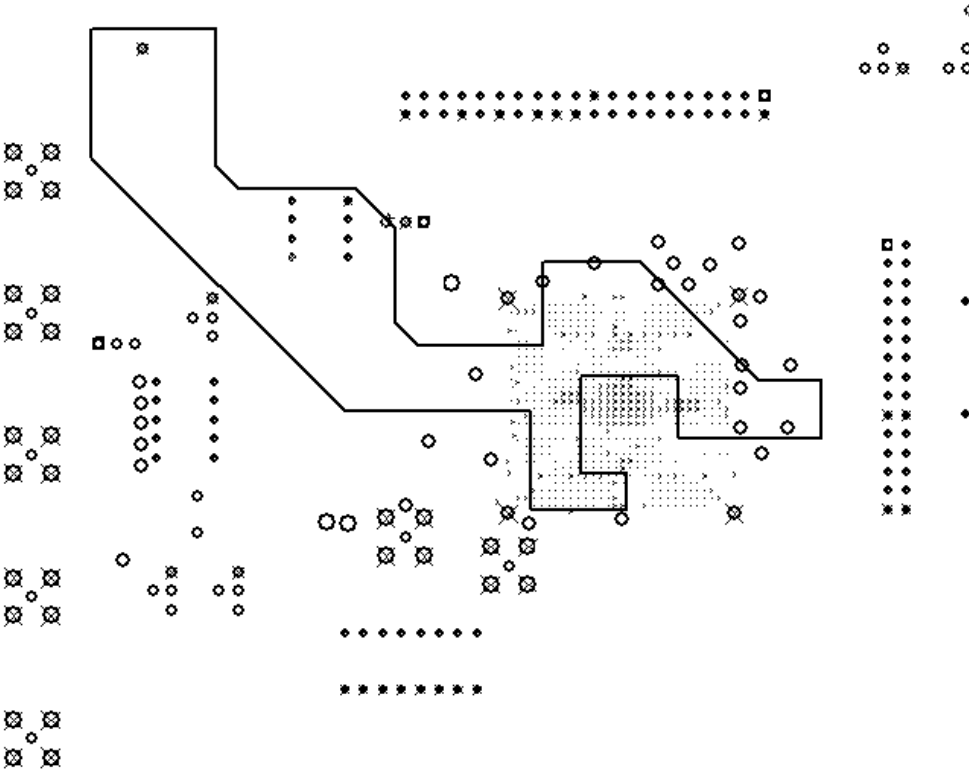
Separate V_{CCA} Power Plane

A mixed signal system is already partitioned into analog and digital sections, each with its own power planes on the board. To isolate the VCCA pin using a separate V_{CCA} power plane, connect the VCCA pin to the analog 1.5-V power plane.

Partitioned V_{CCA} Island within V_{CCINT} Plane

Fully digital systems do not have a separate analog power plane on the board. Because it is expensive to add new planes to the board, you can create islands for VCCA_PLL. Figure 1–23 shows an example board layout with an analog power island. The dielectric boundary that creates the island should be 25 mils thick. Figure 1–23 shows a partitioned plane within V_{CCINT} for V_{CCA}.

Figure 1–23. V_{CCINT} Plane Partitioned for V_{CCA} Island

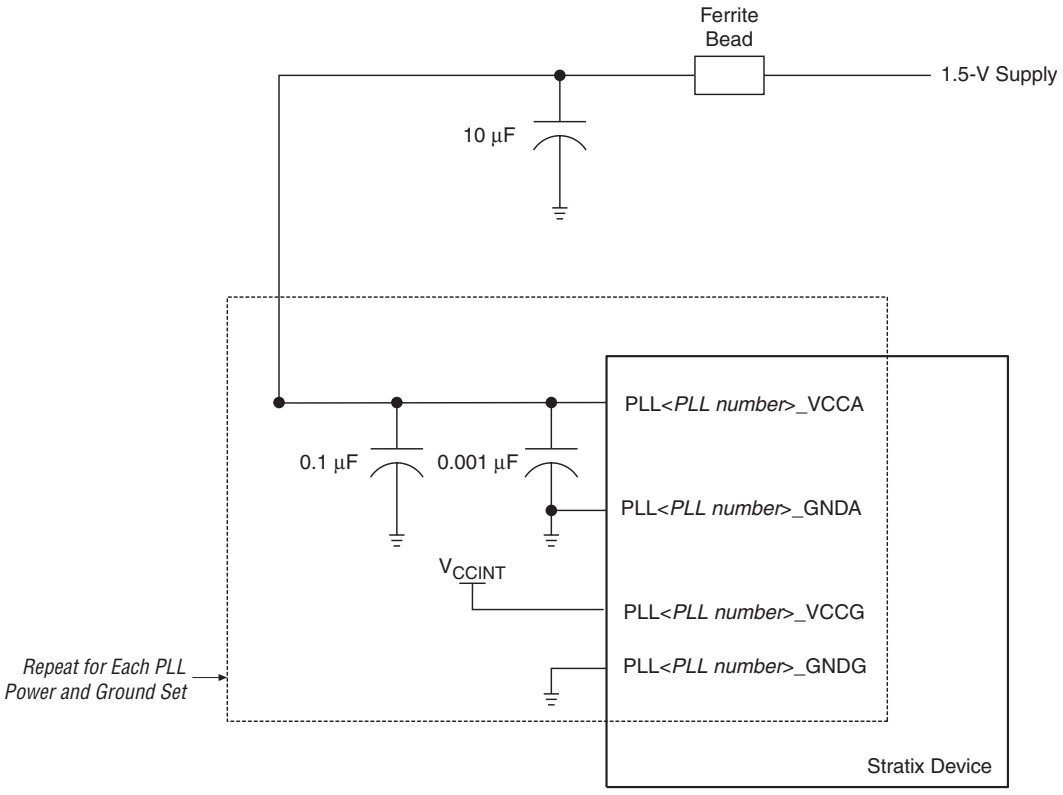


Thick V_{CCA} Trace

Because of board constraints, you might not be able to partition a V_{CCA} island. Instead, run a thick trace from the power supply to each V_{CCA} pin. The traces should be at least 20 mils thick.

In each of these three cases, you should filter each V_{CCA} pin with a decoupling circuit shown in Figure 1–24. Place a ferrite bead that exhibits high impedance at frequencies of 50 MHz or higher and a 10-µF tantalum parallel capacitor where the power enters the board. Decouple each V_{CCA} pin with a 0.1-µF and 0.001-µF parallel combination of ceramic capacitors located as close as possible to the Stratix or Stratix GX device. You can connect the GNDA pins directly to the same ground plane as the device's digital ground.

Figure 1–24. PLL Power Schematic for Stratix or Stratix GX PLLs



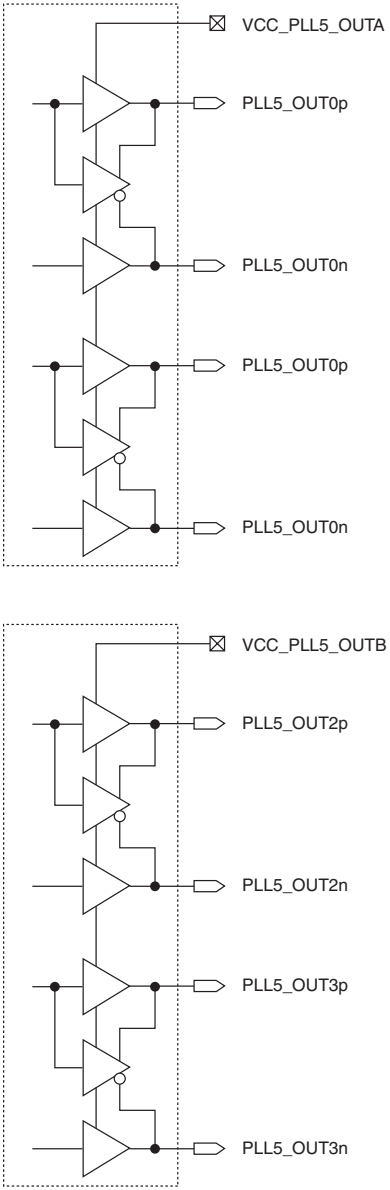
VCCG & GNDG

The guard ring power and ground pins are called PLL<*PLL number*>_VCCG and PLL<*PLL number*>_GNDG. The guard ring isolates the PLL circuit from the rest of the device. Connect these guard ring V_{CCG} pins to the quietest digital supply on the board. In most systems, this is the digital 1.5-V supply supplied to the device's V_{CCINT} pins. Connect the V_{CCG} pins to a power supply even if you do not use the PLL. You can connect the GNDG pins directly to the same ground plane as the device's digital ground. See Figure 1–24.

External Clock Output Power

Enhanced PLLs 5 and 6 also have isolated power pins for their dedicated external clock outputs (VCC_PLL5_OUTA and VCC_PLL5_OUTB, or VCC_PLL6_OUTA and VCC_PLL6_OUTB, respectively). PLLs 5 and 6 both have two banks of outputs. Each bank is powered by a unique output power, OUTA or OUTB, as illustrated in Figure 1–25. These outputs can by powered by 3.3, 2.5, 1.8, or 1.5 V depending on the I/O standard for the clock output in the A or B groups.

Figure 1–25. External Clock Output Pin Association to Output Power Note (1)

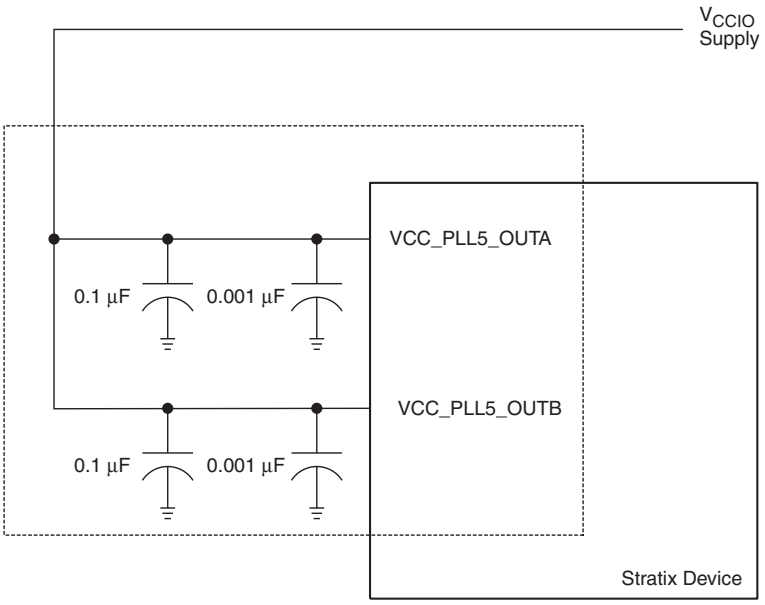


Note to Figure 1–25:

(1) These pins apply to PLL 5. The figure for PLL 6 is similar, except that the pin names begin with the prefix `PLL6` instead of `PLL5`.

Filter each isolated power pin with a decoupling circuit shown in Figure 1–26. Decouple the isolated power pins with a 0.1-µF and a 0.001-µF parallel combination of ceramic capacitors located as close as possible to the Stratix device.

Figure 1–26. Stratix PLL External Clock Output Power Ball Connections
Note (1)



Note to Figure 1–26:
(1) Figure 1–26 also applies to VCC_PLL6_OUTA/B.

Guidelines

Use the following guidelines for optimal jitter performance on the external clock outputs from enhanced PLLs 5 and 6. If all outputs are running at the same frequency, these guidelines are not necessary to improve performance.

- When driving two or more clock outputs from PLL 5 or 6, separate the outputs into the two groups shown in Figure 1–24. For example, if you are driving 100- and 200-MHz clock outputs off-chip from PLL 5, place one output on PLL5_OUT0p (powered by VCC_PLL5_OUTA) and the other output on PLL5_OUT2p (powered by VCC_PLL5_OUTB). Since the output buffers are powered by different pins, they are less susceptible to bimodal jitter. Bimodal jitter is a deterministic jitter not caused by the PLL but rather by coincident edges of clock outputs that are multiples of each other.
- Use phase shift to ensure edges are not coincident on all the clock outputs.
- Use phase shift to skew clock edges with respect to each other for best jitter performance.

  Delay shift (time delay elements) are no longer supported in Stratix PLLs. Use the phase shift feature to implement the desired time shift.

- If you cannot drive multiple clocks of different frequencies and phase shifts or isolate banks, you should control the drive capability on the lower frequency clock. Reducing how much current the output buffer has to supply can reduce the noise. Minimize capacitive load on the slower frequency output and configure the output buffer to drive slow slew rate and lower current strength. The higher frequency output should have an improved performance, but this may degrade the performance of your lower frequency clock output.

Conclusion

Stratix and Stratix GX device enhanced PLLs provide you with complete control of your clocks and system timing. These PLLs are capable of offering flexible system level clock management that was previously only available in discrete PLL devices. The embedded PLLs meet and exceed the features offered by these high-end discrete devices, reducing the need for other timing devices in the system.