

MPSW92

One Watt High Voltage Transistor

PNP Silicon

Features

- Pb-Free Packages are Available*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector – Emitter Voltage	V_{CEO}	-300	Vdc
Collector – Base Voltage	V_{CBO}	-300	Vdc
Emitter – Base Voltage	V_{EBO}	-5.0	Vdc
Collector Current – Continuous	I_C	-500	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.0 8.0	W mW/ $^\circ\text{C}$
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	2.5 20	W mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

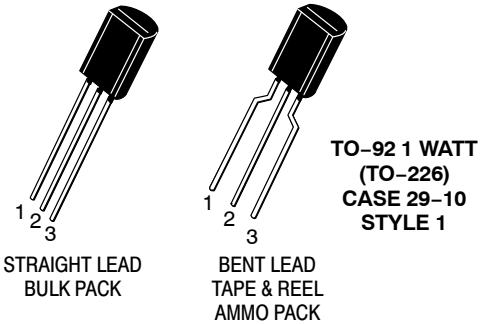
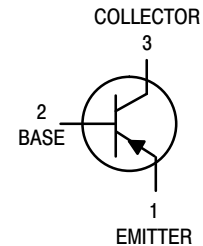
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	125	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	50	$^\circ\text{C}/\text{W}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

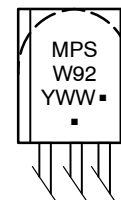


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MARKING DIAGRAM



MPSW45x = Device Code
 x = 45A Devices
 A = Assembly Location
 Y = Year
 WW = Work Week
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MPSW92

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Breakdown Voltage (Note 1) (I _C = –1.0 mA _{dc} , I _B = 0)	V _{(BR)CEO}	–300	–	V _{dc}
Collector–Base Breakdown Voltage (I _C = –100 μA _{dc} , I _E = 0)	V _{(BR)CBO}	–300	–	V _{dc}
Emitter–Base Breakdown Voltage (I _E = –100 μA _{dc} , I _C = 0)	V _{(BR)EBO}	–5.0	–	V _{dc}
Collector Cutoff Current (V _{CB} = –200 V _{dc} , I _E = 0)	I _{CBO}	–	–0.25	μA _{dc}
Emitter Cutoff Current (V _{EB} = –3.0 V _{dc} , I _C = 0)	I _{EBO}	–	–0.1	μA _{dc}

ON CHARACTERISTICS (Note 1)

DC Current Gain (I _C = –1.0 mA _{dc} , V _{CE} = –10 V _{dc}) (I _C = –10 mA _{dc} , V _{CE} = –10 V _{dc}) (I _C = –30 mA _{dc} , V _{CE} = –10 V _{dc})	h _{FE}	25 40 25	– – –	–
Collector–Emitter Saturation Voltage (I _C = –20 mA _{dc} , I _B = –2.0 mA _{dc})	V _{CE(sat)}	–	–0.5	V _{dc}
Base–Emitter Saturation Voltage (I _C = –20 mA _{dc} , I _B = –2.0 mA _{dc})	V _{BE(sat)}	–	–0.9	V _{dc}

SMALL–SIGNAL CHARACTERISTICS

Current–Gain – Bandwidth Product (I _C = –10 mA _{dc} , V _{CE} = –20 V _{dc} , f = 20 MHz)	f _T	50	–	MHz
Collector–Base Capacitance (V _{CB} = –20 V _{dc} , I _E = 0, f = 1.0 MHz)	C _{cb}	–	6.0	pF

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

ORDERING INFORMATION

Device	Package	Shipping†
MPSW92	TO–92	5000 Units / Box
MPSW92G	TO–92 (Pb–Free)	5000 Units / Box
MPSW92RLREG	TO–92 (Pb–Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MPSW92

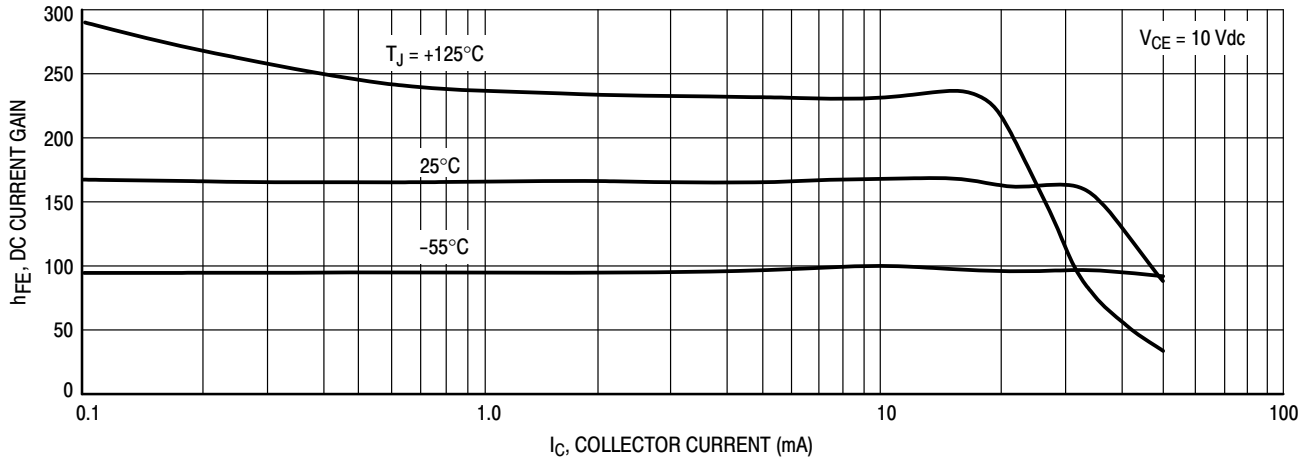


Figure 1. DC Current Gain

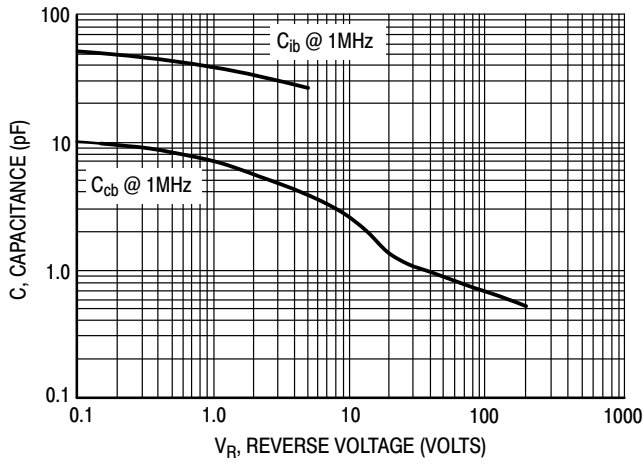


Figure 2. Capacitance

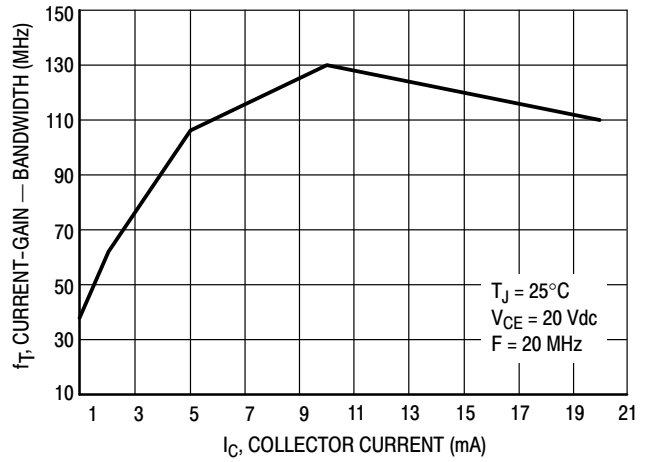


Figure 3. Current-Gain - Bandwidth

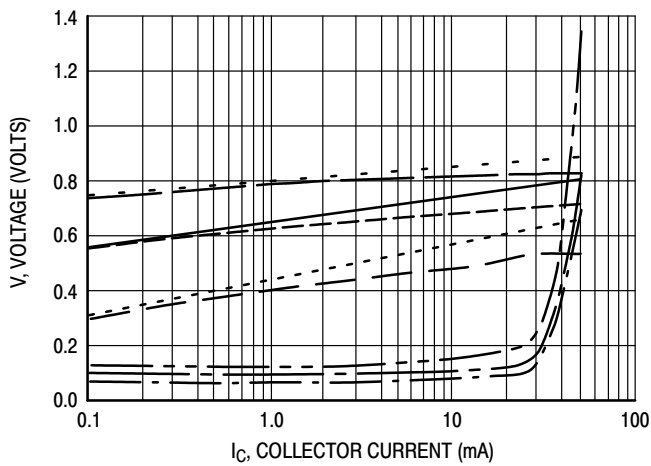


Figure 4. "ON" Voltages

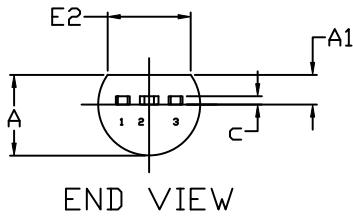
- $V_{CE(sat)}$ @ 25°C , $I_C/I_B = 10$
- $V_{CE(sat)}$ @ 125°C , $I_C/I_B = 10$
- $V_{CE(sat)}$ @ -55°C , $I_C/I_B = 10$
- $V_{BE(sat)}$ @ 25°C , $I_C/I_B = 10$
- $V_{BE(sat)}$ @ 125°C , $I_C/I_B = 10$
- $V_{BE(sat)}$ @ -55°C , $I_C/I_B = 10$
- $V_{BE(on)}$ @ 25°C , $V_{CE} = 10 \text{ V}$
- $V_{BE(on)}$ @ 125°C , $V_{CE} = 10 \text{ V}$
- $V_{BE(on)}$ @ -55°C , $V_{CE} = 10 \text{ V}$



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CASE 29-10
ISSUE D

DATE 05 MAR 2021

STRAIGHT LEAD



NOTES:


1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
4. DIMENSION b AND b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 0.20. DIMENSION b2 LOCATED ABOVE THE DAMBAR PORTION OF MIDDLE LEAD.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	3.75	3.90	4.05
A1	1.28	1.43	1.58
b	0.38	0.465	0.55
b2	0.62	0.70	0.78
c	0.35	0.40	0.45
D	7.85	8.00	8.15
E	4.75	4.90	5.05
E2	3.90	---	---
e	1.27 BSC		
L	13.80	14.00	14.20

STYLES AND MARKING ON PAGE 3

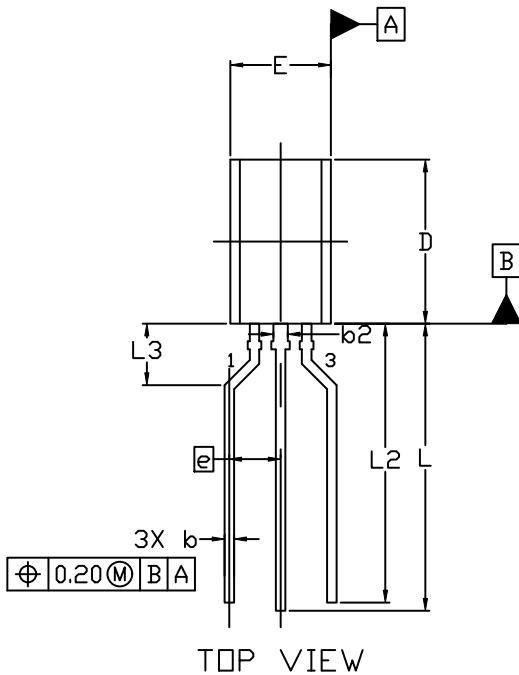
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ISSUE D

DATE 05 MAR 2021

FORMED LEAD




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c	0.35	0.40	0.45
D	7.85	8.00	8.15
E	4.75	4.90	5.05
E2	3.90	---	---
e	2.50 BSC		
L	13.80	14.00	14.20
L2	13.20	13.60	14.00
L3	3.00 REF		

STYLES AND MARKING ON PAGE 3

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CASE 29-10
ISSUE D**

DATE 05 MAR 2021

- | | | | | |
|---|--|--|---|---|
| STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR | STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR | STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE | STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE | STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE |
| STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN | STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE | STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE | STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2 | STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE |
| STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE | STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2 | STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2 | STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE | STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2 |
| STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE | STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER | STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED | STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE | STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE |
| STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE | STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN | STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN | STYLE 24:
PIN 1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE | STYLE 25:
PIN 1. MT 1
2. GATE
3. MT 2 |
| STYLE 26:
PIN 1. V _{CC}
2. GROUND 2
3. OUTPUT | STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT | STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE | STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE | STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE |
| STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE | STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER | STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT | STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC | STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER |

**GENERIC
MARKING DIAGRAM***



- XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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