

NCP4302

Secondary Side Synchronous Flyback Controller

The NCP4302 is a full featured controller and driver that provide all the control and protection functions necessary for implementing a synchronous rectifier operation in a flyback converter. With the use of the NCP4302, the space conscious flyback applications such as Adaptors, chargers, set top boxes can achieve significant efficiency improvements at minimal extra cost. In addition to the synchronous rectifier control, the IC incorporates an accurate TL431 type shunt regulator, current monitoring circuit and optocoupler driver to provide a single IC secondary solution. The NCP4302 works with any type of flyback topology (continuous mode, Quasi-resonant mode or discontinuous mode) – providing a high level of versatility.

Features

- Self-contained Control of Synchronous Rectifier in CCM, DCM, and QR Flyback Applications
- Interface to External Signal for CCM Mode
- True Secondary Zero Current Detection
- High Gate Drive Currents (2.5 A Source/Sink)
- High Voltage Operation
- Current Sense Flexibility (MOSFET $R_{DS(on)}$ OR CS Resistor)
- Accurate Low Voltage Reference
 - NCP4302A 2.55 V, 1%
 - NCP4302B 1.275 V, 1%
- Programmable Independent Secondary Side t_{on} and t_{off} Delays
- Maximum Frequency of Operation up to 250 kHz
- These are Pb-Free Devices

Typical Applications

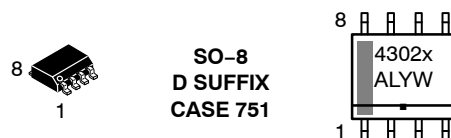
- Notebook Adapters
- LCD TV Adapters
- Consumer Appliances such as DVD, VCR
- Power Over Ethernet Applications (IP phones, Wireless Access Points)
- Battery Chargers



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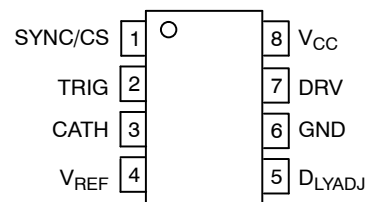
www.onsemi.com

MARKING DIAGRAM



- x = Reference Voltage (A or B)
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

PIN CONFIGURATION



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP4302ADR2G	SO-8 (Pb-Free)	2500/Tape & Reel
NCP4302BDR2G	SO-8 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCP4302

PIN DESCRIPTION

Pin Number	Symbol	Description
1	SYNC/CS	Connected to the flyback winding. The current on this pin is sensed and used to turn on the Synchronous Rectification MOSFET (SRFET). This pin is also used to sense the zero crossing of the MOSFET current either using the $R_{DS(on)}$ of the SRFET or using an external current sense resistor connected between drain of the SRFET and the flyback winding.
2	TRIG	Input pin for direct turn-off of the MOSFET. Typically connected to a signal from primary controller (for CCM mode) or a signal derived from the transformer (for QR mode). Has very short propagation delay to output (<50 ns).
3	CATH	Feedback compensation pin for the TL431 shunt regulator. Has the capability to sinking 10 ma of opto current.
4	V_{REF}	Output voltage feedback through resistive divider connected to this pin. Regulated at 1.28 V (option B) or 2.55 V (option A).
5	D_{LYADJ}	A resistive divider between the power supply output and ground with the center point tied to the D_{LYADJ} input pin allows for independent adjustment of the minimum t_{on} and t_{off} delay time. The maximum external capacitance from this pin to ground is 25 pF.
6	GND	Return pin for the controller – connected to the output return.
7	DRV	Drive output for external MOSFET – 2.5 A peak drive capability, internally clamped to 13.5 V (Maximum)
8	V_{CC}	Bias voltage for the controller. Maximum voltage is 28 V.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Input Current	V_{CC} I_{CC}	-0.3 to 28 100	V mA
Drive Voltage Current	V_{DRV}	-0.3 to 18 100	V mA
Drive Current Source Sink	I_{DRV}	2.5 -2.5	Apk
Analog and Logic Inputs	TRIG, V_{REF} , D_{LYADJ}	-0.3 to 10 100	V mA
Maximum Voltage Current	SYNC/CS	- 10 to 95 100	V mA
Operating Junction Temperature Range	T_J	-40 to 125	°C
Maximum Junction Temperature	T_{Jmax}	150	°C
Storage Temperature Range	T_{Smax}	-65 to 150	°C
Lead Temperature (Soldering, 10 s)	T_{Lmax}	300	°C
Reference input Current, continuous	I_{REF}	-0.05 to 10	mA
Total Power Dissipation	P_D	225	mW
Thermal Resistance Junction-to-Ambient	θ_{JA}	178	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- This device series contains ESD protection and exceeds the following tests:
Pin 1–8: Human Body Model 2000 V per JEDEC Standard JESD22, Method A114E.
Machine Model (MM) 200 V per JEDEC Standard JESD22, Method A115A.
- This device contains Latch-up protection and exceeds ± 100 ma per JEDEC Standard JESD78

NCP4302

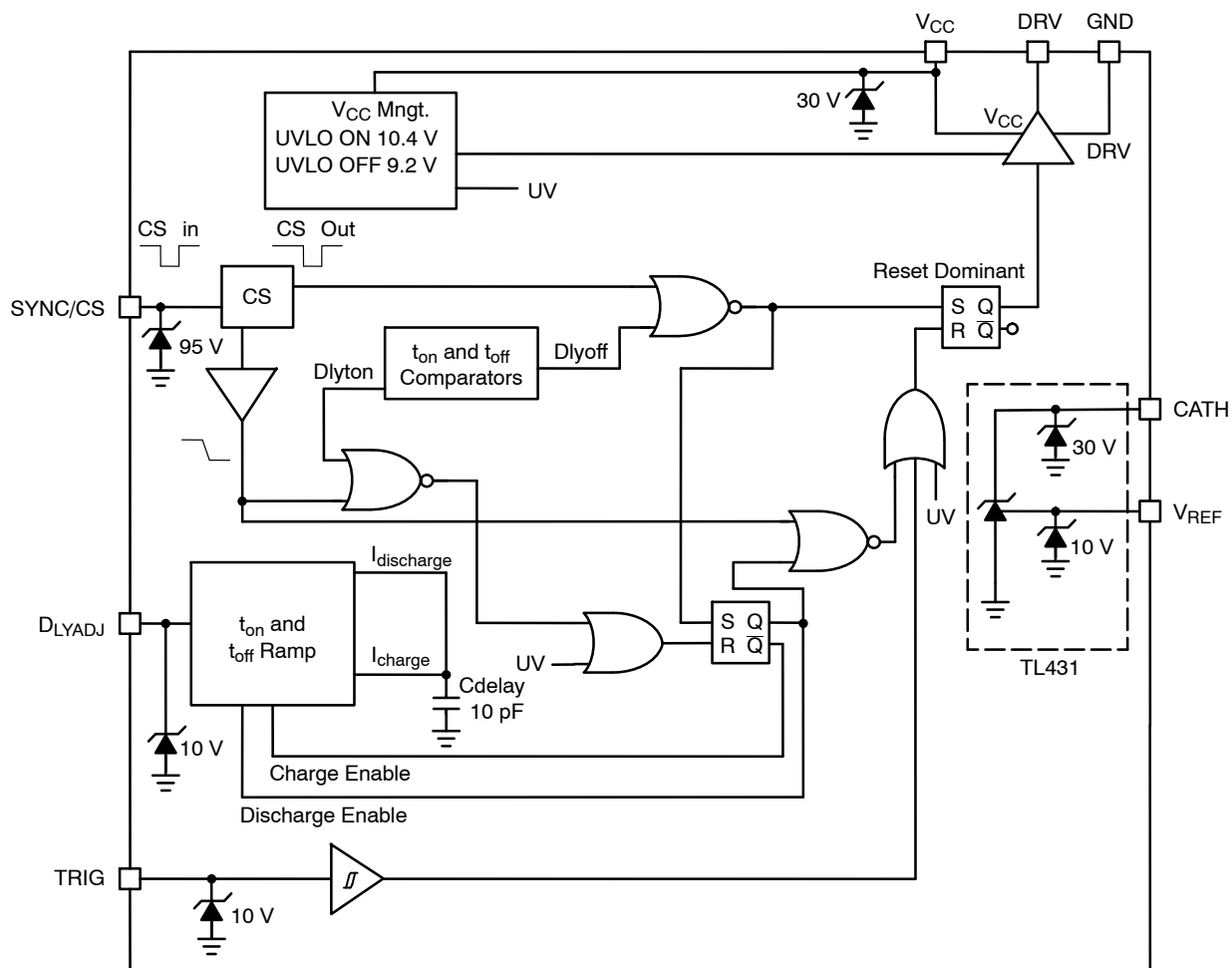


Figure 1. Block Diagram

NCP4302

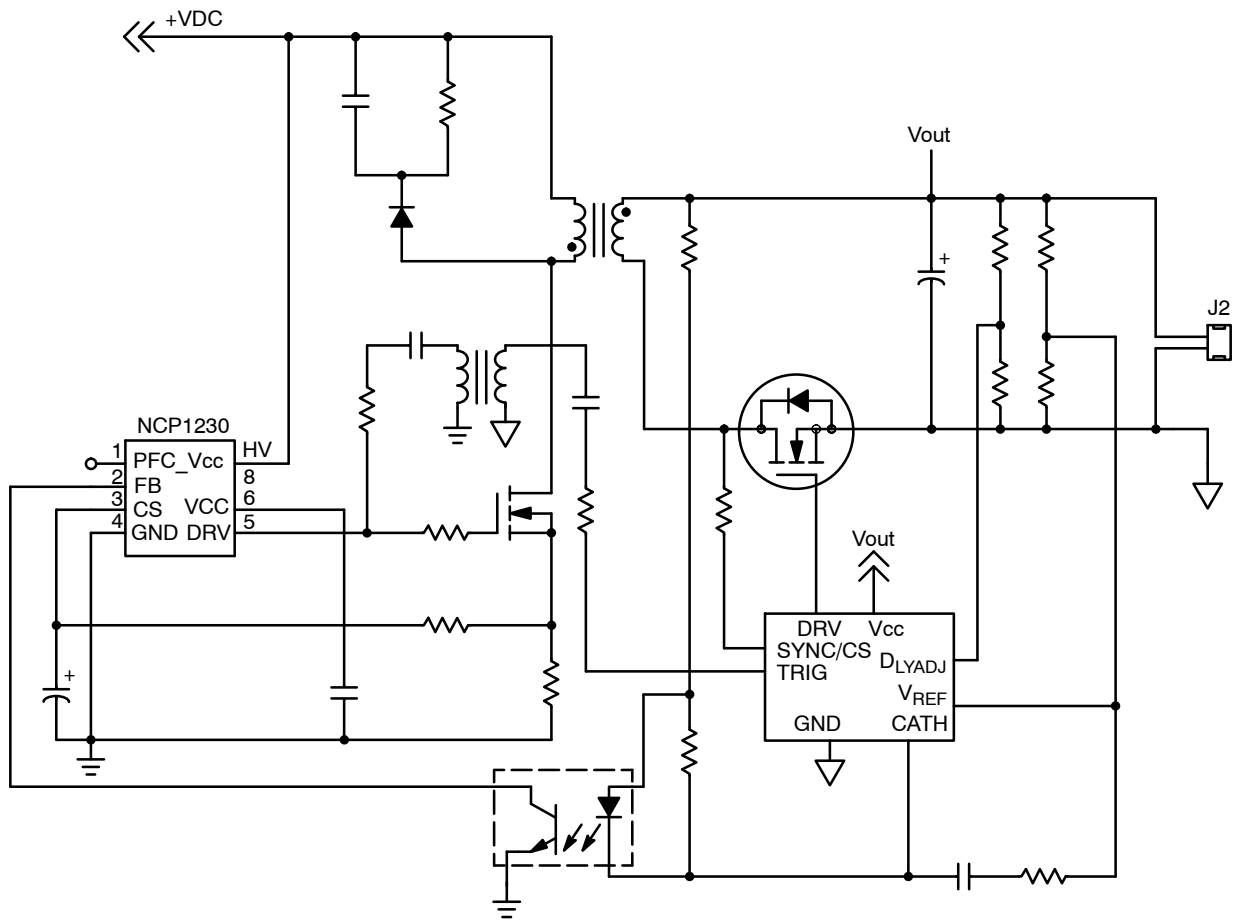


Figure 2. Typical Application

NCP4302

ELECTRICAL CHARACTERISTICS

($V_{CC} = 19\text{ V}$, Sync frequency = 100 kHz, $V_{REF} = V_{KA}$ ($I_{KA} = 1\text{ mA}$), $R_S = 75\text{ ohms}$, $V_{TRIG} = \text{GND}$, $C_{DRV} = 1\text{ nF}$, $R_{DLYADJ} = 30.1\text{ k}$, $V_{DLYADJ} = 2.0\text{ V}$, for typical values $T_J = 25^\circ\text{C}$, for min/max values $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, Max $T_J = 150^\circ\text{C}$, unless otherwise noted)

Rating	Test Conditions	Symbol	Min	Typ	Max	Unit
V_{CC}						
Start-up Threshold	$V_{CC} \uparrow$, SYNC/CS = 0 to -0.5 V 100 kHz, 5 μs pulse, Trig = 0 V	$V_{CC(on)}$	9.6	10.4	11.2	V
Stop Threshold	$V_{CC} \downarrow$, SYNC/CS = 0 to -0.5 V 100 kHz, 5 μs pulse, Trig = 0 V	$V_{CC(off)}$	8.5	9.2	-	V
V _{CC} shutdown Hysteresis	$V_{CC(on)} - V_{CC(off)}$	$V_{CC(HYS)}$	0.9	1.2	1.4	V
Supply current after turn-on	no-load on DRV pin, SYNC/CS = 0 to -0.5 V 100 kHz, 5 μs pulse, Trig = 0 V	I_{CC1}	-	2.7	5.6	mA
Supply current after turn-on	SYNC/CS = 0 to -0.5 V 100 kHz, 5 μs pulse, Trig = 0 V	I_{CC2}	-	3.6	7.5	mA

DRIVE OUTPUT

Output voltage rise-time	10-90% of the output signal SYNC/ CS = 0 to -0.5 V 100 kHz, 5 μs pulse, Trig = 0 V	t_r	-	-	40	ns
Output voltage fall-time	10-90% of the output signal SYNC/ CS = 0 to -0.5 V, 100 kHz, 5 μs pulse, Trig = 0 V	t_f	-	-	40	ns
Output source current (Note 3)		$I_{DRV(source)}$	-	2.5	-	Apk
Driver high level output voltage	$I_{SOURCE} = 200\text{ mA}$, SYNC/CS = 0 to -0.5 V 100 kHz, 5 μs pulse, Trig = 0 V, $V_{CC} = 12\text{ V}$	$V_{DRV(H)}$	6.5	9.5	-	V
Output sink current (Note 3)		$I_{DRV(sink)}$	-	2.5	-	Apk
Driver Output low level output voltage	$I_{SINK} = 200\text{ mA}$, SYNC/CS = 0 to -0.5 V 100 kHz, 5 μs pulse, Trig = 0 V, $V_{CC} = 12\text{ V}$	$V_{DRV(L)}$	-	160	500	mV
Drive voltage internal clamp	$V_{CC} = 28\text{ V}$, SYNC/CS = 0 to -0.5 V 100 kHz, 5 μs pulse, Trig = 0 V, DRVpin = 10 k Ω	$V_{DRV(CLMP)}$	-	-	17	V
Minimum drive output voltage	$V_{CC} = V_{CC(off)} + 200\text{ mV}$, DRV pin = 10 k Ω + 1 nF, SYNC/CS = 0 to -0.5 V 100 kHz, 5 μs pulse, Trig = 0 V	$V_{DRV(MIN)}$	5.5	6.5	-	V

SYNC/CS

The total propagation delay from SYNC/CS to the DRV output	SYNC/CS = +0.5 V to -0.5 V 100 kHz, 5 μs pulse, (Trig = 0 V)(Refer to the Drive Output specifications for Tr 50% of the output signal	t_{p1}	-	70	135	ns
Zero Current Detection	$V_{SYNC/CS} < -30\text{ mV}$	$I_{s(zcd)}$	50	230	450	μA
Current Sense Pin Offset Voltage at Zero Current Level (Note 3)		$V_{S(ZCD)}$	-30	-	-	mV
SYNC/CS Leakage current	$V_{SYNC/CS} = 95\text{ V}$	$I_{SCSLeakage}$	-	-	10	μA

TRIGGER SECTION

Minimum Trigger pulse duration	SYNC/CS = 0 to -0.5 V 100 kHz, 5 μs pulse, Trig \uparrow	trig-pw	75	-	-	ns
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Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Guaranteed by Design

NCP4302

ELECTRICAL CHARACTERISTICS

($V_{CC} = 19\text{ V}$, Sync frequency = 100 kHz, $V_{REF} = V_{KA}$ ($I_{KA} = 1\text{ mA}$), $R_S = 75\text{ ohms}$, $V_{TRIG} = \text{GND}$, $C_{DRV} = 1\text{ nF}$, $R_{DLYADJ} = 30.1\text{ k}$, $V_{DLYADJ} = 2.0\text{ V}$, for typical values $T_J = 25^\circ\text{C}$, for min/max values $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, Max $T_J = 150^\circ\text{C}$, unless otherwise noted)

Rating	Test Conditions	Symbol	Min	Typ	Max	Unit
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TRIGGER SECTION

Trigger Pulse Voltage for Gate turn-off	SYNC/CS = 0 to -0.5 V 100 kHz, 5 μs pulse, Trig \uparrow	Vtrig	2.0	-	4.0	V
Propagation delay from TRIG to DRV turn-off	$C_{DRV} = \text{no-load}$, SYNC/CS = -0.5 V 100 kHz, 5 μs pulse, Trig = 0-5 V \uparrow	t_{p2}	-	25	85	ns

TL431 CHARACTERISTICS

Reference input voltage	$I_{KA} = 5\text{ mA}$, $V_{KA} = V_{REF}$ NCP4302A $T_J = +25^\circ\text{C}$ $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$	V_{REF}	2.525 2.499	2.55 -	2.575 2.60	V
Reference input voltage	($I_K = 5\text{ mA}$, $V_{KA} = V_{REF}$) NCP4302B $T_J = +25^\circ\text{C}$ $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$	V_{REF}	1.262 1.249	1.275 -	1.288 1.301	V
Reference Input Current	$I_{KA} = 10\text{ mA}$	I_{Ref}	-	0.0018	4.0	μA
Minimum CATH current for regulation	$I_{SOURCE} \uparrow 0$ to 1 mA	I_{KA}	-	0.5	1.0	mA
Reference voltage line regulation	$\Delta V_{KA} = V_{CCon} - 16\text{ V}$, $I_{KA} = 1\text{ mA}$ $= \frac{\Delta V_{REF}}{\Delta V_{KA}}$	V_{KA}	-	2.0	5.0	mV/V
Off-State CATH Current	$V_{KA} = 18\text{ V}$, $V_{REF} = 0\text{ V}$ (test circuit 2, V_{REF} pin grounded)	I_{off}	-	11	20	μA
Dynamic impedance	$V_{KA} = V_{REF}$, $\Delta I_{KA} = 1\text{ mA}$ to 10 mA	Z_{KA}	-	0.62	1.5	Ω
The maximum sink current capability	($I_{SOURCE} \uparrow 0$ to 10 mA)	$I_{sinkmax}$	10	-	-	mA

ADJUSTABLE TIME DELAY

The t_{on} time delay	SYNC/CS = 0 to -0.5 V 100 kHz, 5 μs pulse, Trig = 0 V C_{DLYADJ} internal = 10 pF ($V_S = 2.0\text{ V}$, $R_{th} = 30.1\text{ k}\Omega$)	$t_{on(\text{delay})}$	1.0	1.4	1.8	μs
The min and max $t_{on(\text{delay})}$ range (Note 3)	* $R_2 = 190\text{ k}\Omega$, $R_3 = 57\text{ k}\Omega$ * $R_2 = 499\text{ k}\Omega$, $R_3 = 39\text{ k}\Omega$ (*See Figure 27)	$t_{on(\text{range})}$	0.45 -	- -	- 2.0	μs
The maximum and minimum input voltage operating range. (Note 3)	The maximum capacitance from pin 5 to ground is 25 pF.	$V_{inDLYADJ}$	1.5	-	4.5	V
The maximum and minimum input operating current into the D_{LYADJ} pin (Note 3)		$I_{inDLYADJ}$	9	-	200	μA
The t_{off} time delay	SYNC/CS = 0 to -0.5 V 100 kHz, 5 μs pulse, Trig = 0 V C_{DLYADJ} internal = 10 pF ($V_S = 2.0\text{ V}$, $R_{th} = 30.1\text{ k}$)	$t_{off(\text{delay})}$	2.8	3.8	4.8	μs
The min and max $t_{off(\text{delay})}$ range (Note 3)	$R_2 = 66\text{ k}$, $R_3 = 23.6\text{ k}$ * $R_2 = 408\text{ k}$, $R_3 = 32.4\text{ k}$ (*See the schematic below)	$t_{off(\text{range})}$	0.8 -	- -	- 4.6	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Guaranteed by Design

TYPICAL CHARACTERISTICS

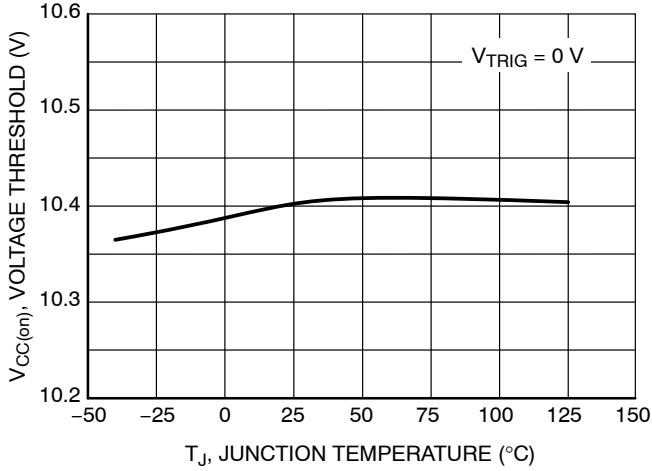


Figure 1. $V_{CC(on)}$ Threshold vs. Junction Temperature

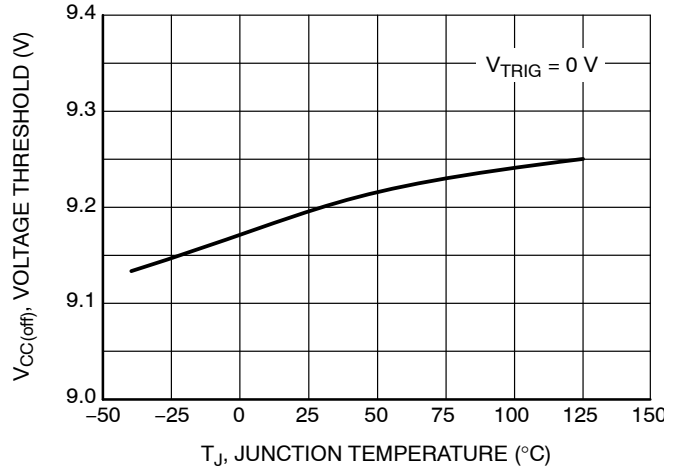


Figure 2. $V_{CC(off)}$ vs. Junction Temperature

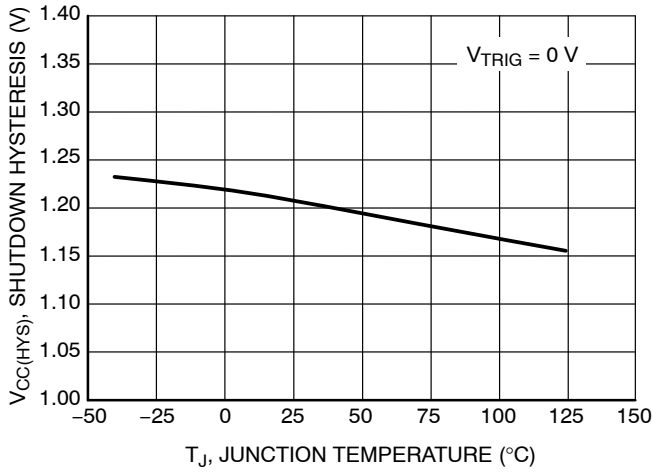


Figure 3. $V_{CC(HYS)}$ vs. Junction Temperature

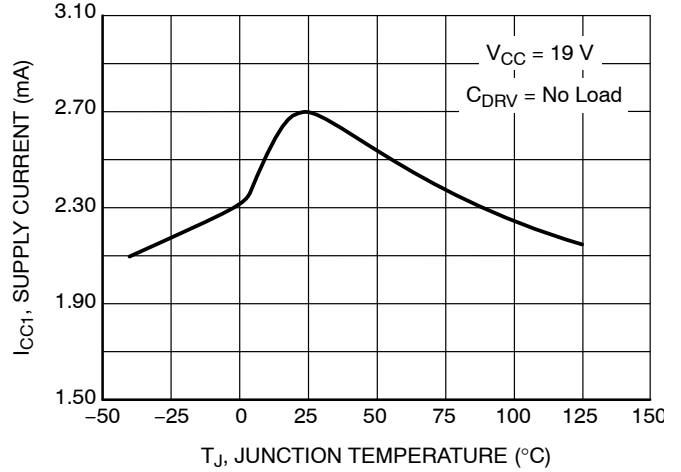


Figure 4. Internal Current Consumption at No Load vs. Junction Temperature

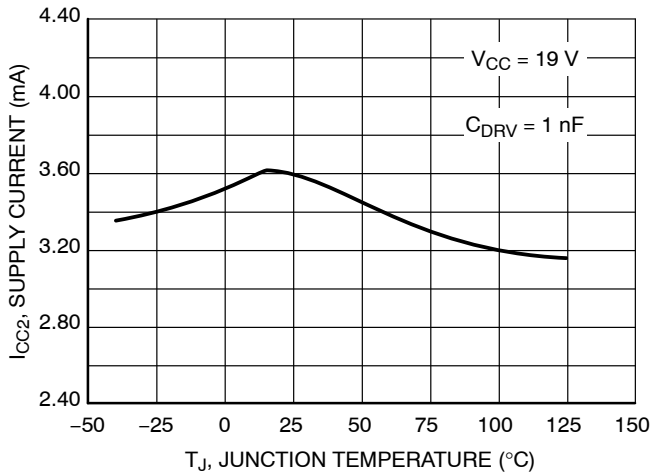


Figure 5. Supply Current Consumption with 1 nF Load vs. Junction Temperature

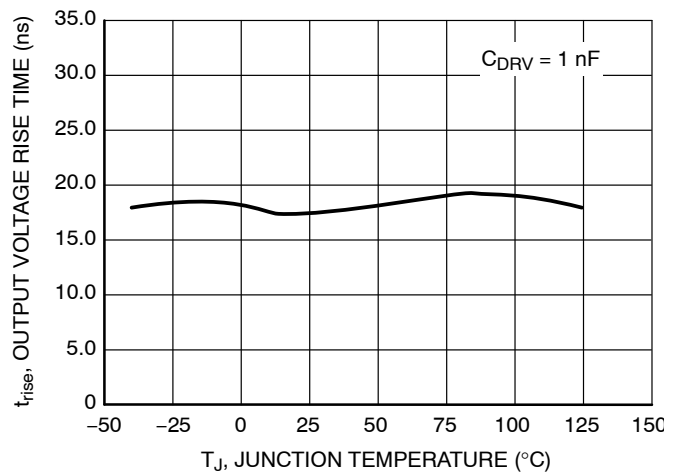


Figure 6. Drive Output Rise Time vs. Junction Temperature

TYPICAL CHARACTERISTICS

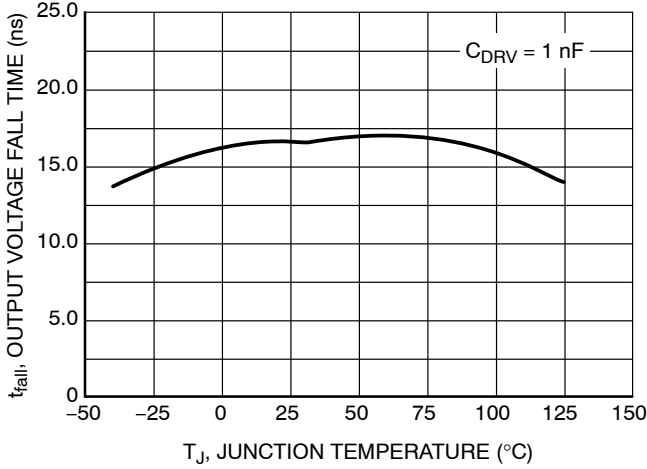


Figure 7. Drive Output Fall-time vs. Junction Temperature

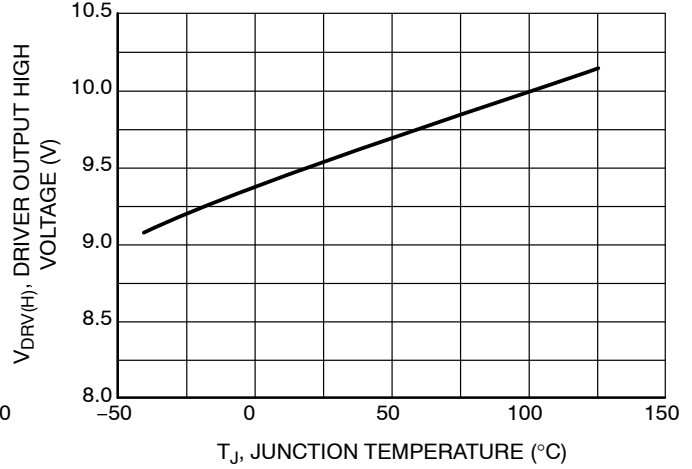


Figure 8. Driver V_{out} High vs. Junction Temperature

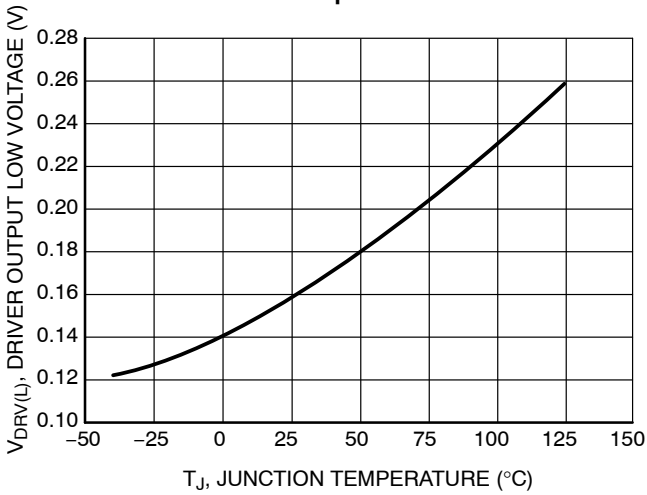


Figure 9. Driver V_{out} Low vs. Junction Temperature

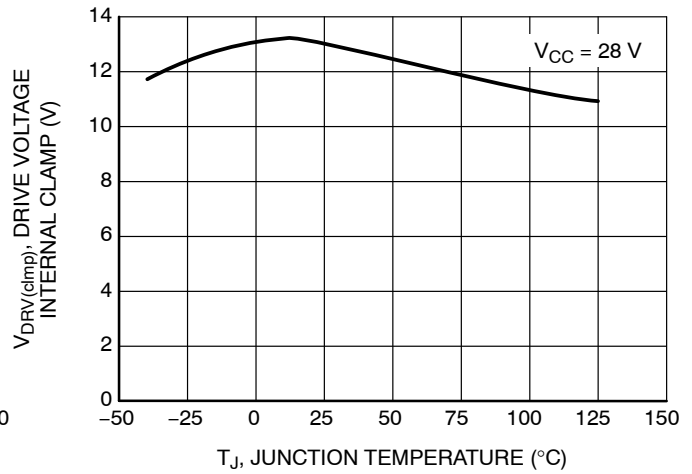


Figure 10. V_{gate} Clamp vs. Junction Temperature

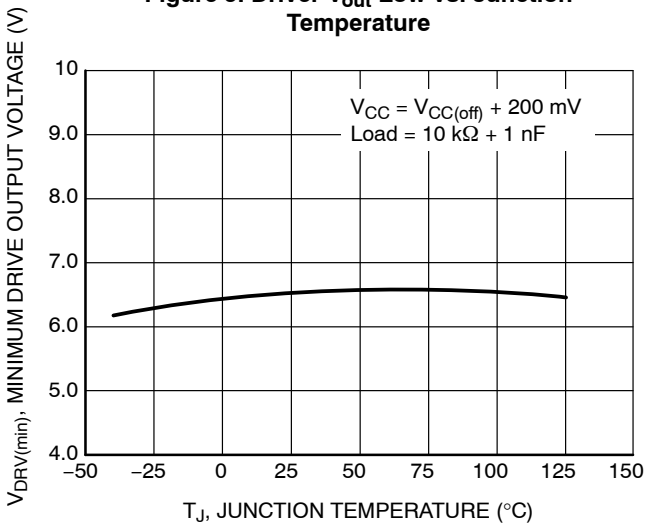


Figure 11. $V_{OUT(min)}$ vs. Junction Temperature

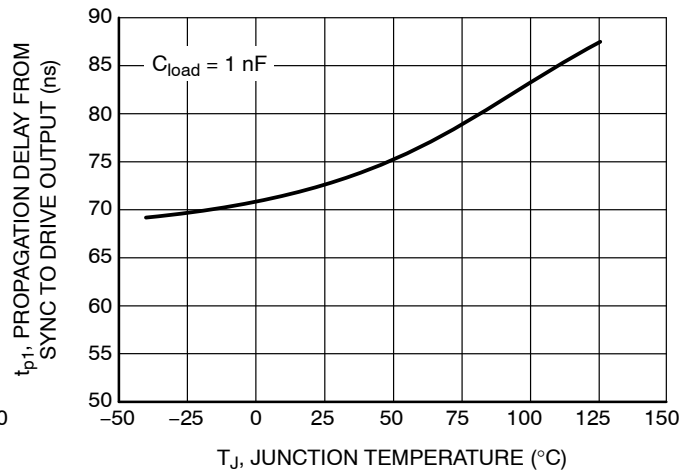


Figure 12. t_{p1} Propagation Delay, SYNC/CS to DRIVE vs. Junction Temperature

TYPICAL CHARACTERISTICS

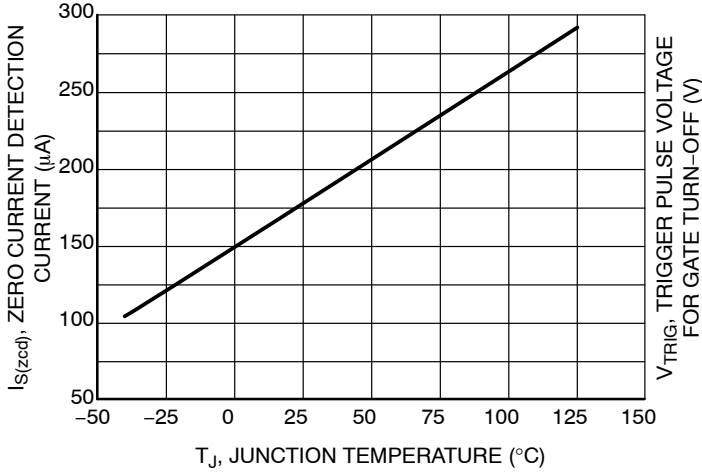


Figure 13. Zero Current Detect I_{source} vs. Junction Temperature

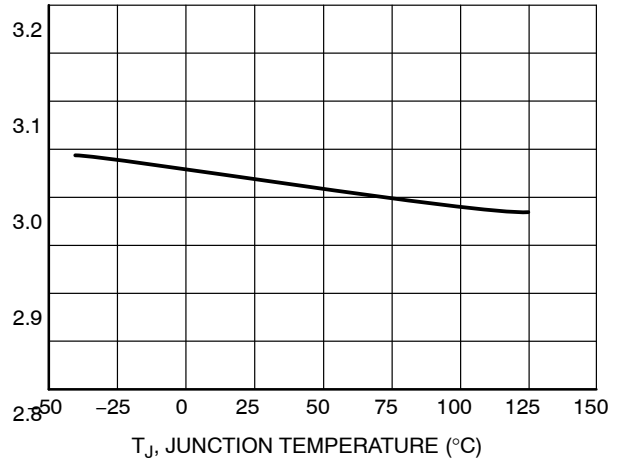


Figure 14. Trigger Pulse Voltage for Gate Turn-off vs. Junction Temperature

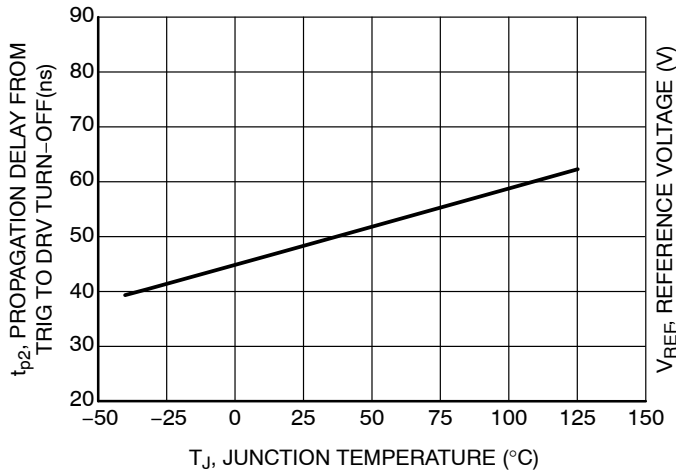


Figure 15. t_{p2} Propagation Delay TRIG in to DRIVE Off, NO Load vs. Junction Temperature

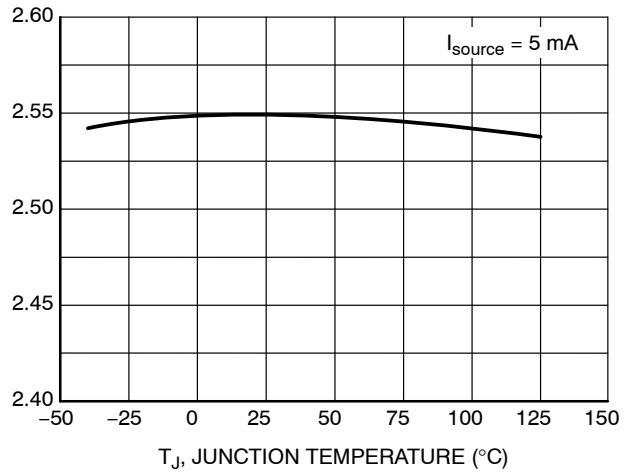


Figure 16. 2.55 V Reference (Option A) Voltage vs. Junction Temperature

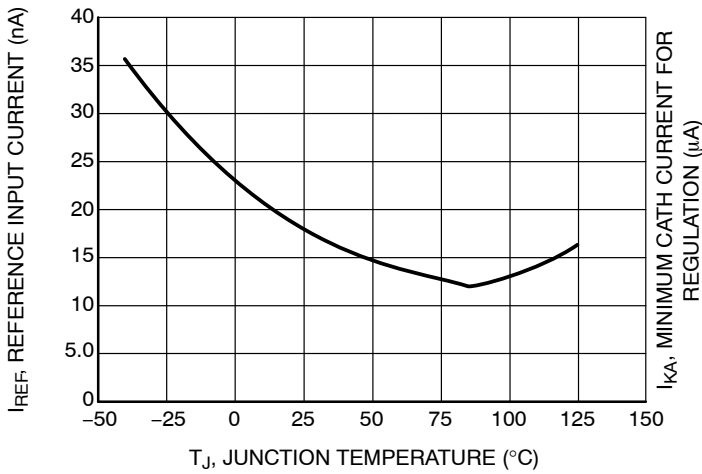


Figure 17. 2.55 V Reference Input Current vs. Junction Temperature

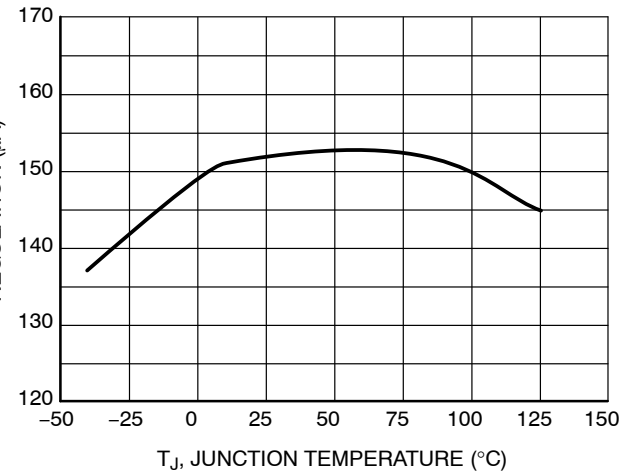


Figure 18. 2.55 V Reference Minimum Cathode Current for Regulation vs. Junction Temperature

TYPICAL CHARACTERISTICS

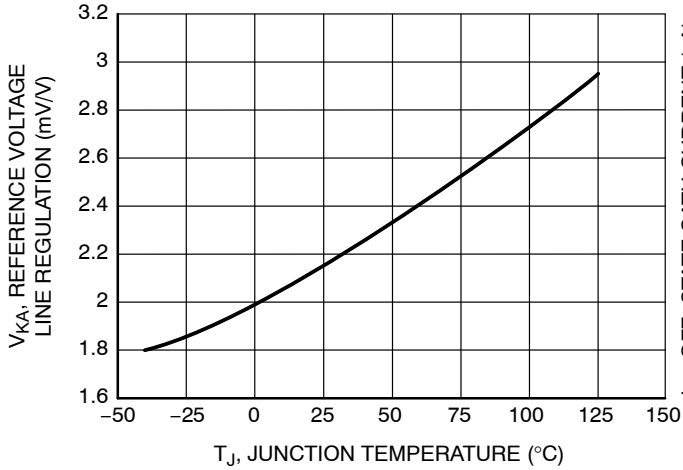


Figure 19. 2.55 V Reference Line Regulation vs. Junction Temperature

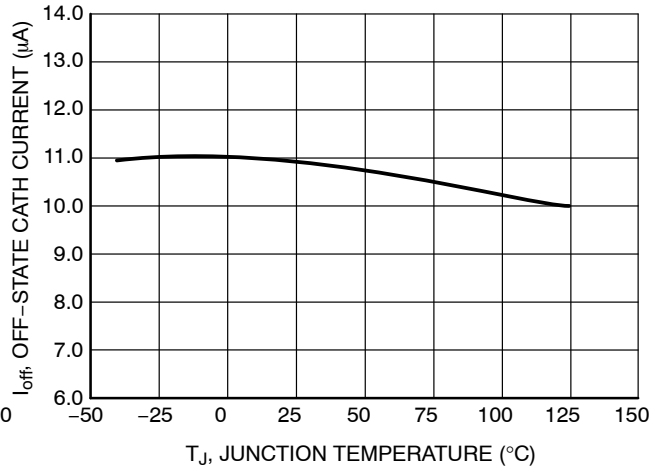


Figure 20. 2.55 V Reference Off-State Cathode Current vs. Junction Temperature

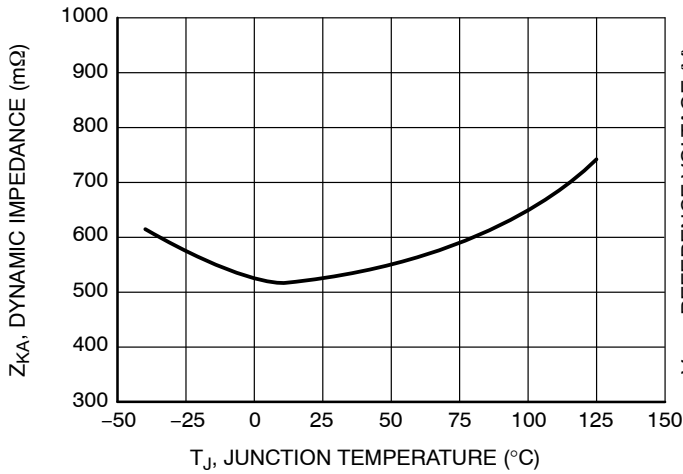


Figure 21. 2.55 V Reference Dynamic Impedance vs. Junction Temperature

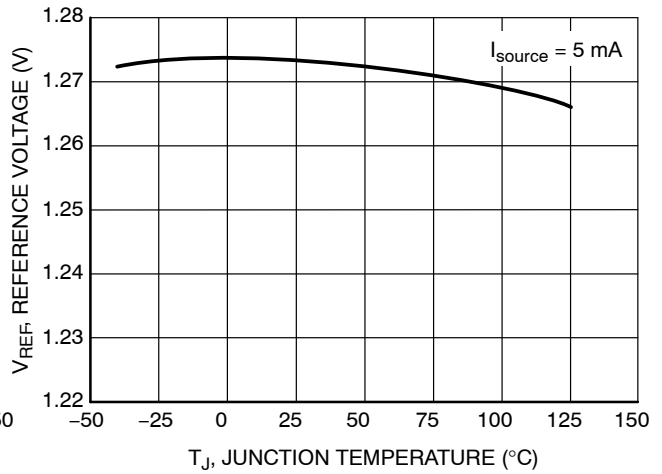


Figure 22. 1.275 V Reference Voltage (Option B) vs. Junction Temperature

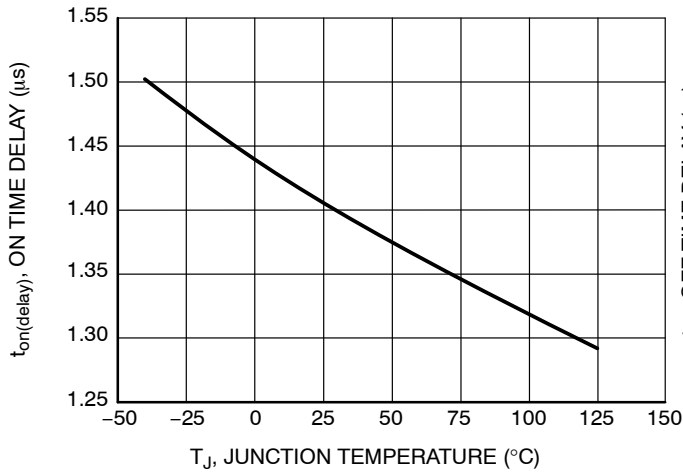


Figure 23. t_{on} Delay vs. Junction Temperature

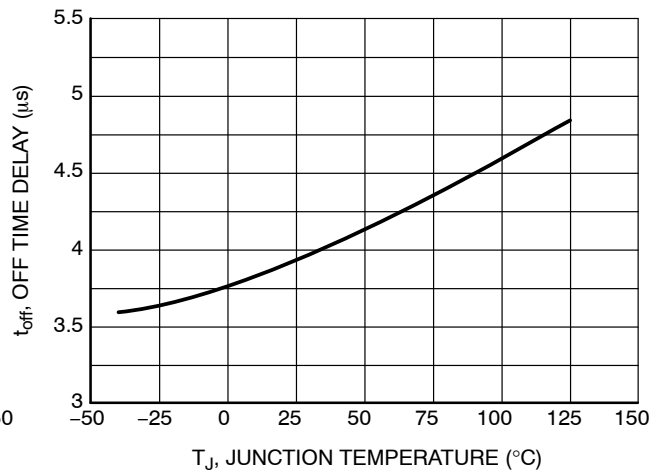


Figure 24. t_{off} Delay vs. Junction Temperature

Detailed Operating Description

The NCP4302 is designed to operate either as a standalone IC or as a companion IC to a primary side controller to help achieve efficient synchronous rectification for flyback converter systems. It has high current gate driver along with fast logic circuitry to provide appropriately timed drive signals to a synchronous MOSFET used for output rectification in a flyback converter. With its novel architecture, the NCP4302 has enough versatility to increase the synchronous rectification efficiency under any operating mode without requiring too much complexity.

Supply Section

The NCP4302 works from an available bias supply that can range from 10.4 V to 28 V (typical). This allows direct connection to the output voltage of many adapters such as notebook and LCD TV adapters. As a result, the NCP4302 simplifies circuit operation compared to other devices which require specific bias power supplies (e.g. 5 V). The high voltage capability of the V_{CC} is also a unique feature designed to allow operation across a broader range of applications. To prevent gate signal from operating under inadequate bias conditions, the NCP4302 features a UVLO circuit that turns on at 10.4 V (V_{CC} rising) typical and turns off at 9.2 V typical (V_{CC} falling).

Gate Drive Section

The NCP4302 features high current gate drivers delivering up to (>2.5 A peak) to achieve fast turn-on and turn-off requirements in a synchronous rectifier. Having a high gate drive current enables fast turn-on when SYNC/CS signal is received (to minimize body diode conduction at the peak of the current waveform) and fast turn-off when zero current or a TRIG signals are received (to prevent current reversal or cross conduction). The higher sink current also allows the MOSFET to be kept off during the instances when there is high dv/dt on the drain.

The gate voltage is clamped at 13.5 V typical to prevent larger excursion of gate voltage than needed when V_{CC} is operating from a 28 Vdc output.

The propagation delays through the logic circuits and the gate drivers are kept at a minimum as shown in the specification table.

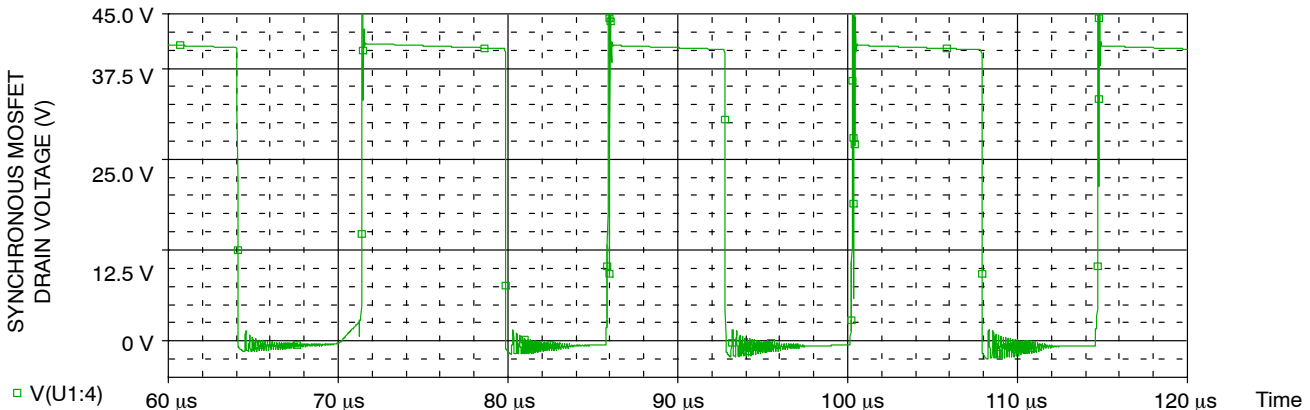


Figure 26. Discontinuous Conduction Mode Drain Waveform

SYNC/CS Input

In a synchronous rectification application after the primary side MOSFET is turned-off, the current in the secondary of the flyback transformer initially flows through the synchronous rectification MOSFET's internal body diode. When this occurs, the drain of the MOSFET will be -0.5 to -1.0 V negative with respect to ground (the V_F of the internal body diode) and the NCP4302 current sense differential amplifier will output a $230 \mu A$ current (typical). This current detection method is used by the NCP4302 to determine when current is flowing in the secondary of the transformer and the Synchronous Rectification MOSFET needs to be turned-on.

The zero current detection senses the current with a slight negative offset so that the switch turn-off occurs without reversal of the current.

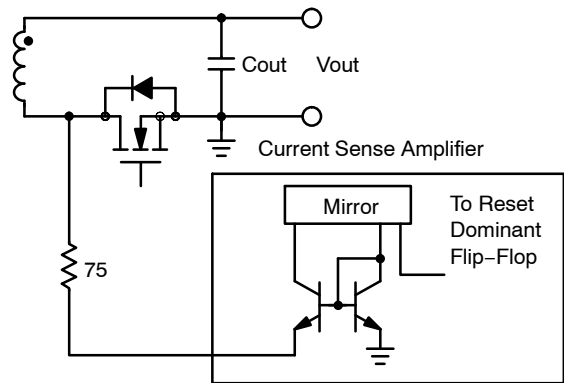


Figure 25. Input Current Sense

Adjustable t_{on} Delay

The SYNC/CS input to the NCP4302 is used as a Reset (through logic) input to the drive enable Flip Flop; refer to the internal block diagram of the NCP4302. When current flows in the secondary of the Flyback transformer any parasitic inductance due to printed wiring board traces, or component lead can cause the voltage at the SYNC/CS input to ring above ground (refer to Figure 26). This ringing may cause the controller drive output to turn-off. To eliminate this problem the NCP4302 has a programmable t_{on} time which blanks the secondary voltage ringing by adding a minimum controller drive on time.

NCP4302

The minimum on time is set with a voltage divider with resistors R2 and R3 (refer to Figure 27).

$$I_{in} = \left(\left(V_{out} \cdot \frac{R3}{R3 + R2} \right) - 0.7 \right) \cdot \frac{1}{R_{th}}$$

Where R_{th} is the Thevenin equivalent resistance and is calculated by:

$$R_{th} = \frac{1}{\frac{1}{R3} + \frac{1}{R2}}$$

This input current is then used to charge an internal 10 pF capacitor setting the minimum t_{on} time.

$$t_{on(delay)} = 10 \text{ pF} \cdot \frac{4 \text{ V}}{I_{in}}$$

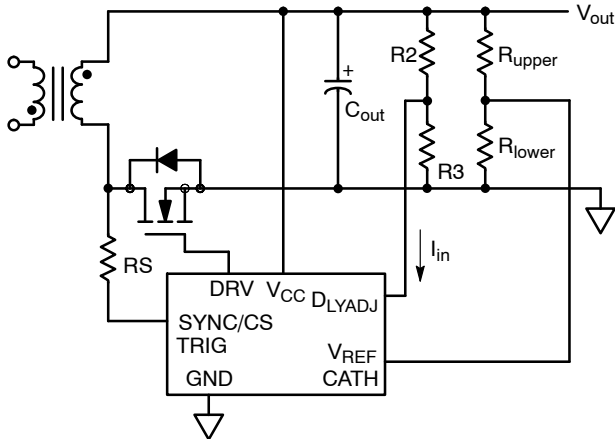


Figure 27. Typical Application

Adjustable t_{off} Delay

The SYNC/CS input to the NCP4302 is used as the Set input to the drive enable Flip Flop; refer to the internal block diagram of the NCP4302. Referring to the SPICE simulations (Figure 28), you can see that when the system is operating under light load conditions the transformer secondary voltage rings below ground when the current reaches zero. When this occurs, the CS amplifier output may be falsely triggered providing a Set input to the Drive Flip Flop, turning on the output drive. To prevent the controller from prematurely turning on the synchronous rectification MOSFET, the output of the current sense amplifier is connected to a logic block with a programmable off time delay. The $t_{off(delay)}$ can be independently programmed through the DLYADJ pin.

$$I_{in} = \left(\left(V_{out} \cdot \frac{R3}{R3 + R2} \right) - 0.7 \right) \cdot \frac{1}{100k}$$

$$t_{off(delay)} = 10 \text{ pF} \cdot \frac{3.35 \text{ V}}{I_{in}}$$

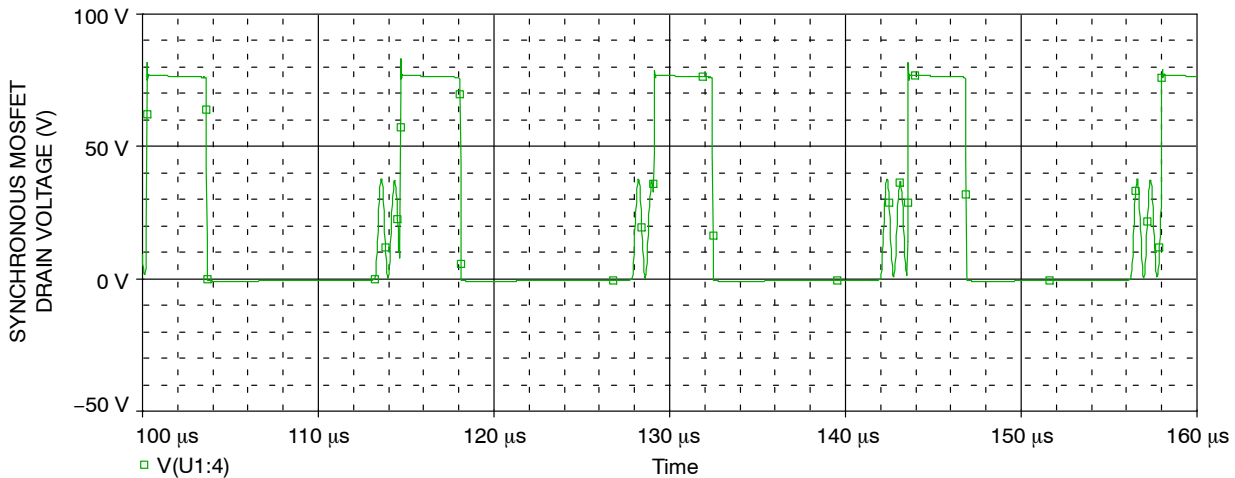


Figure 28. Discontinuous Conduction Mode Drain Waveform

Trigger Input

The TRIG input is used to turn-off the synchronous MOSFET prior to its current reaching zero. This input is required in a CCM operating mode. While there are several ways to determine the TRIG input, the simplest way is to generate a pulse in the primary side that precedes the turn-on of the primary MOSFET and transformer couple that pulse to the secondary into the Trig input. In converters where the operating mode is always designed to be DCM or QRM, the

TRIG input is not used. It is recommended to ground the TRIG pin in these cases.

Voltage Amplifier and Reference

The NCP4302 incorporates an accurate TL431 type Shunt regulator with two reference voltage options. The NCP4302A has a 2.5 V reference and the NCP4302B has a 1.25 V reference.

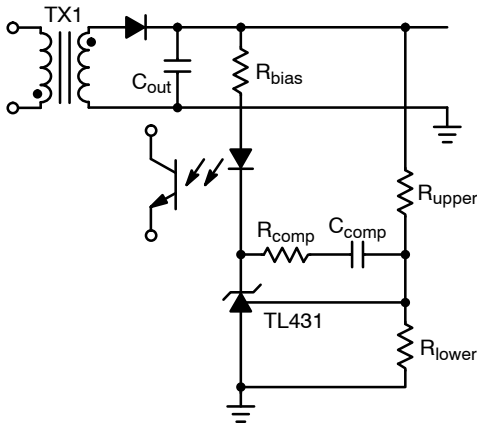


Figure 29. Typical Secondary Side Regulator

When the TL431 is being used to regulate the output of a power supply it is typically configured as shown in Figure 29. Where the output from the power supply is sensed and divided down with a resistive divider made up of R_{upper} and R_{lower} . The center point of the divider is connected to the reference pin of the NCP4302. The divider ratio scales down the output voltage to match the reference voltage, 2.5 V or 1.25 V.

$$V_{REF} = V_{out} \cdot \frac{R_{lower}}{R_{lower} + R_{upper}}$$

The R_{bias} resistor in Figure 29 sets the current through the TL431, which must be greater than 0.5 mA to guarantee its performance under all operating conditions.

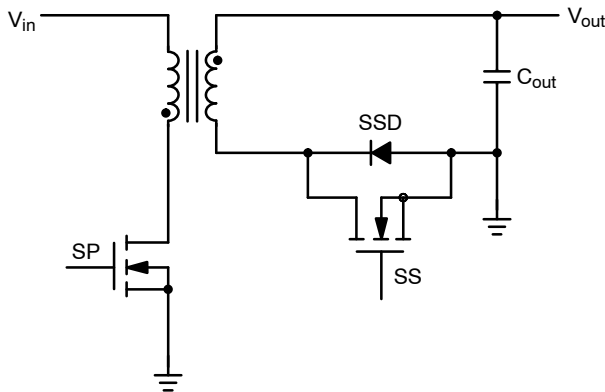


Figure 30. Synchronous Rectifier

Using Synchronous Rectification

For a flyback converter to operate correctly with synchronous rectification there must be a delay between the time when the primary side MOSFET (SP Figure 30) and the secondary side Synchronous rectification MOSFETs (SS Figure 29) are conducting current. The NCP4302 can

operate in CCM, CRM, or QR modes. The next sections cover the losses associated for each of the three operating modes.

Discontinuous Conduction Mode

The basic switching waveforms for the Flyback converter operating in DCM are shown in Figure 31. When the primary side MOSFET (SP in Figure 30) is turned-on current flows in the transformer primary and ramps up from zero to I_{peak} . When the primary side MOSFET (SP) turns-off, the polarity of the transformer reverses and the energy stored in the transformer is transferred to the secondary. When the energy transfer from the transformer primary to the transformer secondary begins, (prior to the secondary side synchronous MOSFET turning-on) the secondary current flows through the internal body diode synchronous rectifiers MOSFETs (SS) and (SSD). To minimize the losses in the SSD, the propagation delay (t_{p1}) must be low. Otherwise, there will be high losses associated with the secondary peak current and the SSD forward voltage drop (NCP4302 has a typical propagation delay of 50 ns).

$$P_{Tsecondary} = P_{on} + P_{SW} + P_{diode} \quad (eq. 1)$$

$$I_{out} = \frac{I_{sec,pk}}{2} \cdot (1 - D_{on}) \quad (eq. 2)$$

$$I_{sec,rms} = I_{sec,pk} \cdot \sqrt{\frac{1 - D_{on}}{3}} \quad (eq. 3)$$

Combining equations 2 and 3,

$$I_{sec,rms}^2 = \frac{4 \cdot I_{out}^2}{3 \cdot (1 - D_{on})} \quad (eq. 4)$$

$$P_{on} = \frac{4 \cdot I_{out}^2}{3 \cdot (1 - D_{on})} \cdot R_{DS(on)} \quad (eq. 5)$$

$$P_{SW} = \frac{1}{2} \cdot C_{OSS} \cdot V_S^2 \cdot f \quad (eq. 6)$$

$$P_{diode} = V_F \cdot I_{out} \cdot t_{delay} \quad (eq. 7)$$

Where:

I_{out} is the dc output current

V_F is

D is the duty cycle

$R_{DS(on)}$ is the on resistance of the MOSFET

$$V_S = \frac{V_{in}}{n} + V_{out}$$

n is the transformer turns ratio

T_{delay} is the delay from the sync to the drive output

Discontinuous Condition Mode

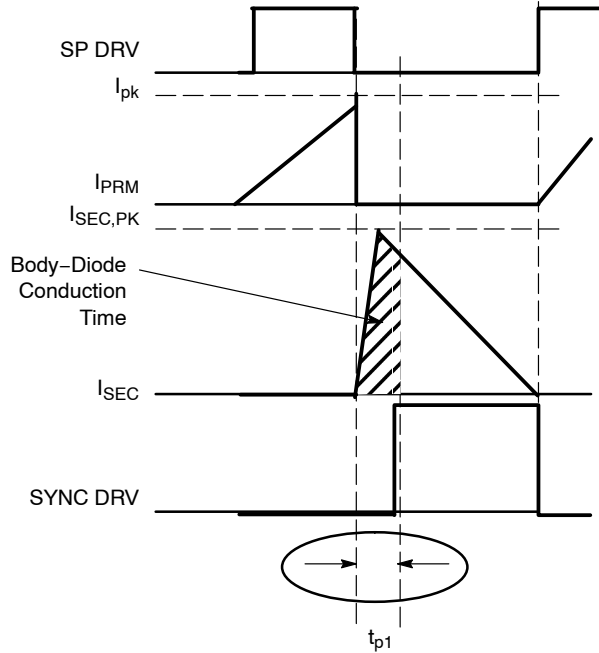


Figure 31. Discontinuous Conduction Mode Waveforms

t_{p1} is the propagation delay from the SYNC/CS input to the drive output.

Continuous Conduction Mode

When operating in continuous conduction mode (CCM) the current in the secondary doesn't fall to zero prior to turning on the primary side MOSFET. To eliminate cross conduction losses (have the primary side MOSFET and secondary side MOSFET on at the same time) the trigger input to the NCP4302 must be utilized. A signal which leads the Primary Side (SP) MOSFET turning on must be coupled to the TRIG input of the NCP4302 which will turn-off the SS MOSFET referring to Figure 32.

When the energy transfer begins in the transformer secondary, prior to the secondary side synchronous MOSFET turning-on, the secondary current flows through the synchronous rectifiers MOSFET's (SS) internal body diode (SSD). To minimize the power loss in the internal body the controller propagation delay has been minimized in the NCP4302.

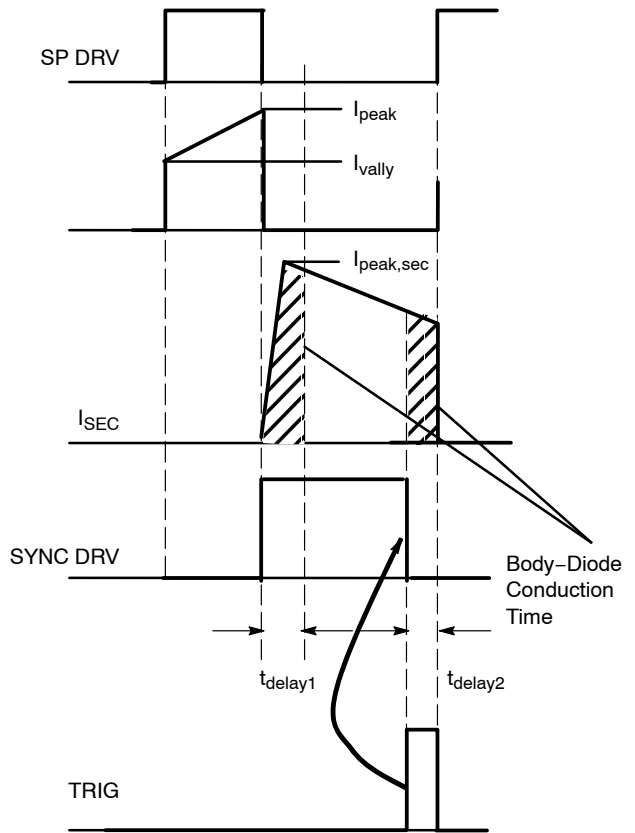


Figure 32. Continuous Conduction Mode Waveforms

$$P_{sync} = P_{ON} + P_{QRR} + P_dP + PP_{OFF} \quad (eq. 8)$$

$$I_{sec,RMS} \approx \left(I_{sec,peak} - \frac{\Delta I_{L_{sec}}}{2} \right) \sqrt{1 - D} \quad (eq. 9)$$

$$I_{sec,RMS}^2 \approx \left(I_{sec,peak} - \frac{\Delta I_{L_{sec}}}{2} \right)^2 (1 - D) \quad (eq. 10)$$

Combining equations 9 and 10,

$$\Delta I_{L_{sec}} = \frac{V_{OUT} + V_f}{\frac{L_M}{n^2}} (1 - D) T \quad (eq. 11)$$

$$P_{on} = I_{sec,RMS}^2 \cdot R_{DS(on)} \quad (eq. 12)$$

$$P_{QRR} = Q_{RR} \left(V_{OUT} + \frac{V_{IN}}{n} \right) f \quad (eq. 13)$$

$$P_{BODY_DIODE} = V_f \cdot I_{OUT} \cdot f(t_{delay1} + t_{delay2}) \quad (eq. 14)$$

$$P_{off} = \frac{1}{2} \cdot C_{OSS} \left(V_{out} + \frac{V_{in}}{n} \right)^2 \cdot f \quad (eq. 15)$$

Q_{RR} is the recovery charge of the internal body diode
 C_{OSS} is the MOSFET drain to source capacitance
 L_M is the transformer primary inductance

NCP4302

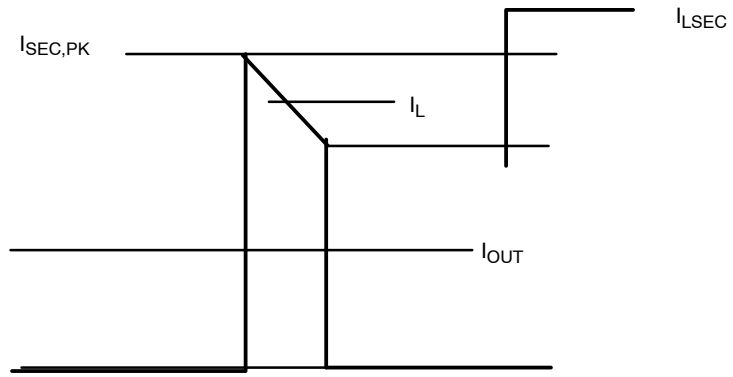


Figure 33.

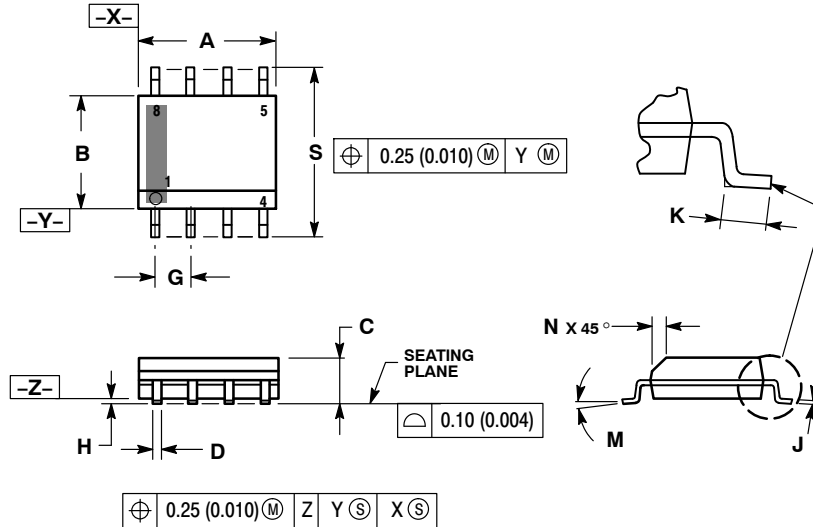
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

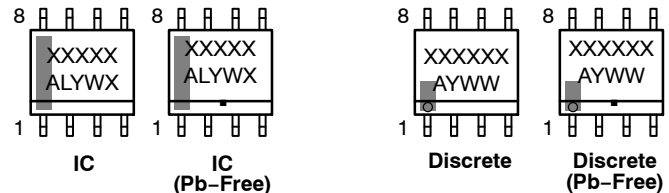
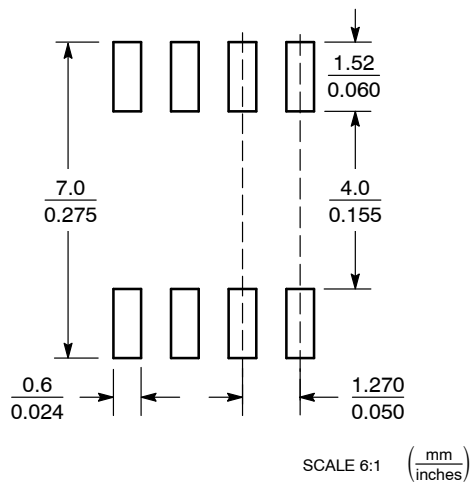


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

GENERIC MARKING DIAGRAM*

SOLDERING FOOTPRINT*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

- | | | | |
|---|--|--|--|
| <p>STYLE 1:
 PIN 1. EMITTER
 2. COLLECTOR
 3. COLLECTOR
 4. EMITTER
 5. EMITTER
 6. BASE
 7. BASE
 8. EMITTER</p> | <p>STYLE 2:
 PIN 1. COLLECTOR, DIE, #1
 2. COLLECTOR, #1
 3. COLLECTOR, #2
 4. COLLECTOR, #2
 5. BASE, #2
 6. EMITTER, #2
 7. BASE, #1
 8. EMITTER, #1</p> | <p>STYLE 3:
 PIN 1. DRAIN, DIE #1
 2. DRAIN, #1
 3. DRAIN, #2
 4. DRAIN, #2
 5. GATE, #2
 6. SOURCE, #2
 7. GATE, #1
 8. SOURCE, #1</p> | <p>STYLE 4:
 PIN 1. ANODE
 2. ANODE
 3. ANODE
 4. ANODE
 5. ANODE
 6. ANODE
 7. ANODE
 8. COMMON CATHODE</p> |
| <p>STYLE 5:
 PIN 1. DRAIN
 2. DRAIN
 3. DRAIN
 4. DRAIN
 5. GATE
 6. GATE
 7. SOURCE
 8. SOURCE</p> | <p>STYLE 6:
 PIN 1. SOURCE
 2. DRAIN
 3. DRAIN
 4. SOURCE
 5. SOURCE
 6. GATE
 7. GATE
 8. SOURCE</p> | <p>STYLE 7:
 PIN 1. INPUT
 2. EXTERNAL BYPASS
 3. THIRD STAGE SOURCE
 4. GROUND
 5. DRAIN
 6. GATE 3
 7. SECOND STAGE Vd
 8. FIRST STAGE Vd</p> | <p>STYLE 8:
 PIN 1. COLLECTOR, DIE #1
 2. BASE, #1
 3. BASE, #2
 4. COLLECTOR, #2
 5. COLLECTOR, #2
 6. EMITTER, #2
 7. EMITTER, #1
 8. COLLECTOR, #1</p> |
| <p>STYLE 9:
 PIN 1. EMITTER, COMMON
 2. COLLECTOR, DIE #1
 3. COLLECTOR, DIE #2
 4. EMITTER, COMMON
 5. EMITTER, COMMON
 6. BASE, DIE #2
 7. BASE, DIE #1
 8. EMITTER, COMMON</p> | <p>STYLE 10:
 PIN 1. GROUND
 2. BIAS 1
 3. OUTPUT
 4. GROUND
 5. GROUND
 6. BIAS 2
 7. INPUT
 8. GROUND</p> | <p>STYLE 11:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. DRAIN 2
 7. DRAIN 1
 8. DRAIN 1</p> | <p>STYLE 12:
 PIN 1. SOURCE
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 13:
 PIN 1. N.C.
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> | <p>STYLE 14:
 PIN 1. N-SOURCE
 2. N-GATE
 3. P-SOURCE
 4. P-GATE
 5. P-DRAIN
 6. P-DRAIN
 7. N-DRAIN
 8. N-DRAIN</p> | <p>STYLE 15:
 PIN 1. ANODE 1
 2. ANODE 1
 3. ANODE 1
 4. ANODE 1
 5. CATHODE, COMMON
 6. CATHODE, COMMON
 7. CATHODE, COMMON
 8. CATHODE, COMMON</p> | <p>STYLE 16:
 PIN 1. EMITTER, DIE #1
 2. BASE, DIE #1
 3. EMITTER, DIE #2
 4. BASE, DIE #2
 5. COLLECTOR, DIE #2
 6. COLLECTOR, DIE #2
 7. COLLECTOR, DIE #1
 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:
 PIN 1. VCC
 2. V2OUT
 3. V1OUT
 4. TXE
 5. RXE
 6. VEE
 7. GND
 8. ACC</p> | <p>STYLE 18:
 PIN 1. ANODE
 2. ANODE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. CATHODE
 8. CATHODE</p> | <p>STYLE 19:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. MIRROR 2
 7. DRAIN 1
 8. MIRROR 1</p> | <p>STYLE 20:
 PIN 1. SOURCE (N)
 2. GATE (N)
 3. SOURCE (P)
 4. GATE (P)
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 21:
 PIN 1. CATHODE 1
 2. CATHODE 2
 3. CATHODE 3
 4. CATHODE 4
 5. CATHODE 5
 6. COMMON ANODE
 7. COMMON ANODE
 8. CATHODE 6</p> | <p>STYLE 22:
 PIN 1. I/O LINE 1
 2. COMMON CATHODE/VCC
 3. COMMON CATHODE/VCC
 4. I/O LINE 3
 5. COMMON ANODE/GND
 6. I/O LINE 4
 7. I/O LINE 5
 8. COMMON ANODE/GND</p> | <p>STYLE 23:
 PIN 1. LINE 1 IN
 2. COMMON ANODE/GND
 3. COMMON ANODE/GND
 4. LINE 2 IN
 5. LINE 2 OUT
 6. COMMON ANODE/GND
 7. COMMON ANODE/GND
 8. LINE 1 OUT</p> | <p>STYLE 24:
 PIN 1. BASE
 2. EMITTER
 3. COLLECTOR/ANODE
 4. COLLECTOR/ANODE
 5. CATHODE
 6. CATHODE
 7. COLLECTOR/ANODE
 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25:
 PIN 1. VIN
 2. N/C
 3. REXT
 4. GND
 5. IOUT
 6. IOUT
 7. IOUT
 8. IOUT</p> | <p>STYLE 26:
 PIN 1. GND
 2. dv/dt
 3. ENABLE
 4. ILIMIT
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. VCC</p> | <p>STYLE 27:
 PIN 1. ILIMIT
 2. OVLO
 3. UVLO
 4. INPUT+
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. DRAIN</p> | <p>STYLE 28:
 PIN 1. SW_TO_GND
 2. DASIC_OFF
 3. DASIC_SW_DET
 4. GND
 5. V_MON
 6. VBULK
 7. VBULK
 8. VIN</p> |
| <p>STYLE 29:
 PIN 1. BASE, DIE #1
 2. EMITTER, #1
 3. BASE, #2
 4. EMITTER, #2
 5. COLLECTOR, #2
 6. COLLECTOR, #2
 7. COLLECTOR, #1
 8. COLLECTOR, #1</p> | <p>STYLE 30:
 PIN 1. DRAIN 1
 2. DRAIN 1
 3. GATE 2
 4. SOURCE 2
 5. SOURCE 1/DRAIN 2
 6. SOURCE 1/DRAIN 2
 7. SOURCE 1/DRAIN 2
 8. GATE 1</p> | | |

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